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Scandium oxide deposited by high-pressure sputtering for memory devices: Physical and interfacial properties

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Scandium oxide (ScO_x) thin layers are deposited by high-pressure sputtering (HPS) for physical and electrical characterization. Different substrates are used for comparison of several ScO_x/Si interfaces. These substrates are chemical silicon oxide (SiO_x), H-terminated silicon surface and silicon nitride (SiN_x), obtained by either electron-cyclotron-resonance chemical vapor deposition or plasma enhanced nitridation of the Si surface. Transmission electron microscopy images show that a 1.7 nm thick SiO_x layer grows when ScO_x is deposited on H-terminated silicon surface. We demonstrate that interfacial SiN_x has some advantages over SiO_x used in this work: its permittivity is higher and it presents better interface quality. It also avoids Si oxidation. An improvement of one order of magnitude in the minimum of interface trap density is found for SiN_x with respect to the SiO_x, reaching values below 2×10^{11} cm^{-2} eV^{-1}. HPS deposited ScO_x films are polycrystalline with no preferential growth direction for the used deposition conditions and their properties do not depend on the substrate. This material could be a candidate for high-*k* material in flash memory applications. © *2010 American Institute of Physics*. [doi:10.1063/1.3354096]

I. INTRODUCTION

Recently, scandium oxide thin films and ternary based compounds such as $GdScO_3$,[1,2] $DyScO_3$,[3,4] and $LaScO_3$ (Ref. 5) have attracted increasing interest in the microelectronic field in two main areas: flash memories and complementary metal-oxide-semiconductor (CMOS) circuits. In flash memory applications,[6] for technology nodes below 45 nm, dielectrics with a relative permittivity *k* in the 9–20 range and band gaps larger than 5 eV are of interest. These can be used for electrical isolation between the control gate and the charge storage layer for both floating gate memories *(flotox)* and charge trap memories. Sc_2O_3 presents a band gap (~6 eV) (Ref. 7) and a *k* value (~13),[8] suitable for these applications.[9] In *flotox* memories, the insulator is sandwiched between the poly-Si gates[10] and is called inter-poly-Si dielectric (IPD). In charge trap memories, the insulator or blocking oxide (BO) lies in contact with a silicon nitride trapping layer and a *p*-type metal.[11] Thus, any material integrated in these memories must be compatible with the variety of materials that is in contact with. As a consequence, for Sc_2O_3 integration, it is important to check the stability of the dielectric layer with Si, Si oxide, and Si nitride.

In CMOS circuits the continuous scaling down of equivalent oxide thickness (EOT) requires a gate insulator with dielectric permittivities in the 10–30 range and band gaps larger than 5 eV, while keeping high values of the conduction band offset with Si.[12] Although pure Sc_2O_3 permittivity is not very high for this application, its ternaries with rare-earths could match well these requirements, together with an excellent thermal stability with Si.[1]

An important issue of high-*k* dielectrics is the interface with Si. A passivation layer of SiO_2 or SiON thin films is commonly used. So far, the problems that the high-*k* dielectrics show have been partially solved with the use of an extremely thin (1 nm or below) SiO_2, thermally or chemically grown on the Si surface prior to the high-*k* dielectric deposition. Such approach has proven to be reasonably effective to solve some problems, but different ways should be analyzed. Among them, we propose the use of silicon nitride (SiN_x) as interfacial layer between high-*k* and silicon to reduce the EOT of the structure.[13]

Up to the moment, Sc_2O_3 thin films with suitable properties are successfully deposited by atomic layer deposition (ALD),[14] but a wide variety of precursor gases are under study and no universal precursor gases are today used. It is important to note that the main drawback of this technique is the complexity in controlling the chemistry of the precursors in order to achieve the completeness of the reactions involved. To produce a relatively thick film by ALD a high amount of precursors must be consumed, and their fabrication includes environmental hazards. Furthermore, although it is usually not mentioned, the ALD films present a high amount of carbon/chlorine content from the precursor, which can be problematic as a source of contamination.

In this work the physical and electrical properties of scandium oxide grown by high-pressure sputtering (HPS) are studied. This deposition technique does not pose the mentioned precursor problem that ALD does. It is well-known that the structure and physical properties of the films grown by sputtering strongly depend on the energy of the particles that reach the substrate. In our nonconventional sputtering deposition method, the working pressure is around 1 mbar, three orders of magnitude higher than a conventional sputtering system. Due to the high pressure the mean free path of the processing gas (Ar), is significantly short (around 0.05 mm). Therefore, the sputtered and reflected particles emitted

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from the target collide with the gas medium losing energy and thermalizing within a short distance, in the 0.1–0.3 cm range for both sputtered and reflected atoms. This thermalization length is much shorter than the target-substrate distance (2.5 cm), so the transport of sputtered particles to the substrate is due to a purely diffusion process. Consequently, the energy of the reflected and sputtered atoms is low enough to prevent damage of the substrate and the growing film itself. This technique has been used to grow high-T_c superconductors[15,16] and we successfully used it to deposit TiO_2 and HfO_2 high-*k* dielectric films.[17–19] It also permits ternary compounds to be grown with a multitarget system which is a very interesting characteristic to pursue scandates research.

Following the previous introduction, in this paper we present a thorough study of the physical and electrical properties of scandium oxide deposited by HPS on different substrates: bare-Si, chemical SiO_2, and several types of SiN_x (deposited and nitrided Si surface).

II. EXPERIMENTAL

A. Fabrication process

The stacked structures were fabricated on single side polished n-Si (100) wafers with a resistivity of 1.5–5.0 Ω cm. To measure the infrared absorbance of the different layers, double side polished n-Si (100) wafers with a resistivity of 200–1000 Ω cm were used. All wafers were cleaned using a standard RCA (*Radio Corporation of America*) process.

We deposited ScO_x on five differently prepared Si substrates: (1) H-terminated Si surface, (2) RCA native oxide, (3) SiN_x deposited, and (4–5) nitrided Si for different times. The H-terminated Si surface was achieved by an etching process of the RCA cleaned substrates in a HF diluted solution for 30 s. This was performed immediately before the introduction of the sample to the HPS chamber. SiN_x was deposited with an electron-cyclotron-resonance (ECR) chemical vapor deposition system[20] using high purity N_2 and SiH_4 as precursor gases, with a N_2/SiH_4 ratio of 9:1 and a total gas flow of 10.5 sccm. The base pressure was 7×10^{-7} mbar and was kept constant at 9×10^{-4} mbar during deposition. The microwave power was fixed at 100 W and the deposition temperature at 200 °C. Finally, ECR nitridation was carried out using N_2 at a 10.5 sccm flow for 30 s and 10 min. ECR samples were HF-etched in N_2 atmosphere and transferred to the ECR chamber without being exposed to atmosphere.

The scandium oxide films were deposited on the differently processed substrates by HPS in pure Ar atmosphere. The deposition conditions for all samples were identical; hence the only intentional difference was the starting substrate. The deposition pressure was 0.50 mbar (base pressure 2×10^{-6} mbar). A commercial 4.5 cm diameter high purity Sc_2O_3 target was used. The 13.54 MHz radio frequency (RF) power was kept at 40 W. Depositions were performed during 2 h keeping the substrate temperature at 200 °C.

For electrical characterization, 500×500 μm^2 metal-insulator-semiconductor (MIS) devices were defined by e-beam evaporation of Al electrodes followed by standard lithography process. After top electrode definition, Al was evaporated to the backside and the samples were annealed during 20 min at 300 °C in forming gas atmosphere (FGA process).

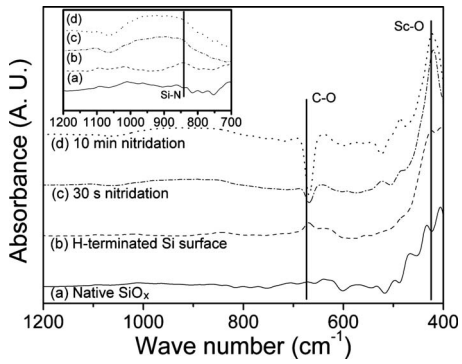

FIG. 1. FTIR spectra of the stacks in the 1200–400 cm^{-1} region: (a) scandium oxide deposition on RCA chemical SiO_x, (b) deposition after etching in HF dilute solution, (c) after 30 s nitridation, and (d) after 10 min nitridation.

B. Characterization techniques

The infrared absorbance of the samples was measured by Fourier transform infrared (FTIR) spectroscopy in the 400–4000 cm^{-1} range using a Nicolet Magma-IR 750 series II spectrometer working in transmission mode at normal incidence to analyze the chemical bonds of the grown layers. A XPERT MRD of Panalytical was used to measure glancing incidence x-ray diffraction (GIXRD) at $\omega=0.5°$ in order to study crystal structure of deposited scandium oxide films. The stacks were characterized by means of cross sectional transmission electron microscopy (TEM) images using a JEOL-JEM-2000FX microscope operating at 200 KeV. In selected samples, high resolution TEM (HRTEM) was performed with a JEOL-JEM-4000EX at 400 KeV. TEM measurements allowed us to determine thicknesses and morphology of films. MIS devices were electrically characterized by the well-known high-frequency/quasi-static C-V method using a Keithley 82 system. From these measurements, EOTs of the stacks are extracted and the energy distribution of interface traps (D_{it}) can be calculated as long as the gate leakage is low enough to avoid quasistatic capacitance distortion.[21] For comparison, C-V and G-V measurements were performed with an Agilent 4294A impedance analyzer and D_{it} was also evaluated by the conductance method.[21] Finally, a Keithley 4200-SCS was used to obtain the gate leakage current at inversion of the stacks as a function of gate bias voltage.

III. EXPERIMENTAL RESULTS

Figure 1 shows representative FTIR spectra of the stacks in the 400–1200 cm^{-1} range. Outside this region there are no other significant features present. These spectra are substrate corrected. The substrate used for correction is RCA cleaned wafer, which is thus covered by a chemical oxide. The peak at 667 cm^{-1} is characteristic of the C–O bond and it is caused by the presence of CO_2 in the chamber of the measurement system, so it will not be further discussed. Two

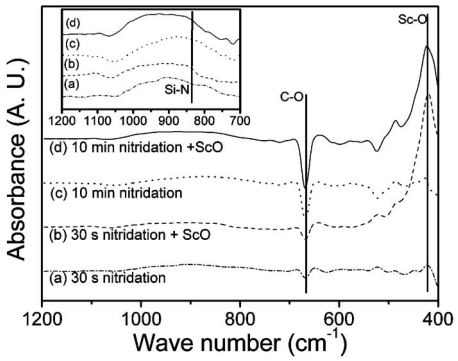

FIG. 2. FTIR spectra of the silicon nitride layers in the 1200–400 cm^{-1} region: (a) 30 s nitridation, (b) 10 min nitridation, (c) 30 s nitridation +ScO_x deposition, and (d) 10 min nitridation+ScO_x deposition.

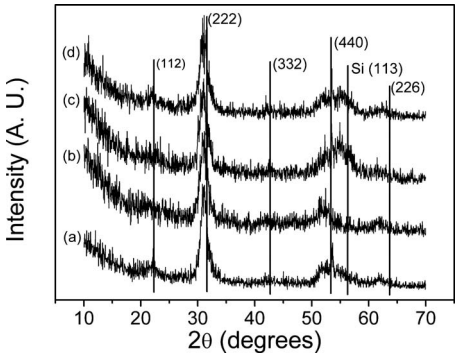

FIG. 3. GIXRD diagrams of ScO_x films deposited on (a) RCA chemical oxide, (b) H-terminated Si surface, (c) 10 min nitrided Si surface, and (d) 30 s nitrided Si surface. The marked crystallographic planes correspond to the most intense peaks in Sc_2O_3 cubic phase.

main features appear clearly in the FTIR spectra: between 400–500 cm^{-1} in all samples and between 800–1100 cm^{-1} only in nitride samples.

First we will focus on the 800–1100 cm^{-1} region. As it can be seen in the inset of Fig. 1, the nitrided samples present a wide and quite flat band centered around 900 cm^{-1} and a valleylike feature around 1065 cm^{-1}. Due to the flatness of the peak together with the baseline of the spectra it is difficult to assure where the maximum is located. Stoichiometric Si_3N_4 has a stretching vibration mode[22] at 835 cm^{-1} so we attribute the measured band to the formation of SiN_x during the nitridation process. The shift toward higher wave numbers may be related to O incorporation[23] to this passivation layer as a contamination from the ECR quartz chamber. Also, the width of the band points to a quite disordered layer. In other words, the angle and distance value spread of the Si–N bonds is bigger than relaxed Si_3N_4 films, and this distribution gives rise to a wider distribution of resonance frequencies. Incidentally, this band is slightly more apparent for the longer nitridation time, which means a thicker SiN_x layer.

The valley at 1065 cm^{-1} is caused by the substrate signal correction as the bare substrates used for correction have a 1–2 nm thick chemical oxide due to the RCA process. Then their absorbance spectra show a Si–O peak at that wave number.[24] This indicates that the content of Si–O bonds in the nitrided samples is lower than in the reference substrate, i.e., the thickness of the interfacial SiO_x in the nitrided samples (if present) is lower than in the RCA chemical oxide. The un-nitrided samples do not show any peak or valley at 1065 cm^{-1}, which indicates that the SiO_x thickness in the stack must be comparable to the RCA chemical oxide.

To gain further insight into the nitride passivation role, FTIR spectra of SiN_x layers were also obtained before ScO_x sputtering deposition and they are represented in Fig. 2. Comparing the spectra before and after sputtering of ScO_x for both nitridation times in the inset of Fig. 2, it can be observed that the band at 900 cm^{-1} and the valley at 1070 cm^{-1} remain present after deposition. Thus, the SiN_x layer is still present and there is no detectable SiO_x regrowth during sputtering. Analogous results can be extracted for deposited SiN_x.[19]

The increase in the absorbance in the 400–500 cm^{-1} range can be associated to Sc–O bonds. This is confirmed by FTIR spectra before and after ScO_x deposition in Fig. 2. It is observed that before sputtering the region between 400 and 500 cm^{-1} remains almost flat, but after ScO_x deposition a peak appears with its maximum at about 420 cm^{-1}. Hardy *et al.*[24] found FTIR peaks at 609 and 711 cm^{-1} for scandium oxide deposited layers. Also, other works[25] propose that Sc_2O_3 has FTIR absorption peaks at 625 and 425 cm^{-1}. Our samples did not present any peak at 609 cm^{-1} or 711 cm^{-1} and at 625 cm^{-1} it is difficult to assure it since it is very close to the CO_2 absorption. However, all samples with the ScO_x layer, including un-nitrided samples from Fig. 1, present the increase in the absorbance in the region around 425 cm^{-1} which supports the conclusion of being related to Sc–O bonds.

Concerning the crystal structure of the stacks, Fig. 3 shows the GIXRD spectra of the deposited scandium oxide films. The only known polymorph of Sc_2O_3 is the cubic bixbyite phase.[26] The most intense peaks of this Sc_2O_3 cubic phase are marked in the graphic. The spectra show that all samples, independent on the substrate type, crystallize in the same cubic phase, without relevant differences. In most samples it can be appreciated that there is a remaining of the (113) plane of the crystalline Si substrate at 2θ=56.4°. This is caused by the relatively low thickness of the scandium oxide film and the glancing incidence of the x rays. According to the relative intensity of the Sc_2O_3 peaks, it can be concluded that there is no preferential direction in the polycrystalline growth.

The most relevant conclusion that can be extracted is that the as-deposited films are polycrystalline, and they do not need further heat treatments to crystallize. It must be noticed that the highest temperature that these ScO_x films reached is 200 °C during deposition process. This is an advantage for memories, where crystal phases are preferred due to their higher dielectric permittivity, but the crystallization temperature should remain below 650 °C in order to enable successful integration with device fabrication.[6]

TEM was used in order to determine the thicknesses of the layers and to confirm the previously shown results (polycrystallinity and interface integrity). The most relevant images that were obtained are displayed in Fig. 4. Figure 4(a) shows scandium oxide film deposited on an H-terminated Si surface. The image shows that a bright layer appears between

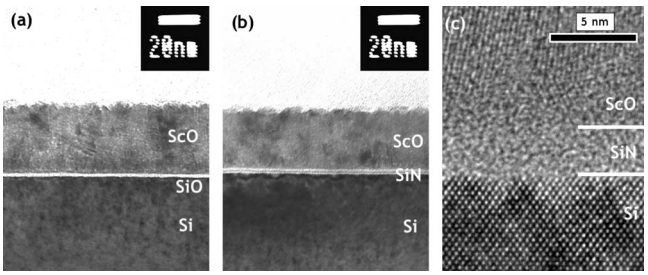

FIG. 4. Cross-sectional TEM images of the ScO_x deposited films (a) on RCA Si after etching in a HF diluted solution and (b) on Si nitrided during 30 s. (c) Cross-sectional HRTEM image of a sample that consists in an interface (30 s nitridation) and ScO_x sputtering deposition. The thickness of the interface layer is 2.8 nm.

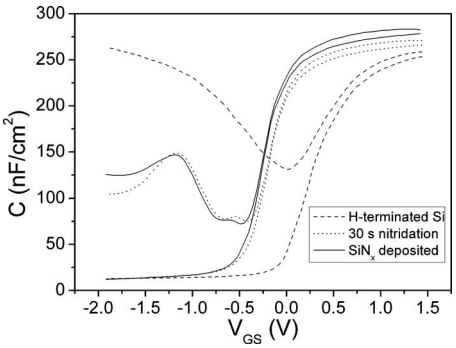

FIG. 5. C_{QS} and C_{HF} characteristics of the stacks.

two darker layers. The top dark layer is the ScO_x film and the layer in the bottom is the Si substrate. The bright layer is silicon oxide that has been grown between the high-*k* dielectric and the Si and its thickness is about 1.7 nm. The formation of this layer could be explained by the O diffusion through the ScO_x film during growth. It must be noticed that SiO_x thickness is low, compared, for instance, with TiO_2 that in similar conditions forms a ~6 nm interface[17] or HfO_2 that presents ~3 nm.[27] This indicates that ScO_x might be more effective in blocking oxygen-radicals diffusion than TiO_2 or HfO_2.

The thickness of the ScO_x layer is around 30 nm, and the image confirms the polycrystalline character of the ScO_x film. Additionally it is observed that the nanocrystals are randomly oriented, with no preferential growth direction which is in agreement with GIXRD measurements. This is in contrast with previous HfO_2 results obtained with the same system,[28] which showed a columnar growth. Finally, close to the interface the nanocrystals are not so clearly observed, suggesting an amorphous initial growth stage. These results show that if an amorphous layer was needed, for example, as a gate dielectric, different HPS deposition conditions should be explored, like substrate temperature, target to substrate distance or RF power. Previous works of our group showed that HfO_2 films deposited with Ar plasma were amorphous whereas deposited films with plasmas of O_2 or different Ar/O_2 ratios were polycrystalline.[29] This will be the subject of future work.

No significant differences in thickness or in polycrystallinity were found for the ScO_x layer deposited on different substrates. Thickness spread was about 20%, which is not surprising due to the long deposition processes (2 h). The main differences are in the ScO_x/Si interface, as we will discuss in the following paragraphs.

In Fig. 4(b), the ScO_x film was deposited on a 30 s nitrided Si. A 2.8 nm interface layer can be observed which is SiN_x after FTIR results. In the figure, the film seems to present three-layer structure, but this might be a TEM artifact. In order to clarify this, HRTEM of the same sample was performed with a higher resolution microscope. Figure 4(c) shows this interface in more detail. It can be seen that the interface is amorphous and homogeneous, with no observable differences as a function of depth, so we can discard a three-layer structure of the nitride. In TEM images of deposited SiN_x (not shown), it is observed that a 3.5 nm thick silicon nitride layer has grown and its structure is also amorphous. From these results, together with FTIR measurements, we conclude that silicon nitride (either deposited or grown from Si) is effective in blocking Si re-oxidation during the initial stages of sputtering.

Finally, capacitance results will be discussed. Quasistatic C_{QS} and high-frequency C_{HF} (100 kHz) C-V characteristics were measured for the stacks with an Al gate. This measuring method is very reliable for D_{it} extraction which is calculated from the difference between the high-frequency and the low-frequency curve in depletion when the bias is swept from accumulation to inversion. However, this technique needs MIS devices with very low leakage current. Otherwise quasistatic C-V is impossible to be measured in thin films. This means that thick insulator layers have to be used, and it is the reason why we used thick 30 nm ScO_x layers. Furthermore, for permittivity calculation, thick layers are less sensitive to interface thickness or dielectric inhomogeneities, since most of the capacitance is due to the high-*k* dielectric.

The most significant curves are shown in Fig. 5. High-frequency C-V curves have been analyzed by the Hauser algorithm.[30] The EOTs are too high for high performance applications but they are in the order used for BO or IPD in flash memories.

Samples with silicon nitride interface have a higher capacitance in accumulation, which means an improvement of the EOT of the structure of 1.4 nm (from 13.1 to 11.7 nm). This is a consequence of the higher *k* value of the SiN_x. Another interesting feature is the displacement of the flatband voltage of the devices with SiN_x (from 0.2 to −0.3 V) which can mean trapped positive charges in the SiN_x layer. Besides, the devices with nitride interfaces show a much more abrupt decrease in the high frequency capacitance. This last effect prompts an improvement in the interfacial density of states (high D_{it} has the effect of screening gate potential,[31] producing a "stretch-out" of the C-V curve).

Nevertheless, when the SiN_x is present, the quasi-static capacitance in inversion does not recover its value of accumulation, which does not happen in samples with SiO_x as an interfacial layer. The reason of this effect is still not completely clear. A possibility is that it can be associated to an intrinsic property of the interfacial SiN_x, but in the past, $HfO_2/SiN_x/Si$ stacks were grown that did not show this problem.[20] Another reason of such effect could be a higher

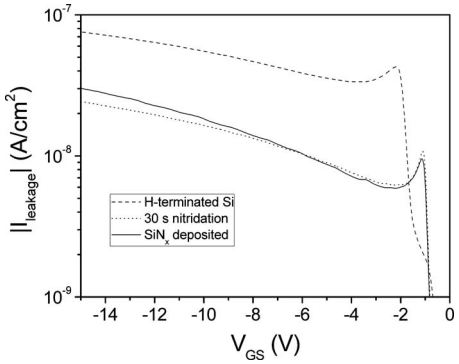

FIG. 6. Gate leakage current in inversion of ScO_x deposited on different substrates as a function of gate bias voltage.

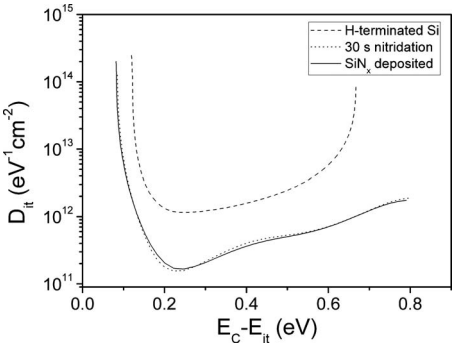

FIG. 7. Density of states D_{it} obtained from C-V characteristics of Fig. 5 as a function of interface trap energy measured from Si conduction band.

gate leakage in inversion due to the smaller band gap of SiN_x compared to SiO_x. The I-V curves of the stacks can be seen in Fig. 6. Samples with SiN_x interfaces present slightly higher leakages than those of samples with SiO-like interfaces at low inversion voltages, but every curve is close to the detection limit of the measurement system. These small differences are not supposed to explain by themselves the behavior of the quasi-static capacitance. Another possible explanation is that this effect is related to charge trapping centers, either in the SiN_x or in the Si surface. A similar behavior was previously found by our group in SiN_x/plasma-oxidized-SiO_2/Si stacks,[32] and we found that after thermal treatments the devices recovered the capacitance in inversion, hi this way, since these MIS devices have only been subjected to a 300 °C FGA, it is likely that thermal annealing will improve their electrical behavior. All these effects are independent from the growth of silicon nitride: a deposition or a nitridation of the Si surface.

The dielectric permittivities of the deposited films were estimated by modeling the capacitance as two capacitors in series, where one is the interlayer and the other is the ScO_x deposition. For calculation, the interfacial layer is considered silicon oxide or silicon nitride, depending on the process of each wafer. Thus, the interlayer permittivity values k_{IL}, that were used, are 3.9 and 8, respectively. The thickness of the interlayer (t_{IL}) and of the ScO_x (t_{ScO}) were obtained from TEM images. Then, the ScO_x permitivity can be calculated as follows:

$$k_{ScO} = \frac{t_{ScO}}{\mathrm{EOT}/k_{SiO} - t_{IL}/k_{IL}}, \quad (1)$$

where k_{SiO} is 3.9, silicon oxide permittivity. This way, as expected, all ScO_x films show a close permittivity value, with a mean value of 9 ± 1. This value is slightly lower than the bulk values reported in literature of about 13.[6] This fact is usual for many thin film materials, but in our case Al might be reacting with the top ScO_x surface, forming an Al scandate and decreasing the effective permittivity.[33] In order to avoid this effect, we are currently working in the substitution of wet-etched Al by lifted-off Pt which is more stable.

Figure 7 depicts the D_{it} extracted from the C-V characteristics[21] of Fig. 5. Thanks to the silicon nitride interlayer, the minimum in the D_{it} decreases from 10^{12} for the SiO_x/Si interface to 10^{11} eV^{-1} cm^{-2} for both deposited SiN_x and 30 s nitrided Si surface. The outcome of these measurements is that there is a significant improvement of the high-k/Si interface with nitride introduction. The D_{it} of the samples have been also calculated by the conductance method at a frequency of 100 kHz. Table I summarizes the results of the two methods for the different substrates used in this work. Although conductance method tends to yield lower D_{it} values compared with the C-V method, it can be clearly observed that the tendency is the same for both methods and the presence of the SiN_x, either deposited or by nitridation of the Si surface, increases interface quality between the high-k and the Si.

IV. SUMMARY AND CONCLUSIONS

In this work, we drew conclusions about scandium oxide as a high-k dielectric and its interface with Si.

Concerning interfacial layer, we have checked that nitrided silicon or deposited SiN_x have several advantages over chemical/native SiO_2: it has a higher dielectric constant than SiO_2 which reduces the EOT of the structure; the interface is better than high-k deposited on H-terminated silicon or chemical SiO_2 (the minimum of the D_{it} improves one order of magnitude); and lastly, it avoids O diffusion from the plasma that could oxidize Si surface. These advantages encourage us to continue with the study of silicon nitride as high-k/Si interface.

On top of that, we analyzed the use of ScO_x deposited by HPS as an alternative high-k gate dielectric and its compatibility with different substrates: Si, SiO_x, and SiN_x. ScO_x potentially fulfils some important requirements of flash memories applications as has been demonstrated in this ar-

TABLE I. Density of states D_{it} for different substrates obtained by the combined high-low frequency capacitance method and the conductance method.

Substrate	$D_{it,min}$ by $C_{QS}-C_{HF}$ method (eV^{-1} cm^{-2})	D_{it} by conductance method at 100 kHz (eV^{-1} cm^{-2})
Native SiO_2 on Si	1.9×10^{12}	7.4×10^{11}
HF-etched Si	1.2×10^{12}	6.7×10^{11}
600 s nitrided Si	4.2×10^{11}	2.6×10^{11}
30 s nitrided Si	1.6×10^{11}	6.7×10^{10}
30 s deposited SiN_x on Si	1.7×10^{11}	1.4×10^{11}

ticle. HPS deposited ScO_x films are polycrystalline with no preferential growth direction and its properties do not depend on the substrate. The dielectric constants of the films are around nine. Future work will be focused on optimizing deposition conditions in order to improve film characteristics and on depositing Sc-based ternary compounds by HPS, which have shown good dielectric constant and thermal stability with Si for gate dielectric applications.

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[1]K. H. Kim, D. B. Farmer, J. S. M. Lehn, P. V. Rao, and R. G. Gordona, Appl. Phys. Lett. **89**, 133512 (2006).
[2]K. A. Pestka II, J. D. Maynard, A. Soukiassian, X. X. Xi, D. G. Schlom, Y. Le Page, M. Bernhagen, P. Reiche, and R. Uecker, Appl. Phys. Lett. **92**, 111915 (2008).
[3]C. Adelmann, S. Van Elshocht, A. Franquet, T. Conard, O. Richard, H. Bender, P. Lehnen, and S. De Gendt, Appl. Phys. Lett. **92**, 112902 (2008).
[4]R. Thomas, P. Ehrhart, M. Luysberg, M. Boese, R. Waser, M. Roeckerath, E. Rije, J. Schubert, S. Van Elshocht, and M. Caymax, Appl. Phys. Lett. **89**, 232902 (2006).
[5]F. Liu and G. Duscher, Appl. Phys. Lett. **91**, 152906 (2007).
[6]J. A. Kittl, K. Opsomer, M. Popovici, N. Menou, B. Kaczer, X. P. Wang, C. Adelmann, M. A. Pawlak, K. Tomida, A. Rothschild, B. Govoreanu, R. Degraeve, M. Schaekers, M. Zahid, A. Delabie, J. Meersschaut, W. Polspoel, S. Clima, G. Pourtois, W. Knaepen, C. Detavernier, V. V. Afanas'ev, T. Blomberg, D. Pierreux, J. Swerts, P. Fischer, J. W. Maes, D. Manger, W. Vandervorst, T. Conard, A. Franquet, P. Favia, H. Bender, B. Brijs, S. Van Elshocht, M. Jurczak, J. Van Houdt, and D. J. Wouters, Microelectron. Eng. **86**, 1789 (2009).
[7]H. H. Tippins, J. Phys. Chem. Solids **27**, 1069 (1966).
[8]R. D. Shannon, J. Appl. Phys. **73**, 348 (1993).
[9]D. O. Klenov, L. F. Edge, D. G. Schlom, and S. Stemmer, Appl. Phys. Lett. **86**, 051901 (2005).
[10]S. Mori, Y. Y. Araki, M. Sato, H. Meguro, H. Tsunoda, E. Kamiya, K. Yoshikawa, N. Arai, and E. Sakagami, IEEE Trans. Electron Devices **43**, 47 (1996).
[11]H. M. An, Y. J. Seo, H. D. Kim, K. C. Kim, J. G. Kim, W. J. Cho, J. H. Koh, Y. M. Sung, and T. G. Kim, Thin Solid Films **517**, 5589 (2009).
[12]M. Houssa, L. Pantisano, L. A. Ragnarsson, R. Degraeve, T. Schram, G. Pourtois, S. De Gendt, G. Groeseneken, and M. M. Heyns, Mat. Sci. and Tech. R **51**, 37 (2006).
[13]M. M. Frank, S. Kim, S. L. Brown, J. Bruley, M. Copel, M. Hopstaken, M. Chudzik, and V. Narayanan, Microelectron. Eng. **86**, 1603 (2009).
[14]M. Putkonen, M. Nieminen, J. Niinistö, and L. Niinistö, Chem. Mater. **13**, 4701 (2001).
[15]M. A. Navacerrada, M. L. Lucía, and F. Sánchez-Quesada, Phys. Rev. B **61**, 6422 (2000).
[16]F. Laviano, L. Gozzelino, E. Mezzettia, P. Przyslupski, A. Tsarev, and A. Wisniewski, Appl. Phys. Lett. **86**, 152501 (2005).
[17]E. San Andrés, M. Toledano-Luque, A. del Prado, M. A. Navacerrada, I. Mártil, G. González-Díaz, W. Bohne, J. Röhrich, and E. Strub, J. Vac. Sci. Technol. A **23**, 1523 (2005).
[18]S. Dueñas, H. Castán, H. Garcia, E. San Andrés, M. Toledano-Luque, I. Mártil, G. González-Díaz, K. Kukli, T. Uustare, and J. Aarik, Semicond. Sci. Technol. **20**, 1044 (2005).
[19]M. Toledano-Luque, M. L. Lucía, A. del Prado, E. San Andrés, I. Mártil, and G. Gonzalez-Díaz, Appl. Phys. Lett. **91**, 191502 (2007).
[20]S. García, J. M. Martín, M. Fernández, I. Mártil, and G. González-Díaz, Philos. Mag. B **73**, 487 (1996).
[21]E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, USA, 1982).
[22]G. N. Parsons, J. H. Souk, and J. Batey, J. Appl. Phys. **70**, 1553 (1991).
[23]A. del Prado, E. San Andrés, I. Mártil, G. González-Díaz, D. Bravo, F. J. López, W. Bohne, J. Röhrich, B. Selle, and F. L. Martínez, J. Appl. Phys. **93**, 8930 (2003).
[24]A. Hardy, C. Adelmann, S. Van Elshocht, H. Van den Rul, M. K. Van Bael, S. De Gendt, M. D'Olieslaeger, M. Heyns, J. A. Kittl, and J. Mullens, Appl. Surf. Sci. **255**, 7812 (2009).
[25]N. T. McDevitt and W. L. Baun, Spectrochim. Acta **20**, 799 (1964).
[26]S. J. Schneider and J. L. Waring, J. Res. Natl. Bur. Stand., Sect. A **67A**, 19 (1963).
[27]M. Toledano-Luque, E. San Andrés, A. del Prado, I. Mártil, M. L. Lucía, G. González-Díaz, F. L. Martínez, W. Bohne, J. Röhrich, and E. Strub, J. Appl. Phys. **102**, 044106 (2007).
[28]M. Toledano-Luque, F. L. Marténez, E. San Andrés, A. del Prado, I. Mártil, G. González-Díaz, W. Bohne, J. Röhrich, and E. Strub, Vacuum **82**, 1391 (2008).
[29]M. Toledano-Luque, E. San Andrés, J. Olea, A. del Prado, I. Mártil, W. Bohne, J. Röhrich, and E. Strub, Mater. Sci. Semicond. Process. **9**, 1020 (2006).
[30]J. R. Hauser, CVC Version 5.0, © 2000 NCSU Software, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC.
[31]R. F. Pierret, *Field Effect Devices* (Prentice-Hall, Englewood Cliffs, NJ, 1990).
[32]E. San Andrés, A. del Prado, I. Mártil, G. González-Díaz, and F. L. Martinez, J. Vac. Sci. Technol. B **21**, 1306 (2003).
[33]H. Kim, P. C. Mchityre, C. O. Chui, K. C. Saraswat, and S. Stemmer, J. Appl. Phys. **96**, 3467 (2004).