Using Optimization Techniques to Characterize Irradiated CMOS Analog Switches

Y. Zong, F. J. Franco and J. A. Agapito

***Abstract*— The use of mathematical optimization techniques allows estimating the degradation of the internal components of irradiated CMOS analog switches from their nonlinear resistance and the value of leakage currents at different power supplies voltages.**

***Index Terms*— Analog switches, COTS, neutron effects, optimization, TID effects.**

I. INTRODUCTION

CMOS analog switches are nonlinear resistors whose value depends on a logic control input, on the power supplies value and the voltage at their edges [1]. They are widely used to connect or break circuits in such applications as multiplexing and function switching. Ideally, they have zero resistance when closed, infinite resistance when open, no leakage current and no parasitic capacitance. This paper will focus on Single Pole Single Throw (SPST) CMOS analog switches, with only one channel in each switch and only one logic control input.

The CMOS switches have several parts: A logic buffer, a level shifter and an analog channel (fig. 1). The buffer, to transform the primary logic input into hard logic values; the level shifter, to change the logic values into voltages more appropriated to bias the analog channel. This stage has a CMOS inverter to obtain the complementary value of the main output.

Finally, the analog channel is made with a couple of PMOS and NMOS transistors with the source and the drain terminal linked together. Taking the PMOS and NMOS in parallel is intended to minimize the non-linearity of the resistance value of the switches. The resistance of the N-channel increases with positive voltage and resistance of the P-channel increases with negative voltage. The resultant parallel combination exhibits the well known ¨crown¨ or twin –peak characteristic. Thus, the equivalent resistor R_{on} has a value that is independent enough on the applied voltage on the sides of the channel (fig. 2). In addition, R_{on} increases as the power supplies are reduced.

CMOS analog switches are also divided into two important families: High voltage switches and precision switches. The difference between them is the voltage applied to NMOS transistor bulk. In the first family, the bulk is connected to the negative power supply. E. g., fig. 1 belongs to this category. The main problem of this choice is the "substrate bias effect" [2] since the threshold voltage of the MOSFET depends on the difference between the source and bulk voltages.

Precision switches solve this problem using additional transistors in the analog channel (fig. 3). In case the NMOS transistor is ON, its bulk is shorted to the source of the switch and, on the contrary, if it is OFF, to the negative power supply. Thus, the NMOSFET threshold voltage does not change.

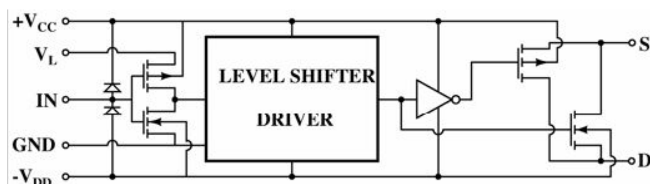

Fig. 1. Analog switches´ internal structure

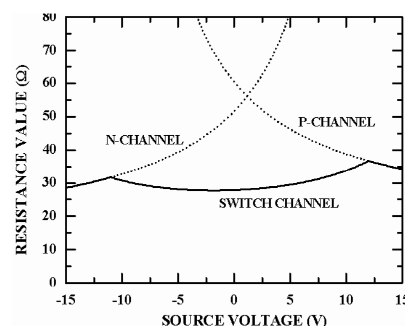

Fig. 2. The equivalent resistor converse the source voltage

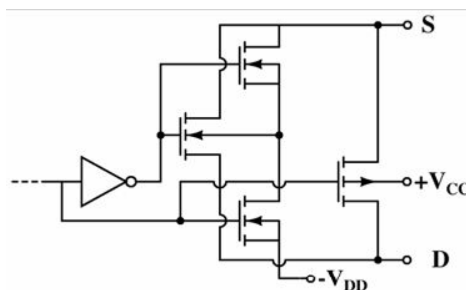

Fig. 3. Additional transistors in the analog channel in precision switches

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II. TESTED DEVICES AND RADIATION ENVIRONMENT

Six kinds of CMOS analog switches were selected to be irradiated in the neutron facility of the Portuguese Research Reactor (Lisbon, Portugal). The precision switches were ADG412, from Analog, DG412, from Vishay Siliconix, and MAX313 from Maxim. The tested high voltage switches were ADG212, from Analog, DG212, from Maxim, and DG212, from Vishay Siliconix. There are four switches in each device, which are normally open if the logic input is low. Also, all of them have a plastic DIP-14 package.

During the irradiation, the switches were biased with ±15 V power supplies and all the inputs joint to ground. In the neutron facility of the Portuguese Research Reactor [3], the switches received in a total neutron fluence between 4.3 & $6.4\cdot10^{13}$ $n\cdot cm^{-2}$, values that were reached after 60 h of irradiation. Moreover, the vestigial gamma radiation reached values between 1520-1700 Gy (air). The total radiation dose of each tested switch is shown in Table I.

TABLE I: TOTAL RADIATION DOSE OF THE TESTED SWITCHES

Tested Switch	**NIEL** $\cdot10^{13}$ $n\cdot cm^{-2}$	**TID** Gy (air)	**D.R.** Gy (air)/h
ADG212	6.39	1720	28.7
ADG412	6.39	1720	28.7
DG212(Maxim)	4.3	1520	25.3
MAX313	4.3	1520	25.3
DG212(Vishay)	5.61	1660	27.7
DG412(Vishay)	5.61	1660	27.7

II. PHYSICAL BEHAVIOR OF CMOS ANALOG SWITCHES

A. MOSFET as nonlinear resistors

According to [2], the current that flows along a NMOS transistor is:

$$I_{DS} = \begin{cases} 0, & V_{GS} < V_{TH} \\ \beta\cdot\left[2(V_{GS}-V_{TH})\cdot V_{DS}-V_{DS}^2\right]\cdot(1+\lambda\cdot V_{DS}) & V_{DS} < V_{GS}-V_{TH} \\ \beta\cdot(V_{GS}-V_{TH})^2\cdot(1+\lambda\cdot V_{DS}) & V_{DS} > V_{GS}-V_{TH} \end{cases} \quad (1)$$

With $V_{TH} = V_{T0} + \gamma\cdot(\sqrt{\phi_B + V_{SB}} - \sqrt{\phi_B})$. β is the transconductance of the transistor, λ is the factor of channel length modulation, V_{TH} is the threshold voltage, V_{SB} is the bulk bias voltage, V_{T0} is V_{TH} for $V_{SB}=0$, Φ_B is the surface inversion potential and γ the body effect coefficient. In the case of the PMOS transistors, the set of equations are symmetric. This is the simplest way to describe a MOSFET. However, more accurate models can be found in the literature and could be used instead of Eq. (1).

The equivalent conductance of an ideal NMOS transistor can be written as:

$$G_{DS} \cong \begin{cases} 0, & V_{GS} < V_{TH} \\ \beta\cdot\left[2(V_{GS}-V_{TH})-V_{DS}\right] & V_{DS} < V_{GS}-V_{TH} \\ \beta\cdot(V_{GS}-V_{TH})^2/V_{DS} & V_{DS} > V_{GS}-V_{TH} \end{cases} \quad (2)$$

The gate voltage of the analog channel transistors are the source voltage values, $+V_{CC}$ & $-V_{DD}$. Also, the dependence of the threshold voltage on the bulk bias voltage must be taken into account. In addition, there are parasitic resistors in the transistors and in the channel that must be incorporated to the device. Eq. (2) is the simplest equation to describe a MOSFET.

B. Effects of radiation on analog switches.

Due to the use of CMOS technology, analog switches are very sensitive to ionizing damage [4]. The main predicted effects are the shift of threshold voltages and the appearance of leakage currents among previously isolated n-zones of the device. The origin of these currents is the accumulation of positive charges in the epitaxial isolated and can be modeled as N-transistors without a gate pin.

In spite of the fact that CMOS devices are very neutron tolerant, the effect of this radiation in the analog switches must be regarded. The reason is that the displacement damage leads to a reduction of the transconductance value and an increase of parasitic resistances [5].

III. MODELING OF SWITCHES IN MATLAB

A. Measuring the actual resistance of the switches

Before and after the irradiation, the switches were connected in series to a resistor R_L with a value at least ten times higher than it and a current source sent a current when a PC system commands (Fig. 4). Thus, a voltage sweep between the values of the power supplies was done. A multimeter measured the voltages of the source and the drain of the channel and saved them into a text file. The value of the current was recorded as well. This process was repeated with several different power supplies (±10V, ±15V, 0-10V, 0-15V).

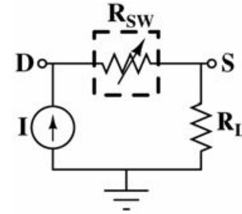

Fig. 4. The measuring circuit

B. Mathematical models of analog switches

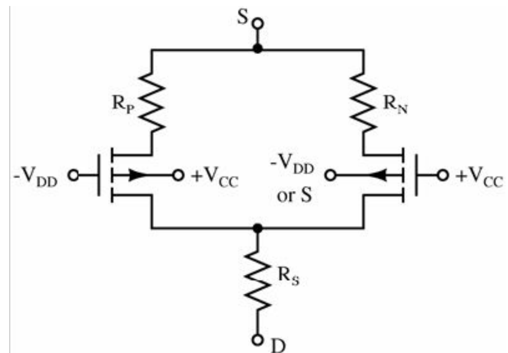

Fig. 5. The channel of an analog switch

Fig. 5 shows the schema of the channel of an analog switch. This device can be converted into a MATLAB function with the following input data: First, there is a set of bias voltages, (V_S, V_D, $+V_{CC}$, $-V_{DD}$), and, second, the physical characteristics of the devices (Value of MOSFET threshold voltages, trans-conductances, parasitic resistors…). Thus, we can determine the current that flows along an analog switch according to the bias voltages and calculate the value of the equivalent resistor as a function of the source voltage V_S.

The main problem of the model of fig. 5 is that it fails if there are leakage currents in the MOSFETs. Independently on the nature of the leakage currents, it can be measured as the difference between the current supplied by the power source and that goes along R_L. According to the relationship between the leakage current and the switch source voltage, which will be depicted later, that current is similar to one or two parasitic NMOS transistors, with their sources in the negative power supply and their drains in the sides of the analog channel (fig. 6). This model can also be converted into a MATLAB function and must be used instead of fig. 5 if there are leakage currents.

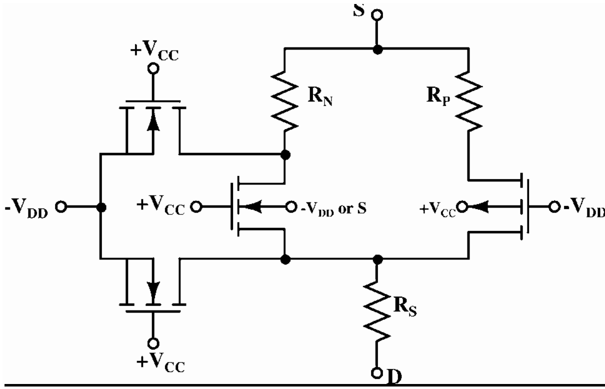

Fig. 6. Modified model of fig.5 with leakage currents parasitic transistor. In fact, parasitic transistors do not have a gate pin. Therefore, we chose an arbitrary value ($+V_{CC}$) to use eq. 1 in the MATLAB model.

IV. THE OPTIMIZATION PROCESS

A. The optimization techniques

As described in section III, analog switches have non-linear behavior. The determination of the coefficients of the established models (fig. 5-6) is accomplished by solving a nonlinear least squares problem with bounds constrains. The purpose is to fit the experimental data to a mathematical function by varying parameters in the function. A specific functional form $E(x, z)$ has been selected from theoretical model. The independent variables are the elements of z_i, e.g., the voltages in the sides of the channel of the analog switch. On the other hand, x is a vector of the parameters to be adjusted [β_{NMOS}, $V_{T0}NMOS$, R_{NMOS}, etc.] until the best fit of E to the experimental data is found.

$$\chi^2(x) = \sum_{i=1}^{m} \left[E(x, z_i) - y_i\right]^2 \qquad i = 1, \ldots\ldots m \qquad (3)$$

The objective function $\chi^2(x)$ to be minimized is the squares of the difference between the theoretical data $E(x, z_i)$ and the experimental data y_i (resistance, conductance or the leakage current). Usually, the Gauss-Newton method and the Levenberg-Marquard method are used to solve the non-linear squares optimization.

The following eq. (4)-(5) define the Gauss-Newton method, where J_k is the Jacobian matrix. As far as the generation of descent directions goes, eq. (4) is likely to be less troublesome than the corresponding one for Newton method [6]. Since the matrix $J_k^T J_k$ is always at least positive semi-definite. The only trouble that can arise in this respect is when $J_k^T J_k$ is rank deficient and hence J_k is singular. However, even if p_k is descent direction this does not guarantee that $f_{k+1} < f_k$. Eq. (4) might be too large, locating x_{k+1} at a point that would surpass the linear minimum and could not converge globally. For these reasons a good starting point is required if there is to be any chance of convergence to a minimum. So the Gauss-Newton method exist some drawbacks of rigid condition and local convergence.

$$x_{k+1} = x_k + p_k \qquad (4)$$

$$J_k^T J_k p_k = -J_k^T f_k \qquad (5)$$

$$(J_k^T J_k + \mu_k I) p_k = -J_k^T f_k \qquad (6)$$

The Levenberg-Marquard method incorporates a technique for dealing with problems related to singularity in matrix $J_k^T J_k$. The Eq.5 is modified to equation 6, where $\mu_k \geq 0$ is a scalar and I is the unit matrix. Then the Eq. (4) is used to attain a point which to begin the next iteration. For a sufficiently large value of μ_k, the matrix $J_k^T J_k + \mu_k I$ is positive definite and p_k is the descent direction. When $\mu_k=0$, p_k is the Gauss-Newton vector. As $\mu_k \rightarrow \infty$, the effect of term $\mu_k I$ increasingly dominates that of $J_k^T J_k$ so that $p_k \rightarrow -\mu^{-1}_k J_k^T f_k$ which represents an infinitesimal step in the steepest descent direction. Since the Levenberg-Marquard method is a compromise between the Gauss-Newton method and the steepest descent method, combing the best features, eschewing the disadvantages between them, we choose the Levenberg-Marquard method to optimize those parameters in the model of fig.5and fig. 6.By appropriately choose μ_k we can make the method converge globally and have a quick convergence rate.

B. Adjusting the parameters

Using MATLAB Optimization Toolbox, we can make an optimization program. First of all, some physical characteristics should be taken into account E.g., the value of β is always positive; the threshold voltage has a positive value for an NMOS transistor, while it is negative for a normal PMOS transistor etc. Actually, we should define a set of lower and upper bounds on the parameters, which are designed to be adjusted. At the same time, the tolerance on the objective function and maximum number of iterations allowed should be given at initial.

Secondly, some M-functions were used to calculate the parameters of the function of interest. In our study, we try to fit our data to the switch conductance using the model of fig. 5 and when we calculate the leakage current, using the sum of the current of two parasitic NMOS transistors of fig.6.

Finally, the program calls an optimization algorithm that

compares the values of the measured data to the theoretical ones and changes the value of the x-vector with the purpose of minimizing the value of χ^2. Thus, we can obtain the most suitable values of the parameters β, V_{TH}, λ, R, etc. for the actual measured data. The program diagram is shown in fig. 7.

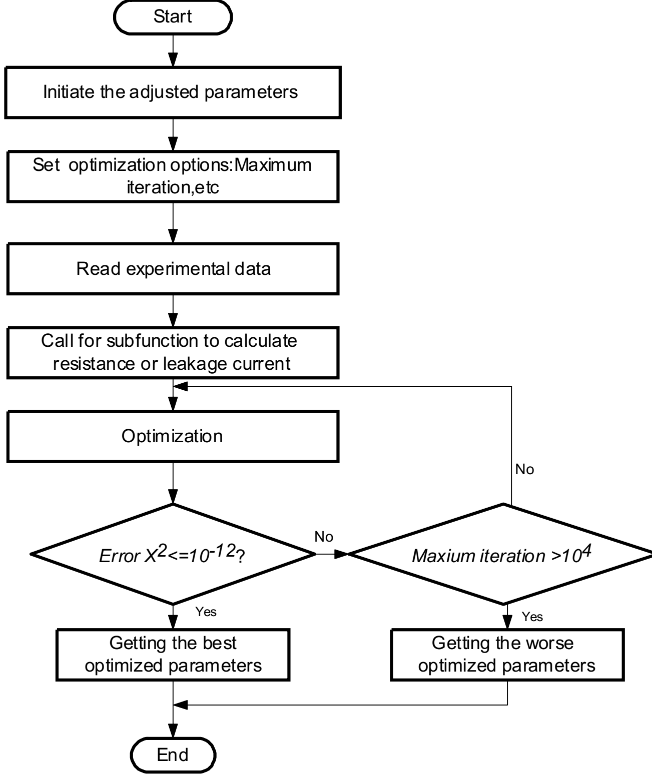

Fig.7. The optimization program diagram

V. RESULTS

A. *Results from the conductance model.*

The first problem that we tried to solve was to find out the appropriate values for the internal parameters of an analog switch. The use of the optimization techniques described in the previous section allows solving this problem. We had four different switches to be tested for each device. Using the experimental data taken before and after the irradiation, we can get the optimized parameters for each device. Table II shows the calculated values in an ADG212 from the data taken before the irradiation. As we will see, some parameters can be easily fitted and the results are coherent with the theoretical predictions. However, the results of the fitting process are not as trustworthy in other parameters. Fig. 8 shows the resistance of non-irradiated ADG212 switch with different power supplies.

Table III corresponds to the fitting of data of switch ADG212 after the irradiation. Fig. 9 shows the actual resistance values of an irradiated ADG212 and the theoretical values calculated from the adjusted parameters in the model of fig. 5. The power supplies are ±10V and ±15V. Fig. 10 shows the resistances of an irradiated ADG212 switch with different power supplies.

TABLE II: PARAMETERS OF NON-IRRADIATED ADG212

Supply	β NMOS	V_{T0} NMOS	R_{NMOS}	$R_{CONT.}$
0-10 V	9.75E-04	3.72E+00	1.35E+01	2.38E-04
0-15 V	9.64E-04	1.66E+00	3.64E+01	2.22E-14
±10 V	9.99E-04	2.82E+00	1.89E+01	2.22E-14
±15 V	8.72E-04	5.00E+00	3.29E+01	1.54E+00
Supply	**β PMOS**	**V_{T0} PMOS**	**R_{PMOS}**	**χ^2**
0-10 V	1.24E-03	-1.65E+00	2.59E+01	2.98E-06
0-15 V	1.12E-03	-7.04E-01	2.72E+01	1.48E-06
±10 V	8.50E-04	-1.06E+00	1.19E+01	1.43E-06
±15 V	7.26E-04	-7.76E-01	1.64E+01	4.04E-06

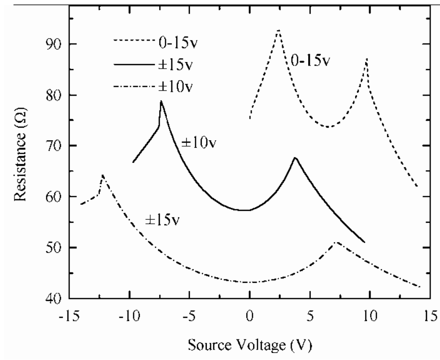

Fig. 8. The resistance of non-irradiated ADG212 with different power supplies

TABLE III: THE OPTIMIZED PARAMETERS OF IRRADIATED ADG212 ACCORDING TO THE MODEL OF FIG. 5

Supply	β NMOS	V_{T0} NMOS	R_{NMOS}	$R_{CONT.}$
0-10 V	5.37E-04	2.49E-00	1.97E+01	5.46E+00
0-15 V	5.63E-04	8.09E-04	2.15E+01	5.11E-02
±10 V	7.62E-04	3.55E+00	4.05E+01	2.20E+00
±15 V	5.16E-04	2.02E+00	3.79E+01	2.22E-14
Supply	**β PMOS**	**V_{T0} PMOS**	**R_{PMOS}**	**χ^2**
0-10 V	7.74E-04	-3.51E+00	5.34E-01	1.02E-05
0-15 V	8.90E-04	-3.91E+00	3.14E+01	9.87E-06
±10 V	8.06E-04	-4.73E+00	2.41E+01	2.14E-06
±15 V	5.73E-04	-2.74E-01	2.43E+01	6.49E-07

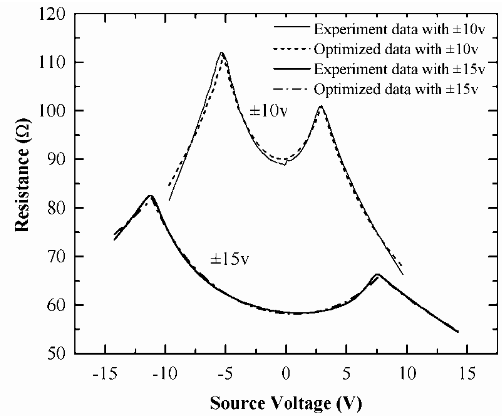

Fig. 9. Theoretical and actual resistance of an irradiated ADG212 with power supplies ±10v and ±15v

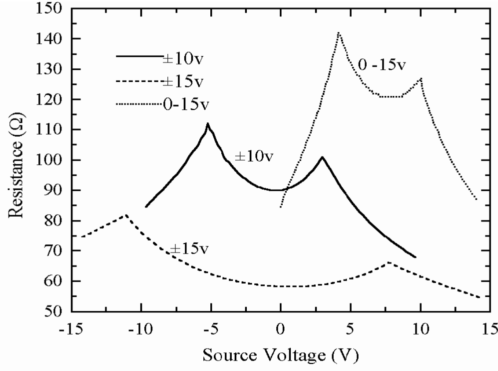

Fig. 10. The resistances of the irradiated ADG212 with different power supplies

Among these adjusted parameters for ADG212, β_{NMOS}, β_{PMOS} could be optimized very well at different power supplies for anyone device. However, the parameter $V_{T0}NMOS$ sometimes shows negative values with some power supplies, even though, in other cases, the calculated values for the same parameter are negative. Besides, the value of $V_{T0}PMOS$ converges to a positive value, an unexpected and forbidden result. This deviant phenomenon always happened, when the power supply was unipolar. In addition, the model failed to estimate the ADG212 with unipolar 10V power supply, representing in the value of R_{PMOS}, which was very less than that with other power supplies.

As regards DG212 (Vishay), fig. 11 shows its resistances with different power supplies after irradiation and the adjusted irradiated parameters are shown in Table IV. We found that the optimized data brought about better result with bipolar 15V power supply than that with bipolar 10V. When the power supply was unipolar 15V, the experimental data could not fit well the to this conductance model. The most difference among those parameters was exhibited by the parameter R_{NMOS}. At the same time, this model could not succeed in predicting the behavior for DG212 (Maxim) with unipolar 15V power supply. This fact can be attributed to a local convergence at a point banned by physical laws (A positive value of $V_{T0}PMOS$).

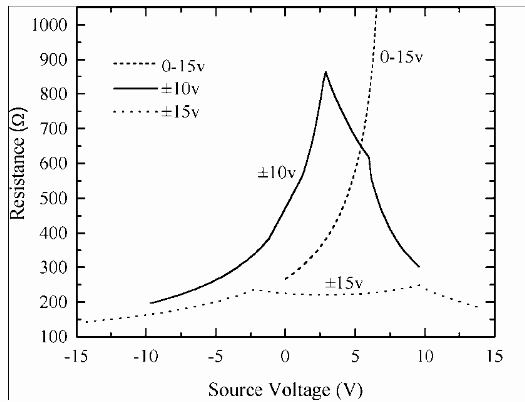

Fig. 11. The resistances of the irradiated DG212 (Vishay) with different power supplies

TABLE IV: THE OPTIMIZED PARAMETERS OF IRRADIATED DG212 ACCORDING TO THE MODEL OF FIG. 5

Supply	β NMOS	V_{T0} NMOS	R_{NMOS}	$R_{CONT.}$
0-15 V	2.08E-04	5.21E+00	7.56E+00	9.19E+00
±10 V	2.01E-04	4.46E+00	1.29E+01	1.32E+01
±15 V	2.19E-04	5.06E+00	4.18E+01	6.47E+00
Supply	**β PMOS**	**V_{T0} PMOS**	**R_{PMOS}**	**χ^2**
0-15 V	1.30E-04	-7.84E+00	4.24E+01	3.08E-06
±10 V	1.81E-04	-9.55E+00	6.80E-12	5.33E-07
±15 V	1.51E-04	-5.39E+00	2.79E+01	3.69E-08

According to the optimized data, for the high voltage family switch, we found that after irradiation, firstly, whatever the bipolar or unipolar power supplies are, the higher the power supply, the better the optimized parameters (see fig. 8). Secondly, when the device was supplied with bipolar power supplies, its optimized data were better than the one with unipolar power supply (see Table III and IV). Finally, it was obviously found that the parameters *β,* $V_{T0}NMOS$ decreased, while the power supplies increased, except the switch DG212 (Vishay).

For the precision switches, we found that the parameter Φ_B of NMOS always was 1.00E-01 with our optimization program, whatever the switches were and with whatever power supplies. It is attributed to the fact that the precision switches are fabricated with its bulk shorted to the source of the switch (see part I.).Thus, the parameter V_{SB} is zero and the formula of threshold voltage (see part II.) does not include the item Φ_B. So it is not an internal parameter to be optimized.

Among the tested precision switches, only DG412 (Vishay) with bipolar 15V power supplies, could fit the model well. The other like ADG412, MAX313 could not fit the conductance model (fig. 5). The reason is that there is leakage current in them, which is related to total ionizing dose (TID). Therefore, we have to turn to other model, e.g. fig. 6.

In addition, comparing fig. 7 and fig. 9, first of all, we observed that the switch resistance increased after the irradiation. This is a consequence of the displacement damage and the evolution of the threshold voltage. On the other hand, the switch resistance decreased with the power supply increased not only before the irradiation, but also after the irradiation (see fig. 7-10).

B. *Results from the leakage current model.*

Since there is leakage current in the switches like ADG412, DG212 (Maxim) and MAX313, we used them to test that the leakage current model was valid or not.

As we previously said, the current is similar to that of an NMOS transistor with its source in the negative power supply and its drain in the analog switch input channel. However, there are some physical reasons that advise the use of a couple of parasitic transistors instead of only one, as fig. 6 shows.

We consider that there is no significant leakage current to be taken into account before irradiation. The optimization tools allow fitting this set of data to the sum of the currents of a

couple of NMOS transistors that follow eq.1. Table V shows the parameters obtained from the optimization study for ADG412. Fig. 12 compares the actual leakage current and the theoretical current sum values of two parasitic NMOS transistor, with power supply ±15V for ADG412. Using the optimized parameters, we could obtain the theoretical leakage current values. Fig. 13 is the theoretical leakage current in an ADG412 analog switch after the irradiation.

TABLE V: PARAMETERS OF THE PARASITIC TRANSISTORS OF AN IRRADIATED ADG412 ANALOG SWITCH.

Supply	β_1(mA·V^{-2})	V_{t1}	λ1	χ^2
0-10 V	8.54E-02	1.21E+01	4.12E-03	1.13E-03
±10 V	4.29E-02	1.43E+01	2.96E-03	6.86E-03
±15 V	2.54E-01	2.94E+01	7.28E-02	9.17E-02
Supply	**β_2(mA·V^{-2})**	**V_{t2}**	**λ2**	
0-10 V	2.40E-14	1.41E+01	2.25E-01	
±10 V	7.94E-03	9.54E+00	2.22E-14	
±15 V	4.05E-02	2.27E+01	2.22E-14	

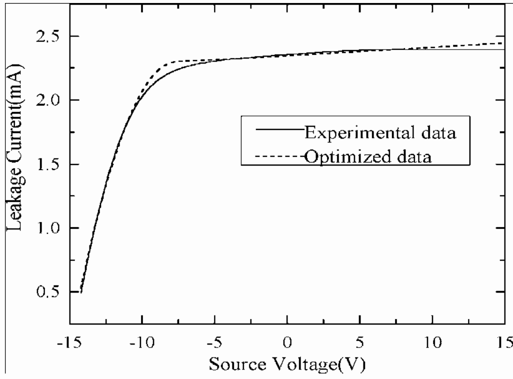

Fig. 12. Theoretical and actual leakage currents of an irradiated ADG412, using the sum of the current of two parasitic NMOS transistor of fig.6

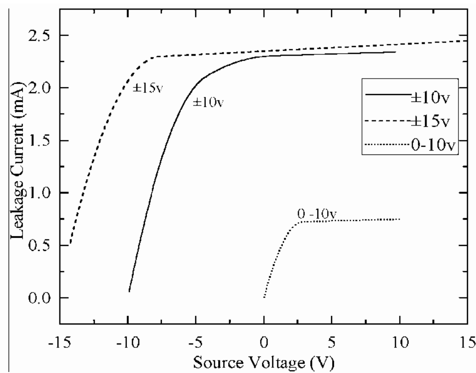

Fig. 13. The theoretical leakage currents of ADG412 with different power supplies after the irradiation

DG212 (Maxim) and MAX313 with bipolar 10V and 15V power supplies could fit the leakage current model. Fig.14 shows the actual and the theoretical leakage current of DG212 (Maxim) and MAX313 with bipolar 15V power supply. We found that MAX313 was more adaptable to the leakage current model than DG212 (Maxim). Fig.15 shows the theoretical and actual leakage current of MAX313 with bipolar 15V and 10V power supplies. We also observed that the fit result of bipolar 15V was better than that of bipolar 10V.

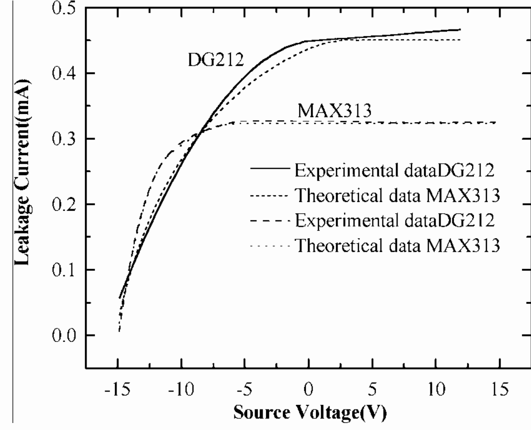

Fig.14. The actual and the theoretical leakage current of DG212 (Maxim) and MAX313 with bipolar 15V power supply

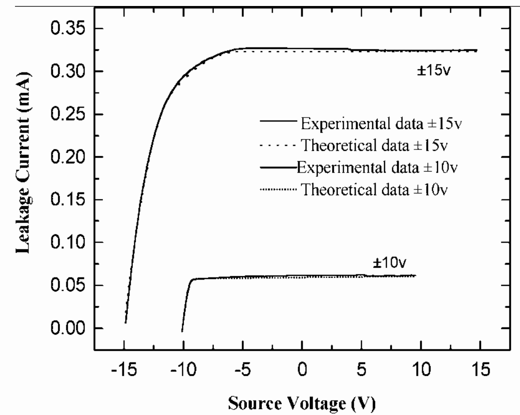

Fig. 15. The leakage currents of MAX313 with different power supplies

Using the KCL or KVL equations of the circuit, further work was done to calculate the switch resistance of the leakage current model (fig. 6). We found that the actual resistances could not fit the model, because there were large leakage currents. It was difficult to obtain the minimum error for our optimization program.

VI. DISCUSSION

A. Dependence on the power supplies

The above results clearly demonstrate that most of the optimized parameters can accurately fit the experimental data according to the models (fig. 5 & 6) with bipolar power supplies. Also, we note that the optimized result with bipolar 15V power supplies is better than that with bipolar 10V power supplies. According to the eq. (2), we consider that the established model becomes more accurate, if the power supplies have a wide range of value. With unipolar power supply, de-

spite having ideal tolerance error between the theoretic and actual data at the optimization process, this leads some parameters, as $V_{T0}PMOS$, appear to be positive, what is not permitted. The possible reason is related to the limitation for the number of iteration in the optimization program.

B. *Comparing results in the same chip*

Our simulation is based on four different switches in the same kind chip. It is observed that although these four switches belong to the same kind, the optimized data for each device still exist some differences. One cause is that the same factory can not produce all their chips equally in the fabricate process. The other reason perhaps is that our optimization program adjusted the same parameter with different step in order to make the optimization algorithm converge to the minimum error.

C. *Dependence on the initial optimization conditions*

During the optimization process, it should be noted that the initial conditions are very important to the optimized result. For example, the range of value of parameters β, V_{TH}, λ, R, etc, if they were given an adapt range of value; we can obtain the result quickly. For certain parameters, they need to be calculated for so many times that the algorithm converges. The possible effect of this can be related to the optimization algorithm, as described in part V.

D. *Parameters hard to calculate*

According to the results from the established models, parameters like λ and β could be obtained easily, while the parameter V_{TH} is difficult to be calculated. It is unstable, whose value depends vitally on the initial optimization conditions.

VII. CONCLUSIONS

From a hardness-assurance point of view, it is very important to estimate as accurately as possible the degradation of an irradiated device. The present paper based on a large set of irradiation data for different CMOS analog switches. We have taken advantage of optimization technique to accurate predict their degradation. This method can be used to estimate the degradation of other commercial devices.

We found that if leakage current did not appear in the switch, like ADG212, DG212 (Vishay), these switches could fit well the conductance model (Fig. 5). Using this model, we could characterize well their internal components behavior after the irradiation, especially with bipolar power supply. At the same time, the higher the power supply, the more accurate the prediction.

The results in Table II and III show that the reasons of the degradation of the analog switches are those predicted by radiation damage theories:

> Optimization techniques discover that the values of the transconductances β have decreased and the value of parasitic resistances are larger. These phenomena are attributed to displacement damage effect.
>
> Moreover, there is a clear shift of the threshold voltage of the internal MOS transistors, caused by the TID damage. The scattering of this parameter is large, because of the influence of bulk effect and the large number of parameters (Eq. 1) needed to calculate the threshold voltage.

In addition, if there were leakage currents in switches, as ADG412, MAX313and DG212 (Maxim), optimization techniques showed that the leakage currents could be modeled like a couple of NMOS transistors.

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