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Inactivity Windows in Irradiated CMOS Analog Switches

F. J. Franco, Y. Zong and J. A. Agapito

***Abstract*— AbstractRadiation tests have shown the existence of inactivity windows in analog switches. It means that the devices lose their ability to switch between ON and OFF states if the total radiation dose is placed between two characteristic values. Once the total ra- diation dose goes beyond the top value of the window, the switching ability reappears. A physical mechanism based on the evolution of the threshold voltage of irradiated NMOS transistors is proposed in this paper. Finally, consequences of inactivity windows in the conception of radiation tests are discussed.**

***Index Terms*— Analog switches, complementary metaloxide semiconductor (CMOS) devices, total ionizing dose (TID).**

I. Introduction

THE development of the new accelerator LHC (Large Hadron Collider), being nowadays built in the European Center for the Nuclear Research (CERN), which has the purpose of replacing the ancient electron-positron accelerator, LEB, has caused the rising of a great deal of technological challenges. One of the main research lines of the preliminary investigation is the selection of rad-tol electronic devices. In fact, all the elements around the particle beams will be exposed to radiation so they are liable to undergo a degradation that might commit the reliability of the system. The radiation is expected to be significant several meters far away from the particle beam. In particular, at the instrumentation system devoted to control the temperature of the cold mass, which keeps several powerful electromagnets in superconducting state so that the particle beam could be confined in 27-km circumference tunnel.

Computer simulations show that the radiation will consist of neutral particle, mainly neutrons and a small fraction of pions, and gamma radiation [1]. In general, charged particles are expected only in very few points, as magnet gaps, since they will be swept away by the powerful electromagnetic fields. For a period of 10 years of the LHC activity, the instrumentation might face a total radiation dose (TRD) on the order of $5{\cdot}10^{13}$ n$\cdot$cm^{-2} and several hundreds of Gy (Si) of ionizing radiation.

In order to simulate the LHC radiation environment, a specially devoted neutron facility was built in the Portuguese Research Reactor, fully described in other previous works [2], [3]. The tests were scheduled to be performed in five sessions of 12 hours, followed by 12 h-intervals of technical shutdown. Thus, 60-h radiation tests were carried out. The neutron fluence was measured with ^{58}Ni foils and the neutron energy spectrum was that of the ^{235}U after removing the thermal neutrons, similar to the expected in the LHC cryogenic system. Some calculations have shown that the damage factor is 1.28 [3]. In other words, despite all the neutron fluence values are those directly measured from the nickel foils, they can be immediately expressed in standard 1-MeV neutron/cm^2 multiplying the value of the neutron fluence by 1.28. Besides, due to the dependence on the dose rate of the damage caused by the ionizing radiation [4], the neutron facility was trimmed so that the vestigial gamma dose should be about 5 times the one expected in the LHC, as standard protocol tests recommend [5]. This is the reason why the total ionizing dose values were between 1.5 & 2.0 kGy (Si) instead of only several hundreds of Gy (Si).

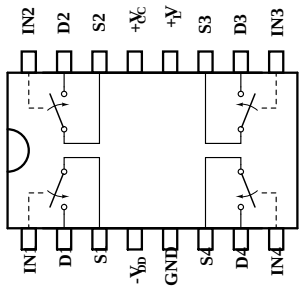

Fig. 1. Internal layout of a typical 4xNO SPST analog switch.

During the first stage of the development of the cryogenic system, the necessity of using 4NOxSPST (Single Pole Single Throw) analog switches arose, so radiation tests on this kind of devices were scheduled. In a few words, an SPST analog switch is a resistor whose value depends mainly on a control logic input, which sets the state of the analog switch (open & close). If the switch is in open state, the value of the resistance can be supposed infinite, but on the contrary, if it is closed, the resistance value is very low (1-200 Ω). The 4xNO symbol means that there are four switches in each chip and that they are *Normally Open* with low logic input. To clear up this definition, Fig. 1 shows the typical internal layout of this kind of devices, as it is found in this kind of devices and, in particular, in all the irradiated devices.

Previous works [6], [7], also related to these tests, showed that, after the irradiation, these devices had suffered an in-

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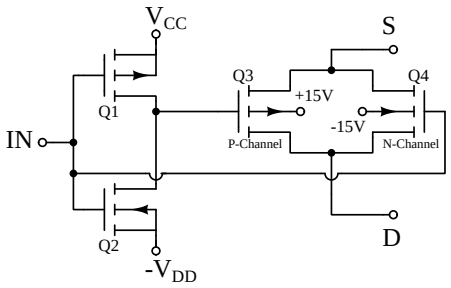

Fig. 2. Simplified structure of the analog channel.

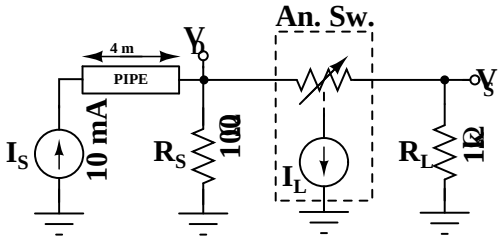

Fig. 3. Network to measure the values of the series resistance and the leakage current of the analog switch.

crease of the series resistance because of displacement damage and of the shift of the threshold voltage of the internal MOS transistors; also, there was evidence of the appearance of leakage currents from the analog channel to the negative power supply and, finally, an increase of the value of the minimum power supply value as well as a shift in the switching threshold voltage and hysteresis. However, these results were obtained from an off-line tests whereas the results reported in this paper were obtained during the irradiation. This continuous tracking of the values of the main parameters allowed to discover the existence of a physical phenomenon that, otherwise, could not have been reported. These phenomena was the appearance of inactivity windows in the irradiated CMOS devices.

II. First signs of inactivity windows

In a preliminary campaign, two samples of DG412 from Maxim were tested. Like most of the analog switches, this device is built in *bluk* CMOS technology. Usually, a single CMOS switch consists of an N-channel and a P-channel MOSFET transistors in parallel (Fig. 2). The respective drains and sources of the two transistors are connected to both terminals of the analog channel, *D & S*, while the gates of the two transistors are driven by a digital network. The output voltage values of this network are equal to the power supply voltages, V_{CC} and $-V_{DD}$, which controls the transition from ON to OFF state and vice versa. These voltage values are obtained from typical logic values (e.g., 0 &5 V) with logic level shifters that will be later described. the N-channel transistor is ON for positive gate-to-source voltage and OFF for negative gate-to-source voltages (vice versa for the P-channel transistor). The use of a pair of MOSFET guarantees that the resistance value is hardly dependent on the voltage of the channel edges [8].

During the irradiation, the samples were biased with $\pm$15V power supplies and with a logic supply, V_L, of +5V, characteristic of a TTL-compatible logic. By means of the system sketched in Fig. 3, resistances of the switch and leakage currents were measured every few minutes during the radiation and their values saved by a PC controlled system. The system worked as follows: First of all, an accurate current source, I_S, outside the facility and, thus, immune to the radiation effects, sent a current of 10 mA to a resistor of 100 Ω, R_S, placed on the test board. We preferred to use a current input source instead of a voltage one because of the distance between the devices and the measuring system, as it is encouraged in the design of instrumentation systems [9]. In parallel to R_S, there was another branch consisting of the analog switch and a load resistor, R_L. It is easy to prove that, in this situation, most of the current flows along R_S and a stable voltage value about 0.9 V is guaranteed. Finally, an accurate voltmeter, controlled by the computer and not affected at all by any kind of ground loops, measured the values of V_D and V_S. It must be reported that, once the characterization had ended, some mechanical relays, absent from Fig. 3, isolated the switch from the input current source and connected it to ground until the loop restarted. In fact, the full characterization of a chip took about 10 s, being performed every 12 minutes.

The series resistance of the switch can be immediately deduced from the values of V_D and V_S along with the resistor R_L. Also, in case leakage currents (I_L) appear, they can be detected since a discrepancy between the values of the input current, I_S, and the sum of the currents flowing along R_S and R_L comes out.

Let us focus now on the behavior of the series resistance of the irradiated switches. Fig. 4 shows the evolution of this parameter during the irradiation. According to the graph, the series resistance value increases during the irradiation, this phenomenon being related either to the Si-resistivity growth, associated with displacement damage, or with the shift of MOSFET threshold voltage, caused by TID damage [6]. The most interesting detail of the graph is that the switch stops working when the total radiation dose (TRD) was $2.25{\cdot}10^{13}$ n$\cdot$cm^{-2} & 700 Gy. In other words, whatever the logic input was, the switch was in OFF state, showing an infinite resistance value. Nevertheless, when the TRD value reached a value of $3.0{\cdot}10^{13}$ n$\cdot$cm^{-2} & 900 Gy, the device recovered the switching function and did not lose it until the end of the irradiation. As a consequence of this phenomenon, all the lines plotted in Fig. 4 show a gap between two values of TRD, which corresponds to an inactivity window in this device.

This strange and unexpected recovery happened during the irradiation, while the devices were irradiated, and not during the technical shutdowns of the reactor. Therefore, it must not be attributed to the annealing of the semiconductor lattice but to other phenomena. Finally, it must be remarked that, in spite of the fact that the device had recovered the ability to switch, by no means it could be thought as radiation tolerant. The reason is that the leakage currents were on the order of 2 mA, making the device useless for any actual electronic system.

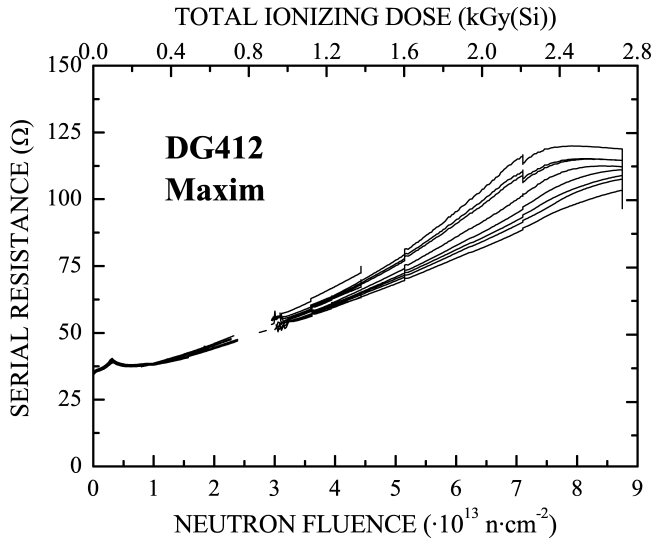

Fig. 4. Shift of the DG412 series resistance during the irradiation. Each line is related to one of the four switches present in each device.

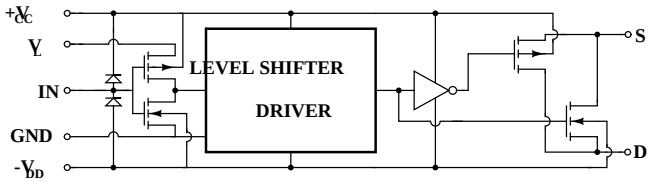

Fig. 5. High voltage switch, with logical control network

III. A DEEPER STUDY OF INACTIVITY WINDOWS

In the following campaign, different types of switches from several companies were tested to obtain more information about this strange phenomenon and, obviously, to carry out the selection of a suitable device for the LHC electronic instrumentation. CMOS analog switches are divided into two large groups: *High voltage* and *precision* families, regarding the node to which the bulk of the NMOS transistors of the analog channel is connected (Fig. 5-6). In high voltage switches, it is shorted to $-V_{DD}$ whereas, in the other family, a couple of NMOS transistors chooses the node between $-V_{DD}$ and the source of the switch, *S*, depending on the logic state. Thus, precision switches avoid the influence of the bulk voltage on the NMOS threshold voltage, resulting a very low and constant resistance value, which cannot be achieved in the samples of the other family.

Tested precision switches were ADG412, from Analog Devices, DG412 from Vishay-Siliconix and MAX313, from Maxim. The high voltage switches were ADG212, from Analog Devices, DG212 from Vishay and DG212 & MAX332 from Maxim. More data about these devices can be found on the manufacturers website [10], [12], one sample of each type being irradiated in this new campaign. The test set-up had slightly changed from the first one. First of all, samples were tested while biased with $\pm 15V$ and $V_L = 15V$. The reason of using these voltage values was that, after the first irradiation, the higher the power supplies values, the better the irradiated DG412 samples worked. Like in the first experience, the PC

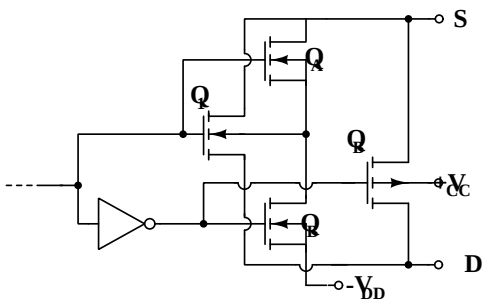

Fig. 6. Analog channel of a precision analog switch. The core of the analog chanel is Q_1 & Q_3. When the switch is ON, the gate voltage in Q_1 is $+V_{CC}$ and, in consequence, Q_Q is closed whereas Q_B is open. Thus, the bulk of Q_1 is joined to S. On the contrary, when the switch is OFF, the gate voltage of Q_1 us $-V_{DD}$ and, in this case, Q_B is closed instead of Q_B, joining Q_1 bulk to $-V_{DD}$. The Q_2 bukk is not controled.

based system measured the resistance and the leakage currents. However, unlike the first experiment, the logic input was not constant since the computer did a DC sweep from 0 to 15 V, with a step of 1 V, measuring the series resistance at all the values of the logic input voltage. When the system was not characterizing the switch, an array of mechanical relays joined all its inputs to ground.

In the neutron facility of the Portuguese Research Reactor, these switches received a total neutron fluence between 4.3 & $6.4{\cdot}10^{13}$ n·cm^{-2}, values that were reached after 60 h of irradiation. Moreover, the vestigial gamma radiation reached values between 1520-1700 Gy (Si) (Dose rate: 25.3-28.3 Gy/h). The total radiation dose of each tested switch is shown in Table I.

TABLE I
TOTAL RADIATION DOSE OF THE TESTED SWITCHES

Tested devices	N. Fluence ($\cdot 10^{13}$ n·cm^{-2})	TID Gy(Si)	D.R. Gy/s
ADG212	6.39	1720	28.7
ADG412	6.39	1720	28.7
DG212 (Vis)	5.61	1660	27.7
DG412 (Vis)	5.61	1660	27.7
DG212 (Max)	4.90	1580	26.3
MAX332	4.90	1580	26.3
MAX313	4.31	1520	25.3

A. Evolution of Switching Threshold Voltage and Inactivity Windows

Almost from the beginning of the irradiation, a shift in the switching threshold voltage was observed in all the samples. This evolution was not similar in the whole set of tested devices, as it can be deduced from the various kinds of technologies of the devices: In some switches, like the ADG212, the threshold value monotonically decreased but, on the contrary, it soared in other ones, like DG212 switches from Maxim & Vishay. The evolution of some of the samples is shown in Fig. 7.

The destruction of the switches happened following two different typical behaviors. In some cases, the steady diminution

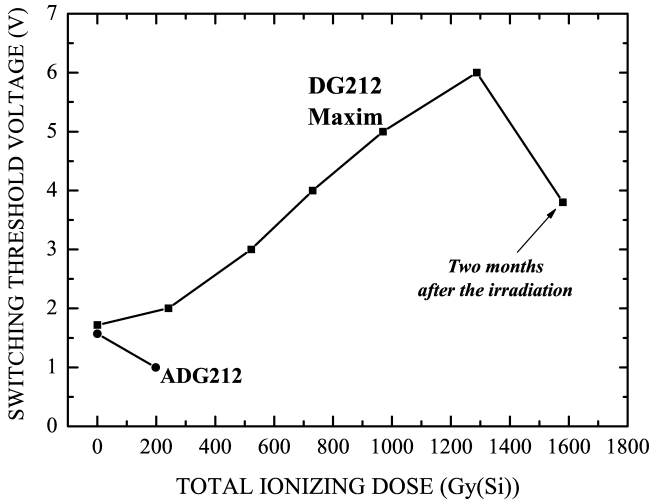

Fig. 7. Evolution of the switching threshold voltage in some devices. This graph shows the measured values during the irradiation along with the value after the isotope deactivation, two months later.

of the switching threshold voltage makes it go below 0 V. Obviously, the switch cannot work since the logic input value is limited by 0 & 15 V. DG212, from Analog and Vishay, belongs to this set of devices. In other cases, the switch suddenly stops working when it reaches a critical value of TRD, i.e., MAX332: At a TRD value of $8{\cdot}10^{12}$ n·cm^{-2} & 240 Gy, the possibility of switching between ON & OFF states definitively disappears.

A good way to visualize the evolution of the analog switches is by means of bar diagrams. These graphs have the following set of characteristics. The horizontal axis, with a discrete value range from 0 to 15 V, represents the control logic input while the two vertical axes are related to the TRD values: Left, the neutron fluence and right, the TID. Every value in the left Y-axis has a correspondence in the right one and the scaling factor is deduced from Table I.

Over every value of control input on the X-axis, there is a bar in black & white. In this 2D-graph, every point of the graph is related to a value of TRD, by means of the two vertical axes, and to a logic voltage, corresponding to the horizontal one. If one point is painted in white, this means that the switch is OFF and, obviously, if black, the switch is ON. For example, the evolution of ADG212 and DG212 from Maxim, already depicted in Fig. 7, can be summarized in this kind of bar diagrams (Fig. 8-9). E.g., it is immediately observed in Fig. 8 that a pristine device cannot switch with an input voltage of 1 V but it can from a TRD value of $7.4{\cdot}10^{13}$ n·cm^{-2} & 200 Gy on and, finally, the total absence of black regions shows that it cannot switch for any value of logic input voltage if the value of TRD goes beyond $2.17{\cdot}10{\cdot}10^{13}$ n·cm^{-2} & 585 Gy.

This kind of representation has been introduced since it is very appropriate to present the phenomenon of inactivity windows. For instance, Fig. 10 summarizes the behavior of the ADG412 switch. In this figure, we can observe that the switch stops working at a TRD of $1.84{\cdot}10^{13}$ n·cm^{-2} & 495 Gy. In fact, no matter the value of the input threshold voltage may be, the switch is always open. However, as the irradiation goes

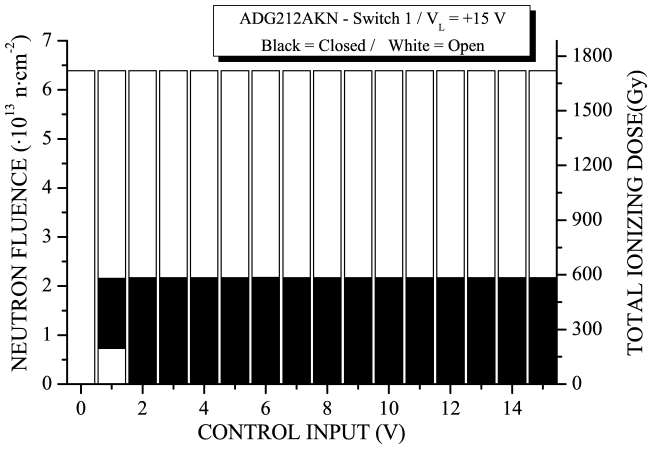

Fig. 8. Bar diagram associated to the ADG212

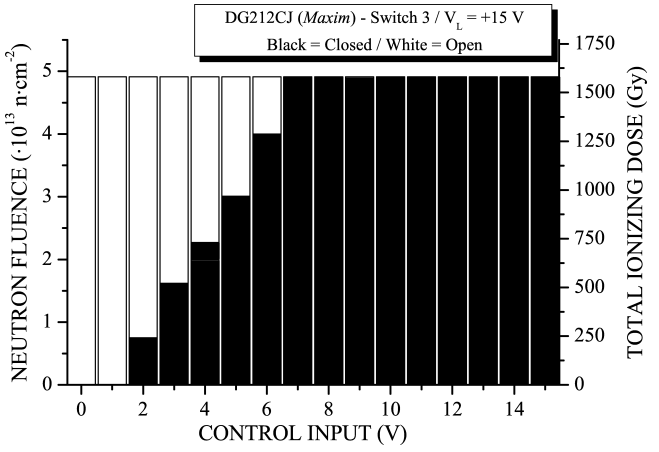

Fig. 9. DG212s bar diagram, where the increase of the switching threshold voltage is easily observed.

on and the TRD value reaches a value of $4.77{\cdot}10^{13}$ n·cm^{-2} & 1285 Gy, the switch suddenly recovers its ability to work. According to the graph, the switch is ON if the value is 2 V or more and OFF if below. The existence of the inactivity window can be also observed regarding the evolution of its resistance and conductance, shown in Fig. 11.

Inspecting the whole set of data, the following characteristics of the inactivity windows are eventually discovered: First of all, the inactivity windows can appear in only a subset of the four switches of the switch. For example, inactivity windows were observed in switches 1 & 2 of Fig. 1 while in the switches 3 & 4 were not. Besides, some devices can undergo several inactivity windows. (E.g., MAX313 in Fig. 12).

Sometimes, the inactivity windows can be misled with the lattice recovery caused by the annealing during the reactor technical shutdowns.For example, in Fig. 10, we can see a narrow strip starting at $1.69{\cdot}10^{13}$ n·cm^{-2} & 444 Gy and ending at $1.73{\cdot}10^{13}$ n·cm^{-2} & 454 Gy. However, this is not an actual inactivity window but just a phenomenon related to the annealing. In fact, this switch gave up working some minutes before the reactor stopped. During the night, the switch semiconductor lattice partially recovered so the switch could work again the following morning. However, the device

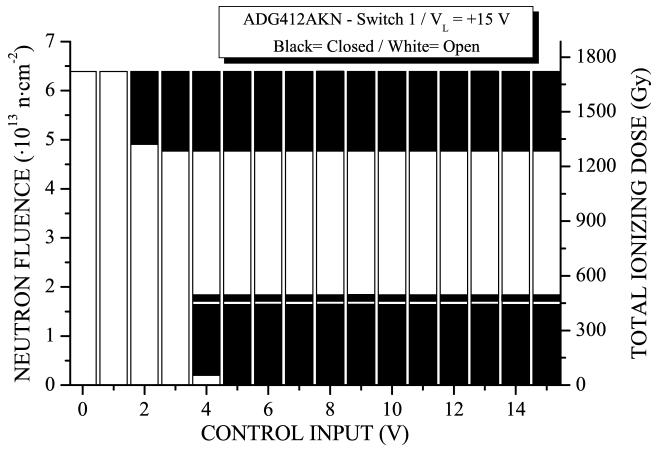

Fig. 10. Evolution of the switching threshold voltage and inactivity window of the ADG412.

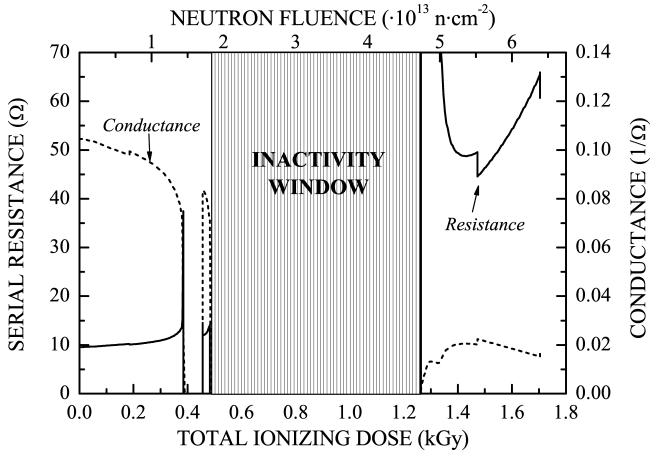

Fig. 11. Serial resistance and conductance of ADG412, from Analog Devices, with logic input voltage of 15 V. The inactivity window happens between 495 & 1285 Gy, and its defining characteristic is a drop of the conductance value down to 0 Ω^{-1}.

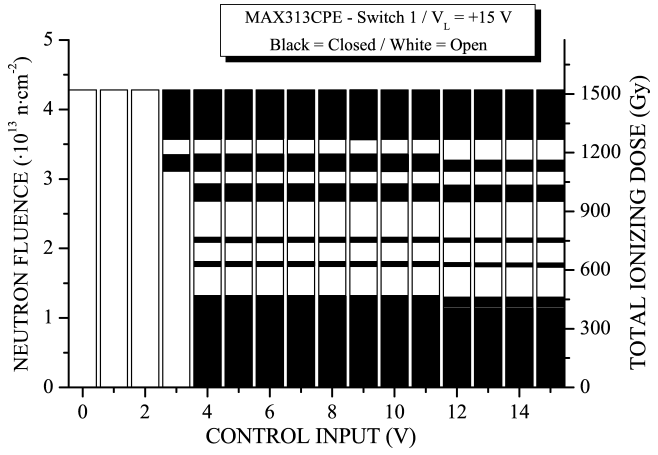

Fig. 12. Evolution of the switching threshold voltage and inactivity windows in MAX313 with V_L=15V.

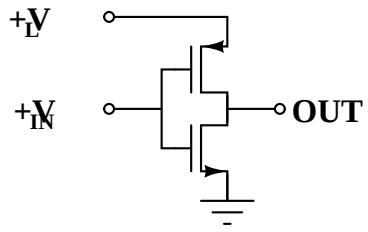

Fig. 13. CMOS inverter, as a logic input stage. This structure is present in some networks of the analog switches.

was still so damaged that it could not come back to activity when the new radiation session began. In general, the inactivity windows must appear and end while the reactor is functioning, being usually very wide and lasting for some hours or days.

B. Anomalous behavior of the hard logic levels

Other odd phenomenon is related to the behavior of MAX313 switch (Fig. 12). If the TRD value is between $3.25{\cdot}10^{13}$ n·cm^{-2} & 1115 Gy and $3.35{\cdot}10^{13}$ n·cm^{-2} & 1190 Gy, the switch is open with hard logic voltages, (0 & 15 V). However, it can be closed with intermediate voltages between 3 & 11 V. The same fact was found in the DG412 from Vishay when the TRD is between $6.3{\cdot}10^{12}$ n·cm^{-2} & 175 Gy and $6.8{\cdot}10^{12}$ n·cm^{-2} & 190 Gy. In other words, hard logic levels are not valid even though intermediate values are.

IV. Discussion

A. Origin of inactivity windows in CMOS inverters

Usually, internal topologies of commercial devices are not public because of manufacturers' property policies. However, data sheets of these devices usually show the presence of structures as CMOS inverters, level shifters, etc. (Fig. 5-6). A study of these simple CMOS networks helps to propose a physical mechanism that could explain the appearance of the inactivity windows. Let us consider a simple CMOS inverter, as drawn in Fig. 13. A P-channel MOSFET is used as a pull-up load device for an N-channel MOSFET pull-down device. For the CMOS inverter, the drain current of NMOS must equal the drain current of PMOS under all static operating conditions. The modes of operation for a P-channel MOSFET are the same as those for the N-channel MOSFET. The drain current expressions are identical in form with the voltage polarities and current directions reversed. In this digital network, the values of the noise margins V_{IL} & V_{IH} are obtained by solving two linear and quadratic equations, respectively [13]:

$$V_{IL} = V_{TH,N} + V' \cdot \frac{3 + k'_R + 2 \cdot \sqrt{k'_R \cdot (k'_R + 3)}}{(k'_R + 3) \cdot (k'_R - 1)} = V_{TH,N} + C_{TN} \cdot (V_L - V_{TH,N} + V_{TH,P}) \quad (1)$$

$$V_{IH} = V_{TH,N} + V' \cdot \frac{k_R \cdot (k_R + 3) + 2 \cdot \sqrt{k_R \cdot (k_R + 3)}}{(k_R + 3) \cdot (k_R - 1)} = V_{TH,N} + C_{TP} \cdot (V_L - V_{TH,N} + V_{TH,P}) \quad (2)$$

where $V_{TH,X}$ are the threshold voltage of the NMOS and PMOS, $V' = (V_{DD} - V_{TH,N} + V_{TH,P})$ and $k'_R = \frac{k_N}{k_P}$, $k_R = \frac{k_P}{k_N}$; C_{TX} symbolizes two different parameters for V_{IH} and V_{IL} whose values depend on the values of the transconductances k_P and k_N. The negative solutions deduced from the quadratic expression are omitted because of being non-sense. An effect of the ionizing radiation on MOS transistors is the shift of the threshold voltage value [14]. PMOS transistors exhibit a growth in the absolute value of that parameter but, on the contrary, the evolution of NMOS transistors depends on the dose rate [15]. In these devices, two phenomena with opposite consequences (Trapping of positive charge, creation of interface states) compete in such a way that there is a great dependence on the dose rate in the final value of $V_{TH,N}$. If the irradiation is very slow, the threshold voltage value increases since the trapping of negative charge in the interface states outdoes the positive charge on the oxide. On the contrary, a very quick irradiation will lead to a diminution of threshold voltage value due to the large number of trapped positive charges inside the gate oxide. However, in most actual irradiations, NMOS transistors present a mixture of both behaviors since they usually exhibit a decrease of V_{TH} in the early stage of the irradiation that ceases when a critical TID value is reached. Then, the threshold voltage value starts increasing.

If the threshold voltage changes as previously explained, the initial positive value of $V_{TH,N}$ in eq. 1 & 2 may become close to 0 V or even negative, leading the inverter to a situation where the OUT voltage cannot switch between HIGH & LOW values since $V_{IH} < 0$. However, the rebound expected in $V_{TH,N}$ would lead to a state where V_{IH} has returned to positive values. In short, the CMOS inverter would manage to switch again after an interval where it was unable to work correctly. Thus, an inactivity window would have been observed.

C_{TX} in eq. 1 & 2 is always related to the value of $k'_R = \frac{k_N}{k_P}$. The dependence on this ratio adds new details for the comprehension of the nature of inactivity windows. Both parameters derive from the carrier surface mobilities, which depend on the silicon mobility and on the concentration of SiO_2-Si interface states [16]. Thus, displacement damage, which decreases to the silicon mobility, could play a secondary role in the evolution of the windows.

B. Level shifters

The previous discussion has pinpointed a phenomenon that may explain the appearance of inactivity windows in some circumstances. However, the main drawback of this explanation is that the the shifts of threshold voltage values must be on the order of several volts (similar to V_L or V_{CC}).

However, simulations performed in several typical level shifter networks have shown that inactivity windows appear even with small shifts of V_{TH}. The only condition to be accomplished is that the threshold voltage value of the NMOS transistors becomes negative during the irradiation.

Unlike the internal CMOS inverters, manufacturers are reluctant to publish the internal structure of the level shifters.

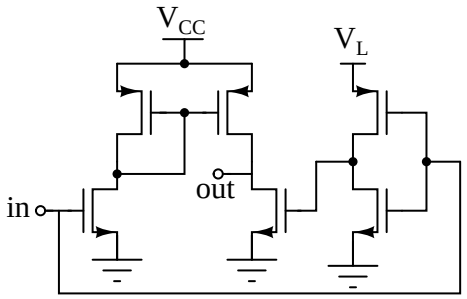

Fig. 14. Simple DC level shifter [19].

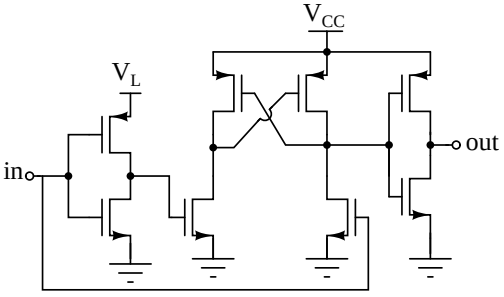

Fig. 15. DC level shifter with crossed gates [20].

However, an scan of the literature [17]- [22] allow us to know that the most popular shifters are based on the structures of Fig. 14 & 15. Now, let us suppose that the MOS threshold voltage values change as Fig. 16 shows, typical behavior of the MOS transistors [23].

The structures of Fig. 14 & 15 were simulated in SPICE seeking the switching threshold value with values of $V_L = 5V$ and $V_{CC} = 15V$. For this purpose, a DC sweep from -10 to 10V was performed for several values of TID, the MOS threshold voltages being selected from those of Fig. 16. The results are shown in Fig. 17. In this graph, we can realize that the simple structure of Fig. 14 shows a slight decrease followed by a final growth. However, the most important

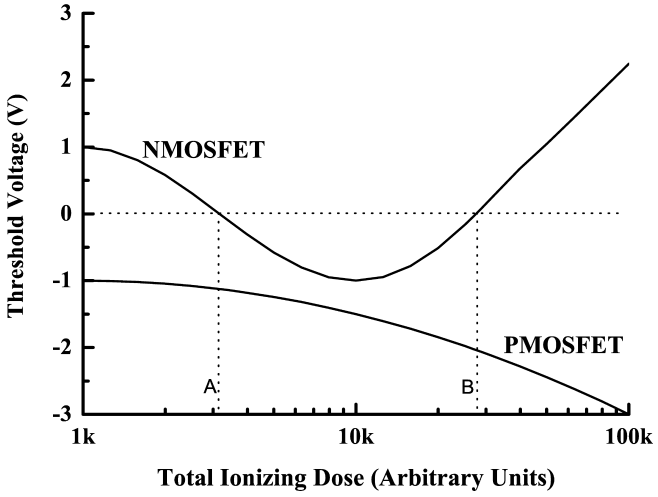

Fig. 16. Typical evolution of the value of the MOS transistors.

information is provided by the evolution of the switching threshold value of Fig. 15. Unlike the other structure, this does show actual inactivity windows. According to Fig. 17, after the beginning of the irradiation but prior to A, related to the TID value where $V_{TH,N}$ becomes lower than 0V, the switching threshold voltage of the shifter, $V_{TH,SW}$ softly decreases from 4.56V down to 3.82V. However, once the value of $V_{TH,N}$ is lower than 0V, SPICE simulations point out to the fact that the value of $V_{TH,SW}$ undergoes a sudden increase up to 5.59V. Given that the top input value is $V_L = 5V$, it is clear that the output of the DC level shifter is 0V whichever the logic input value is. Thereby, the channel of the analog switch, which is controlled by this stage, is open.

If the total ionizing dose keeps increasing, the threshold voltage of the NMOS transistor reaches its minimum and, afterwards, starts increasing. The consequence of this fact is a steady shift of the value of $V_{TH,SW}$, which is always higher than the highest value of the logic input voltage, V_L. However, when the value of $V_{TH,N}$ again becomes positive, the value of $V_{TH,SW}$ suddenly suffers another modification. In fact, when the level shifter is in B, the value of this parameter drops from 6.96V down to 4.50 V. In other words, the DC level shifter can work again. In consequence, the inactivity window is directly related to a negative sign of the threshold voltage of NMOS transistors.

Afterwards, the irradiation goes on and a consequence of it is the slow but continuous growth of $V_{TH,SW}$. When this parameter reaches the top logic value, $V_L = 5V$, the output of the level shifter can no longer switch between ON & OFF states (C in Fig. 17) so the level shifter is supposed to be destroyed unless the irradiation stops and the annealing of the transistors brings the value of $V_{TH,SW}$ to the zone between 0V-5V.

A final result obtained from the simulations is that an increase of the power supplies values allows the devices to switch again. For instance, if the SPICE simulation is repeated with $V_L = 10V$ instead of $V_L = 5V$, the calculated value of the logic switching threshold is 6.77V. Therefore, the device is capable of switching. This is the reason why the DG412 samples of the first experience work with $V_L = 15V$ and not with $V_L = 5V$. his theory can satisfactorily explain the appearance of onlyone inactivity window although in some devices there was evidence of two or more windows. However, we must bear in mind that actual analog switches have more complicated structures and also other additional blocks. In this situation, inactivity windows happening in each individual block inside the analog switch would cause the existence of several windows in the whole device

C. Inactivity windows & test methods

The physical mechanism proposed to explain the inactivity windows can be easily applied not only to analog switches but to other CMOS devices. Therefore, inactivity windows are susceptible to appear in any kind of CMOS structures. A consequence of the existence of inactivity windows is the fact that radiation tests carried out irradiating devices with only a few values of TID might not detect the existence of inactivity

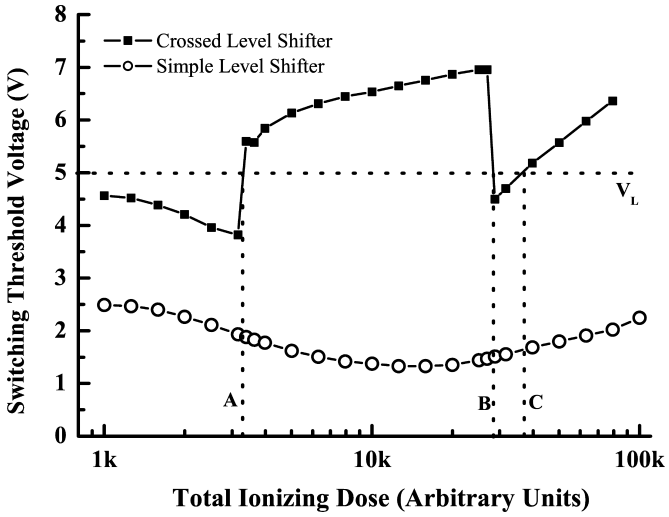

Fig. 17. Evolution of the switching threshold value of the typical DC level shifters. Simulations performed with SPICE OPUS, improved version of Berkeley SPICE [24].

windows. In consequence, a supposed rad-tol system might fail because the undetected inactivity windows of one of the devices used in the system design.

Finally, it must be taken into account that the evolution of any irradiated CMOS device depends on other parameters, such as the dose rate, bias voltages, temperature, etc., so the characteristics of the inactivity windows must be also influenced by these parameters. In any case, further works are necessary to deeply understand this phenomenon.

V. Conclusion

This paper has proved the existence of inactivity windows in analog switches and has provided a physical reason to explain this phenomenon. Besides, the existence of the inactivity window may be supposed to appear in other CMOS devices so radiation tests should be careful enough to detect the existence of these windows and not overrate the radiation tolerance of the device.

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