Field effect transistors based on α-MoO_3 exfoliated crystals: fabrication, functionalization and characterization

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Abstract (max. 200 words)

α-MoO_3 Field Effect Transistors (FETs), exhibiting n-type behaviour, were fabricated. These devices are based on α-MoO_3 exfoliated crystals, which were produced from bulk crystals by mechanical exfoliation and then transferred onto Si/SiO_2 substrates, through a two-step clean transfer process. The FET devices were then achieved by depositing three electrical contacts in a bottom-gate geometry, using photolithography, metal sputtering deposition and lift-off. Thermal treatments in different atmospheres (vacuum and air) were performed to tune the electrical properties of the channel material, by controlling the oxygen vacancy concentration. Preliminary electrical characterization of a modified device reveals a modulation of channel resistance with the gate bias, in agreement with the characteristic n-type behaviour of α-MoO_3. Notably, it exhibits a promising electron mobility value of approximately 0.117 $cm^2\ V^{-1}\ s^{-1}$, which is comparable to values reported for n-type FETs based on a single/few atomic layers of α-MoO_3 and MoS_2. Additionally, the transfer curves exhibit anticlockwise hysteresis effects, likely attributed to the adsorption/desorption processes of oxygen molecules on the channel surface, promoted by the applied gate voltage.

Keywords: two-dimensional, molybdenum oxide, field effect transistor, thermal annealing, anticlockwise hysteresis

1. Introduction

Two-dimensional (2D) materials have been the subject of interest in recent years due to their unique physical and chemical properties, not found in their three-dimensional (3D) counterparts. In nature, these

materials typically do not exist in their 2D form, but rather as bulk crystals, where multiple atomic layers are stacked together. Based on their elemental composition and atomic structure, these materials can be categorized into different groups, including the graphene family, transition metal chalcogenides, and transition metal oxides.[1] Graphene stands out for its remarkable electron mobility (~10^5 cm^2 V^{-1} s^{-1})[2], however, the absence of a band gap restricts its use in electronic devices. Although transition metal chalcogenides exhibit significant band gaps, devices based on these materials often suffer from relatively low charge carrier mobility.[3,4] In contrast, molybdenum trioxide (MoO_3), which belongs to the family of transition metal oxides, has emerged as a promising candidate for achieving high electron mobility, since its high dielectric constant can promote an effective reduction of Coulomb scattering effects, thereby facilitating charge carrier transport.[5–7] Additionally, MoO_3 is recognized as one of the most promising semiconductors for various applications[8], including biosensors[9], gas sensors[10], solar cells[11], and lithium-ion batteries[12].

Molybdenum oxide (MoO_3) is a n-type wide band gap semiconductor that can crystalize in different phases, with the orthorhombic phase (α-MoO_3) being the only thermodynamically stable form at room temperature.[13] This phase exhibits a lamellar structure along the [010] direction, which allows an easy exfoliation into single or few atomic layers, with a high crystalline quality and a high surface-to-volume ratio.[14] In addition to its high dielectric constant, stoichiometric α-MoO_3 exhibits an insulating behavior related to its wide band gap, which makes this material a good candidate to use as a dielectric layer in several types of electronic devices.[15–17] Furthermore, defects in MoO_3, namely oxygen vacancies, play a crucial role in defining its electrical properties. Indeed, oxygen vacancies will act as donors, providing electrons to the conduction band and, consequently, increasing the conductivity of the material. Thus, by controlling the concentration of these defects, the insulating nature of stoichiometric α-MoO_3 can be modified, leading to a semiconductor or even metallic behavior.[18–21] Indeed, semiconducting behaviour has been observed in MoO_x phases with $2 < x \leq 3$, while the MoO_2 phase exhibits semi-metallic electrical characteristics.[22,23] Additionally, W.-B. Zhang et al.[7] demonstrated, using deformation potential theory and first-principles calculations, that the charge carrier mobility in a few layers of MoO_3 can exceed 3000 cm^2 V^{-1} s^{-1} at room temperature. This high value is related to the high dielectric constant of the material, which minimizes Coulomb scattering effects and enables high charge carrier mobility. This reduction in Coulomb scattering is particularly advantageous for electronic applications, such as field-effect transistors (FETs), as it allows for the tuning of the material properties by creating defects, without compromising the performance of the final devices. For example, S. Balendhran et al.[5] demonstrated the incorporation of MoO_{3-x} nanocrystals, with ~11 nm thickness, in FET devices. Despite the atypical response of an n-type semiconductor, the authors reported mobility values greater than 1100 cm^2 V^{-1} s^{-1}, exceeding the values reported for silicon[24] and MoS_2 monolayers[4]. Additionally, M. M. Y. A. Alsaif et al.[6] evaluated the performance of MoO_{3-x} FET devices as a function of the reduction level (x value) of the material and also found atypical transfer curves resembling that of a p-type channel. The optimal performance was observed for x = 0.42, yielding electron mobility values of 600 cm^2 V^{-1} s^{-1} and an I_{ON}/I_{OFF} ratio of 10^5.[6] In contrast, n-type field-effect transistors based on a few monolayers of α-MoO_3 have demonstrated lower electron mobilities. For example, F. Rahman et al. [25] reported electron mobilities of approximately 175 cm^2 V^{-1} s^{-1} for FETs based on post-etched MoO_3 crystals. Moreover, electron mobilities ranging from 0.03 to 0.09 cm^2 V^{-1} s^{-1} were observed, when 2D MoO_3 nanosheets and single crystals were incorporated into FETs.[26,27] Additionally, M. Zhong et al. [27] demonstrated a strong in-plane electron transport

anisotropy in 2D α-MoO_3 crystals, which result in an electron mobility values along the [001]-axis 2.2 times higher than that along the [100]-axis.

In this work, we report the fabrication, functionalization and characterization of α-MoO_3 field effect transistors, exhibiting an n-type response. These FETs were produced from MoO_3 exfoliated crystals with thicknesses of a few hundred nanometers, using clean room facilities and a bottom-gate configuration. Given the high resistance of the α-MoO_3 crystals, thermal treatments in different atmospheres were performed to tune the electrical properties of the material, by modulating the defects concentration. Specifically, vacuum annealing was carried out to increase the conductivity of the crystals by creating oxygen vacancies, while thermal treatments in air were performed to gradually decrease their conductivity through the recovery and/or passivation of these defects. This modification process allowed us to obtain a device exhibiting transfer curves typical of an n-type semiconductor, along with anticlockwise hysteresis effects, attributed to oxygen adsorption/desorption processes on the channel surface. With this geometry, an electron mobility of 0.117 $cm^2\ V^{-1}\ s^{-1}$ was achieved, surpassing that of some MoO_3-based FETs reported in the literature [26,27] and comparable to MoS_2 FETs.[28–31]

2. Experimental Results

2.1. Defect engineering of the 2D-MoO_3 exfoliated crystals

Figure 1(a) shows the schematic diagram of the back-gate α-MoO_3 FETs obtained in this work, where the source and drain metal contacts (200/1000 Å Ti/Au) were deposited on top of the exfoliated crystals, while the gate electrode (50/800 Å Ti/Au) was deposited on the back side of the substrate (Si part of the substrate). In this geometry, the 300 nm thick SiO_2 layer of the substrate works as dielectric layer of the device. Figures 1(b) and 1(c) show optical microscopy images of two α-MoO_3-FET devices, where the drain/source contacts have a width of 20 µm and are separated 10 µm.

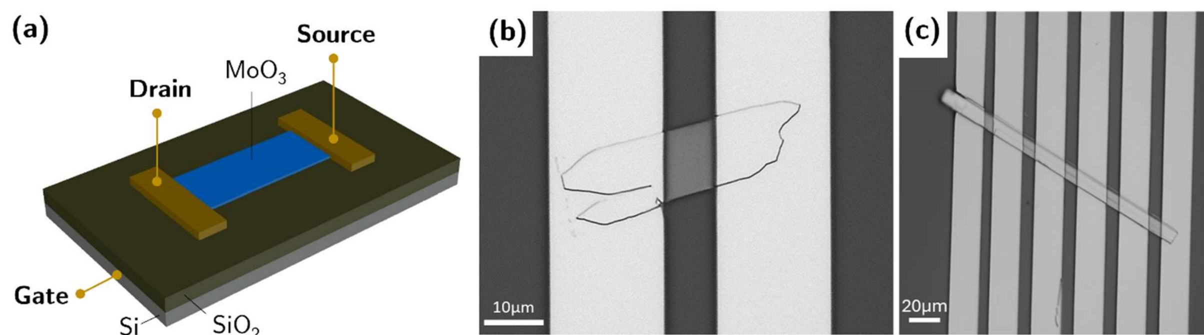


Figure 1 – (a) Schematic of the α-MoO_3 FET devices with a bottom-gate, top-contacts (BGTC) geometry. (b)-(c) Images obtained by optical microscopy of two distinct α-MoO_3 FET devices, taken after the entire microfabrication process.

Figure 2(a) shows some representative I-V curves, in logarithmic scale, of the final devices, measured between the drain and source contacts, before and after thermal treatments in vacuum/air. Note that, all the I-V curves in Figure 2(a) exhibit an ohmic behaviour, as demonstrated in Figure S1 of the Supporting Information. The geometry of these characterized devices is illustrated in Figure 2(b). Based on the grey curves in Figure 2(a), it is possible to observe that the obtained devices exhibit high resistance, as expected for a wide band gap semiconductor, with the lowest measured value being ~117 MΩ. After vacuum annealing at 350°C for 30 minutes – blue curves in Figure 2(b) – an increase of the conductivity over several

orders of magnitude is observed, which was attributed to the increase of the free carriers (electrons), resulting from the creation of oxygen vacancies, as suggested by the micro-Raman spectroscopy measurements shown in Figure S3 of the Supporting Information. Indeed, the formation of oxygen vacancies in MoO_3 introduces shallow donor levels within the band gap, increasing the number of free carriers inside the material and, consequently, its electrical conductivity.[19,23,32,33] Establishing a clear relation between conductivity gain and annealing conditions (temperature and duration) proved challenging, due to the variation of conductance among devices even when processed simultaneously, as seen in Figure 2 and in Figure S1 of the Supporting Information. Such variations are attributed to different MoO_3 crystal dimensions as well as surface degradation during processing, as discussed later. However, it was estimated that the threshold temperature, above which a significant increase in the conductivity of the crystals is observed, is approximately 300°C, in agreement with threshold temperatures for the formation of oxygen vacancies reported in the literature [34]. It should be noted that none of the as-fabricated or vacuum annealed devices revealed transistor behaviour. While the former were too resistive, the latter were too conductive to allow a gate modulation with our equipment.

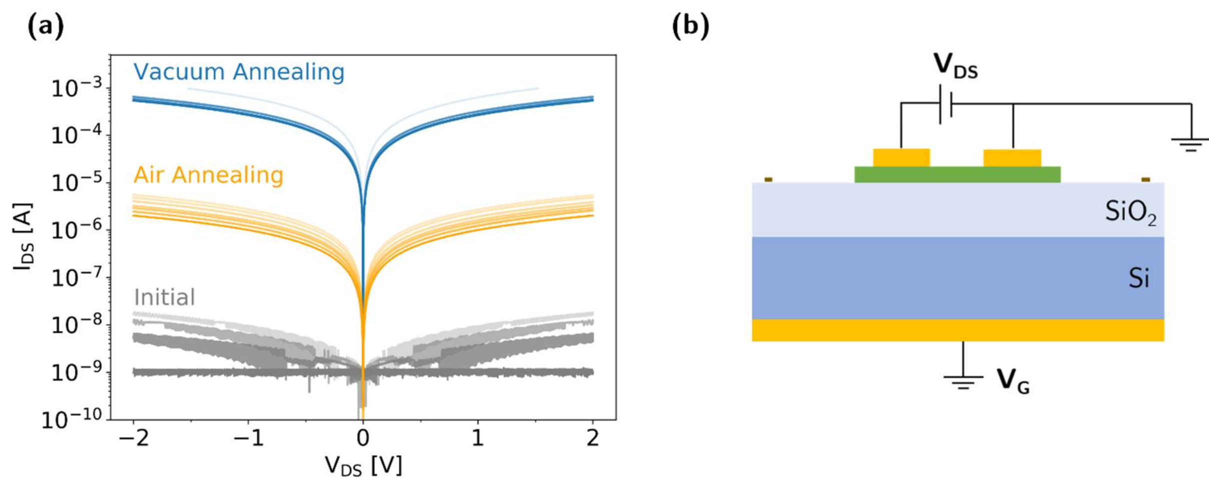
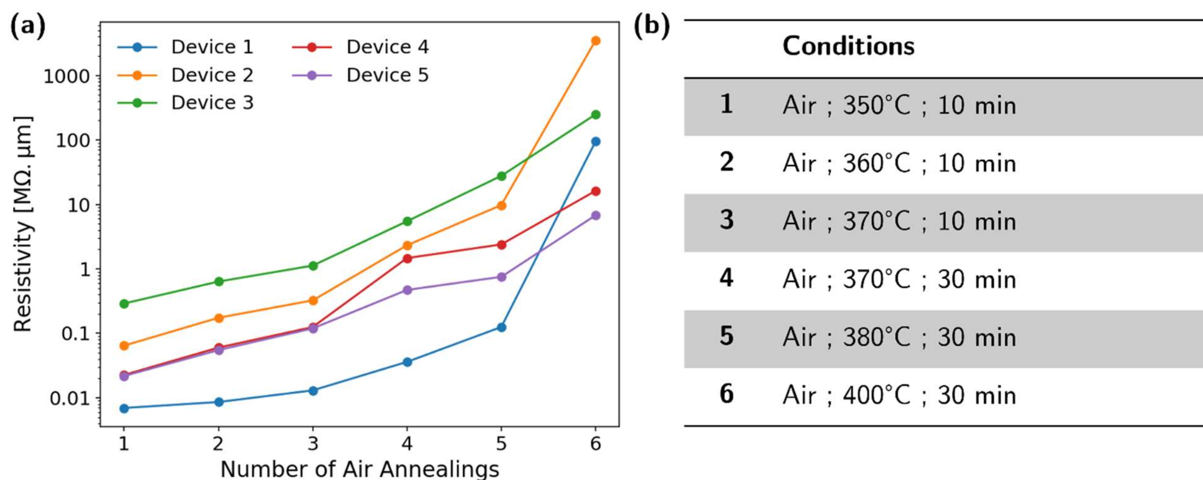


Figure 2 - Representative I-V curves, in logarithmic scale, of several α-MoO_3-FET devices processed simultaneously: before any thermal treatment – grey curves - after vacuum annealing (1×10^{-4} mbar) at 350°C for 30 minutes – blue curves – and after vacuum annealing (1×10^{-4} mbar) at 350°C for 30 minutes, followed by air annealing at 300°C for 20 minutes - orange curves. The geometry of the characterized FET devices is represented in (b).

After the increase in conductivity induced by vacuum annealing – blue curves in Figure 2(a) - the conductivity of the exfoliated crystals can be reduced through thermal treatments in air. This behaviour is demonstrated in Figure 2(a) by the orange curves, which represent the I-V curves in logarithmic scale of various devices after vacuum annealing at 350°C for 30 minutes, followed by air annealing at 300°C for 20 minutes. Comparing the blue and orange curves in Figure 2(a), it is possible to see that, after vacuum annealing, the measured current values are in the milliamperes range, decreasing to microamperes after air annealing. This effect is attributed to the recovery of oxygen vacancies during air annealing, as well as by the adsorption of oxygen molecules on the surface of the crystals. Indeed, a similar effect is observed when the samples are exposed to air, where their conductivity decreases over time. Note that, the adsorption processes are promoted by the presence of oxygen vacancies on the surface of the crystals, which act as active sites that attract oxygen molecules to the surface. This conductivity modulation demonstrates that by combining both types of annealing (in vacuum and in air), the electrical properties of the final devices can

be more precisely controlled, allowing for the production of devices with electrical characteristics better suited for a typical FET response. An example of this is shown in Figure 3, demonstrating the evolution of the resistivity of five different FET devices on the same substrate, all subjected to the same air annealing sequence. The total resistance of the devices was determined from their respective I-V curves, while the channel dimensions were estimated using optical microscopy (for length and width) and AFM measurements (for thickness). In the resistivity calculations, the contact resistance was assumed to be negligible, as discussed later. These devices were first subjected to vacuum annealing to increase the conductivity of the MoO_3 channel, followed by multiple thermal treatments in air - summarized in Figure 3(b) - to gradually reduce the conductivity of the devices. A representative example of the evolution of the I-V curves with this annealing sequence is shown in Figure S2 of the Supporting Information. Based on Figure 3(a), it is possible to conclude that there is a gradual increase in the resistivity of the devices as the number of thermal treatments in air increases. Furthermore, although the devices exhibit different resistivity values, the evolution of their resistivity with the number of annealing steps is quite similar. This behaviour indicates that the gain in conductivity of the devices subjected to the same annealing process is identical, regardless of the initial characteristics of the crystals. However, correlating this increase in conductivity with the annealing parameters, such as temperature and duration, remains a significant challenge. Also, when calculating the resistivity, we assume that the current path corresponds to the entire channel. However, it is possible that, despite air annealing, a conductive surface layer with high oxygen vacancy concentration remains. While this does not change the conclusions drawn here, it may have a significant effect on FET device performance, as will be discussed later. It is also worth noting that, multiple air annealing sequences were tested, and, in all cases, the devices exhibited a similar resistance evolution with the number of annealing steps.



	Conditions
1	Air ; 350°C ; 10 min
2	Air ; 360°C ; 10 min
3	Air ; 370°C ; 10 min
4	Air ; 370°C ; 30 min
5	Air ; 380°C ; 30 min
6	Air ; 400°C ; 30 min

Figure 3 – (a) Evolution of the resistivity of several devices belonging to the same substrate, as a function of the number of thermal treatments in air (1→6). (b) Summary of the air annealing conditions used.

Finally, by performing four-point probe (4PP) measurements on the FET devices subjected to the different thermal treatments, it was possible to conclude that the changes in the electrical properties of the final devices, shown in Figures 2 and 3, are due to the creation/annealing of defects in the MoO_3 crystals, rather than modifications in the resistance of the electrical contacts – see Section 3 of the Supporting Information for a detailed discussion. Indeed, the total resistance of the electrical contacts is negligible compared to the

resistance of the MoO_3 channel, independently of the type of thermal treatment performed – Figure S5 and Table S1 of the Supporting Information.

2.2. FET based on 2D-MoO_3 exfoliated crystals

By combining vacuum and air annealing to tune the electrical properties of the final FET devices, it was possible to obtain one device that exhibits a typical FET response, as shown in Figure 4(a), where the I-V characteristic curves (I_{DS}-V_{DS}), for different applied gate voltages (V_G) are plotted. Thus, for a fixed voltage between the drain and source contacts (V_{DS}), an increase in the I_{DS} current is observed when the gate voltage (V_G) varies from -80 V to +80 V - Figure 4(a) - confirming a modulation of the channel resistance with the gate bias. This means that the channel resistance decreases with increasing gate voltage, which is consistent with the n-type behaviour characteristic of α-MoO_3. The hysteresis effects observed in all output curves shown in Figure 4, may be associated with the presence of defects on the surface of the crystal and/or at the semiconductor-dielectric interface, which act as traps to the charge carriers. Note that, this hysteresis effects are specific to this device and that most other devices did not show hysteresis effects for V_G=0V, as shown in Section 2.1 and in Section 1 of the Supporting Information for V_G=0 V. Furthermore, it is important to mention that the lack of a transistor response in most of the obtained devices may suggest that the current flows through a thin and highly conductive surface layer, formed due to the presence of a significant number of oxygen vacancies induced by the vacuum annealing. As a result, depending on the combination of the thermal treatments in air and vacuum and the crystal thickness, the electrical field induced by the applied gate voltages may not be strong enough to effectively modulate the current flow. However, further tests are needed to draw definitive conclusions regarding these aspects.

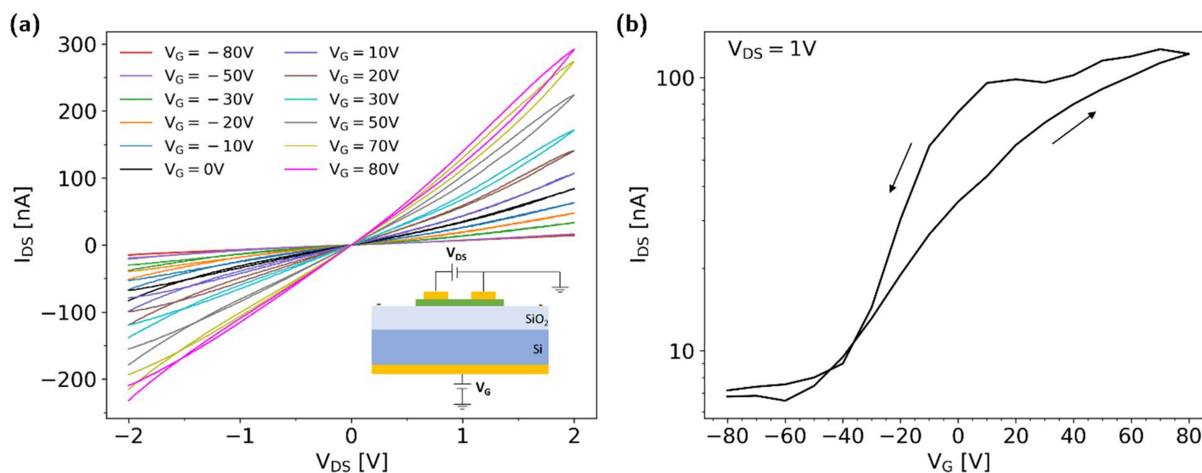


Figure 4 – Electrical characterization of an α-MoO_3 FET device: (a) Evolution of the I-V characteristic curves (I_{DS}-V_{DS}), as the gate voltage (V_G) varies from -80 V to +80 V. The schematic illustration of the geometry of the FET device used for the electrical characterization is shown in the inset. (b) Transfer curve (I_{DS}-V_G) for a fixed V_{DS} of 1V, obtained from the I-V characteristic curves in (a) for a gate voltage (V_G) sweep of -80 V → +80 V → -80 V (black arrows).

Figure 4(b) displays a representative transfer curve of an α-MoO_3 FET at a fixed V_{DS} voltage of 1 V, obtained through the I-V characteristic curves for different applied gate voltages. In addition to the modulation of channel resistance with gate bias, Figure 4(b) also reveals the presence of anticlockwise hysteresis in the transfer curve, which makes the response of the device dependent on the direction of the V_G sweep. Note that, although the performance of the device degraded quickly during consecutive sweeps of the high gate

voltages, the hysteresis consistently shows the presented anticlockwise behaviour. The presence of hysteresis effects in transfer curves is widely reported in 2D-FET devices, where these effects are often attributed to the capture and release of electrons in intrinsic defects/traps. These traps can have different origins, such as: adsorbed species on the semiconductor surface, defects in the material structure, defects at the semiconductor/dielectric layer interface, or within the dielectric layer.[35] The direction of the hysteresis depends on the predominant process.[35] In MoS_2 and amorphous α-IGZO (indium-gallium-zinc oxide) FET devices, the observed anticlockwise hysteresis at room temperature is attributed to the presence of mobile ions inside the dielectric layer (SiO_2), whose spatial distribution varies with the applied gate voltage.[35,36] In synaptic transistors based on α-MoO_3 thin films and crystals, a similar anticlockwise hysteresis is attributed to the incorporation/release of protons, resulting from the dissociation of water molecules.[37,38] By comparing the transfer curves of the α-MoO_3 FET devices with those of β-Ga_2O_3 (not shown here) - both obtained simultaneously and with the same geometry - it was possible to conclude that the hysteresis exhibits opposite direction, being clockwise for the β-Ga_2O_3 FET devices. Therefore, the presence of mobile ions within the SiO_2 layers cannot be the main responsible for the hysteresis effects exhibited by the fabricated devices, as the dielectric layer is the same for both the MoO_3 and Ga_2O_3 FETs. Thus, the hysteresis effects shown in Figure 4(b) may be related to the presence of adsorbed molecules on the crystal's surface, such as oxygen and/or water molecules. Note that, due to the vacuum annealing performed to increase the electrical conductivity of the final devices, a significant number of defects (namely, oxygen vacancies) are expected on the crystal's surface, which will promote the adsorption of species from the atmosphere. In fact, A. R. Head et al.[39] demonstrated by ambient pressure X-ray photoelectron spectroscopy (XPS) and density functional theory (DFT) calculations that, contrary to what is observed at stoichiometric MoO_3 surfaces, the adsorption and dissociation of water molecules on MoO_3 is promoted by the presence of oxygen vacancies and OH^- groups on the surface of the material. On the other hand, it has also been demonstrated that the adsorption of molecules on the surface of these MoO_3 crystals, particularly oxygen, plays a crucial role in their electrical response.[40] For example, the conductivity of vacuum-annealed MoO_3 crystals decreases significantly over time, when the crystals are left in ambient air.[40] This behaviour was attributed to the recovery and/or passivation of defects due to the adsorption of oxygen on the surface of the crystals.[40] Additionally, the adsorption and desorption of oxygen molecules on the surface of these crystals allowed to explain the high persistent conductivity observed, after irradiation with UV light and protons in vacuum.[40] Indeed, under vacuum conditions, switching off the excitation sources resulted in slow response times and a strong persistent conductivity. In contrast, exposing the crystals to atmospheric pressure led to a faster current decay, with the current returning close to its initial value.[40] In the present study, the adsorption of oxygen molecules on the channel surface of the FET devices may give rise to the hysteresis effects observed in Figure 4(b). Furthermore, this adsorption process can be modulated by the voltage applied at the gate contact, as illustrated in Figure 5. Note that, the model represented in Figure 5 was adapted from hysteresis models developed for MoS_2 FET devices, where hysteresis was attributed to the adsorption of species on the channel surface.[35,41]

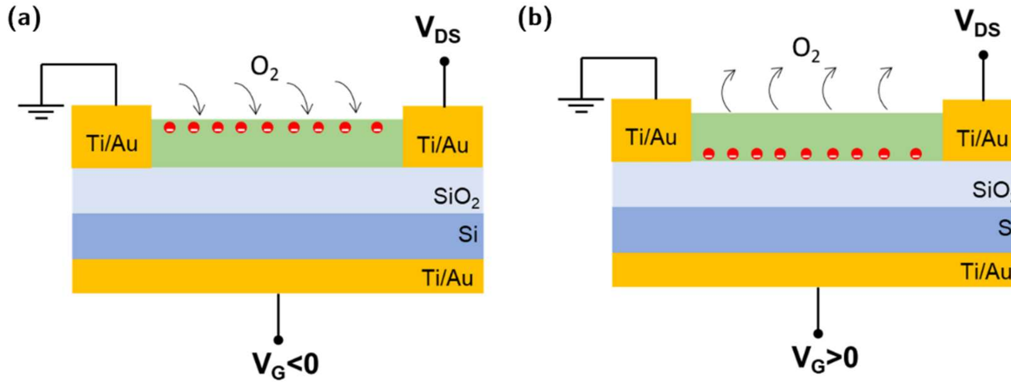


Figure 5 - Schematic of the electron capture/release process due to the adsorption/desorption of oxygen molecules on the channel surface of α-MoO_3 FET devices, modulated by the voltage applied at the gate contact (V_G): (a) electron capture by oxygen molecules under negative gate voltage, and (b) release of electrons from the adsorbed oxygen molecules under positive gate voltages and desorption of O_2.

According to the proposed model, applying negative voltages to the gate contact repels the charge carriers (electrons) towards the crystal's surface, depleting the channel of free charges, which originates the OFF state of the device – Figure 5(a). Additionally, the presence of electrons on the surface of the material will promote the adsorption of oxygen molecules, which will capture these electrons (forming O_2^-), thereby making the material more resistive. As the gate voltage increases (towards positive values), the electrons progressively migrate into the material, and the adsorption processes becomes less predominant. For positive gate voltages – Figure 5(b) – the electrons are attracted to the semiconductor/dielectric interface, promoting the desorption of oxygen molecules from the surface. As reported by several authors[40,42,43], oxygen molecules adsorbed at the oxygen vacancy sites can be desorbed by releasing the captured electrons back into the lattice, indicating that these molecules are weakly bound on the surface of the material. This leads to an increase in charge carriers inside the channel and, consequently, an increase in the conductivity of the final device. Since the desorption of species is a slow process, it does not follow immediately the evolution of the voltage applied at the gate contact. As a result, the channel exhibits lower conductivity during the gate voltage sweep from -80 V to +80 V, and higher conductivity when the voltage sweep is reversed (from +80 V to -80 V), which is in agreement with the transfer curve shown in Figure 4(b). It will be interesting to further test this model, e.g., by performing similar device characterisation in vacuum. It is important to note that, in addition to the adsorption of oxygen molecules on the channel surface, other processes may also contribute to the observed hysteresis effects. For example, water molecules trapped at the semiconductor/dielectric interface can also contribute to these effects, as the applied gate voltage may promote the intercalation of H^+ ions, resulting from the dissociation of water molecules through a process similar to that reported in Refs.[37,38]. This intercalation will lead to the formation/dissociation of an hydrogen molybdenum bronze phase (H_xMoO_3) within the channel, for positive/negative voltages applied at the gate contact, thereby contributing to anticlockwise hysteresis effects. In fact, a similar local proton intercalation process was observed in MoO_3 nanosheets, promoted by the electric field induced by the polarization of an AFM tip.[44]

Figure 6 shows the transfer curve (I_{DS}-V_G) presented in Figure 4(b) for the V_G sweep from -80V to 80V, and the corresponding logarithm of the I_{DS} current as a function of the gate voltage. Based on the transfer curves shown in Figure 6, several parameters were extracted, including the onset voltage (V_{ON}), the threshold voltage (V_{th}), the ratio between the ON and OFF state currents (I_{ON}/I_{OFF}), the transconductance (g_m), the

subthreshold swing (SS), and the electron mobility (μ_e). The obtained parameters are summarized in Table 1.

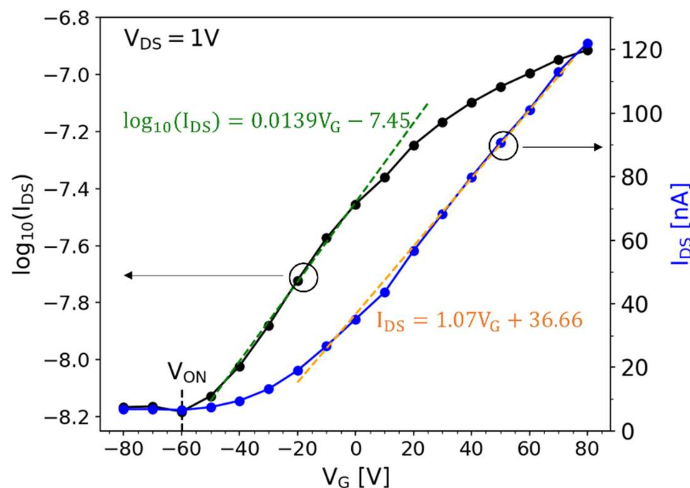


Figure 6 - Transfer curve (I_{DS}-V_G) and the logarithm of the I_{DS} current as a function of the gate voltage, obtained from the evolution of the I-V characteristic curves for a V_G sweep from -80 V to +80 V. These curves were obtained for a fixed V_{DS} voltage of 1 V. Transconductance (g_m) and subthreshold swing (SS) values were determined from the slope of the orange linear fit and from the inverse of the slope of the green linear fit, respectively. The threshold voltage (V_{th}) was estimated by intercepting the orange linear fit with the x-axis.

Table 1 - Onset voltage (V_{ON}), threshold voltage (V_{th}), I_{ON}/I_{OFF} current ratio, transconductance (g_m), subthreshold swing (SS), and electron mobility (μ_e) values, obtained from the curves shown in Figure 6.

V_{ON} [V]	V_{th} [V]	I_{ON}/I_{OFF}	g_m [nS]	SS [V/dec]	μ_e[cm^2/V.s]
-60	-34	19	1.07	72	0.117

As shown in Figure 6, the modulation of I_{DS} current with gate voltage results in an onset voltage of -60 V, a threshold voltage of -34 V and an I_{ON}/I_{OFF} ratio of 19, as summarized in Table 1. This onset and threshold voltage align with the values observed in FET devices with a thick dielectric layer (~300 nm), where high gate voltages (> |10 V|) are typically needed to induce the transition between the OFF and ON states of the device.[45] Additionally, factors such as the low-quality of the dielectric layer (low dielectric constant), the high thickness of the crystals, and the presence of adhesive residues and/or adsorbed species on their surfaces can further contribute to an increase in the onset/threshold voltage. Indeed, the threshold voltage can increase significantly with the thickness of the channel device, as demonstrated in Ga_2O_3-FETs.[46,47] It is important to note that most of the crystals obtained by mechanical exfoliation in this work have thicknesses in the order of hundreds of nanometers, which is significantly thicker than what is typically reported in the literature for MoO_3 and MoS_2, where only a few monolayers (generally a few tens of nanometers thick) are used.[5,28–30,48] As a result, it is expected that thicker materials will require higher gate voltages to effectively modulate the charges within the material. Moreover, the channel layer may still be too conductive, requiring high negative voltages to reach the OFF state. Additionally, as demonstrated in Figure S6 in the Supporting Information, the I_{DS} current takes approximately 50 minutes to stabilize, when a fixed V_{DS} and V_G voltages are applied. However, the V_G sweeps carried out in this work were much faster (~30 seconds per point), suggesting that the channel did not reach an equilibrium state for each

applied gate voltage. This factor may contribute to the low I_{ON}/I_{OFF} current ratio shown in Table 1 and may be related with the hysteresis effects discussed above.

From the transfer curve in Figure 6, a transconductance value (g_m) of 1.07 nS and a subthreshold swing (SS) of 72 V/dec were also obtained, as summarized in Table 1. The transconductance value (g_m) was determined from the slope of the orange linear fit in Figure 6 and represents the increase in I_{DS} current per unit of gate voltage (V_G) applied. Similarly, the subthreshold swing (SS) quantifies the gate voltage required to increase the I_{DS} current by a factor of 10, and is derived from the inverse of the slope of the green linear fit in Figure 6. For comparison, in an ideal FET device based on 2D materials, the subthreshold swing value is approximately 60 mV/dec, which corresponds to the thermionic limit.[45] However, most reported devices exhibit, not only, thick dielectric layers, but also a high density of traps at the semiconductor/dielectric interface, which increases the SS value to the order of hundreds of mV/dec.[45] In fact, in addition to the adsorption/desorption process of molecules on the channel surface, which were mentioned as the primary cause of hysteresis effects in the transfer curves, defects at the semiconductor/dielectric interface or within the dielectric layer may also act as traps for free charges. Furthermore, the presence of adhesive and organic residues (such as photoresist) on the crystal's surface can also contribute to the degradation of the electrical performance of the devices. For example, J. Liang et al.[49] demonstrated that the conductivity, mobility and charge density within the channel were negatively affected by residues on the surface of MoS_2 and WSe_2 crystals, resulting from the lithography process. It is also important to mention that craters with a few nanometers in height were observed on the surface of the crystals, suggesting material degradation, likely due to the exposure of the crystals to the organic compounds used during the microfabrication process – see Section 7 of the Supporting Material. Despite all the efforts, this degradation could not be entirely prevented, resulting in a negative impact on the performance of the devices.

Once the transconductance value (g_m) was determined, the electron mobility (μ_e) was calculated using the expression $\mu_e = \frac{L}{C_d W V_{DS}} g_m$. In this calculation, a channel with a length (L) of 8.86 µm and a width (W) of 7.04 µm, and a dielectric capacitance per unit area (C_d) of $1.15 \times 10^{-8} F\ cm^{-2}$[5] were considered. The calculated electron mobility, which represents the velocity of electrons under an electric field, was found to be 0.117 $cm^2\ V^{-1}\ s^{-1}$, as summarized in Table 1. Comparing this value with those reported in the literature, the obtained MoO_3 device exhibits an electron mobility that is one order of magnitude higher than that of some similar devices based on a few atomic layers of MoO_3 (0.03-0.09 $cm^2\ V^{-1}\ s^{-1}$) [26,27]. On the other hand, the obtained electron mobility is within the range of values reported for FET devices with monolayers of MoS_2 on SiO_2 (0.1-10 $cm^2\ V^{-1}\ s^{-1}$).[28–31] Note that, these were our first tests on incorporating MoO_3 exfoliated crystals into FET devices, and therefore, improved performance can be achieved by optimizing the geometry and microfabrication processes, similar to what was observed in MoS_2.[4,28,50] For example, encapsulating the device will effectively minimize the interaction of the crystals with the surrounding atmosphere, preventing the adsorption of species onto their surface. Indeed, H. Qiu et al. [28] demonstrated that annealing MoS_2 FET devices in vacuum led to an increase in electron mobility from ~0.12 $cm^2\ V^{-1}\ s^{-1}$ to ~2.4 $cm^2\ V^{-1}\ s^{-1}$. Similarly, J. Li et al.[50] reported an improvement in the I_{ON}/I_{OFF} ratio, which increased from 1.4×10^6 to 1.8×10^7, along with a rise in charge mobility from 1 $cm^2\ V^{-1}\ s^{-1}$ to 4.2 $cm^2\ V^{-1}\ s^{-1}$, and a 30% reduction in subthreshold swing for MoS_2 FET devices when placed in vacuum. This improvement in device performance was attributed to the desorption of species on the material's surface, namely oxygen and water molecules, which acted as traps for free carriers. Additionally, it is expected that the Coulomb scattering effects will be minimized in MoO_3 compared to MoS_2, due to the higher relative

dielectric constant of MoO_3 (> 500 for MoO_3 versus ~5 for MoS_2), which will contribute to higher mobility values.[5] In fact, a notable increase in conductivity, by several orders of magnitude, was observed in these crystals, after introducing a significant amount of defects in the lattice by ion implantation. [20]

3. Conclusions

In this work, n-type MoO_3-FET devices were fabricated using clean room microfabrication processes, starting from α-MoO_3 bulk crystals. The microfabrication process involved the mechanical exfoliation of the bulk crystals and their transfer to Si/SiO_2 substrates, followed by deposition of the three electrical contacts in a bottom-gate geometry, using photolithography and metal sputtering deposition. By performing thermal treatments in both air and vacuum atmospheres, the electrical conductivity of the final devices was tuned, due to the modulation of defect concentration within the channel. Specifically, the creation of oxygen vacancies by vacuum annealing at temperatures between 300°C and 400°C, results in an increase in the conductivity of the final devices by several orders of magnitude. In contrast, successive thermal treatments in air, in the same temperature range, promote the recovery of defects as well as their passivation through the adsorption of oxygen molecules on the surface of the material, which progressively reduces the conductivity of the devices. This modification strategy allowed to obtain one device with a typical n-type FET response, where a modulation of the channel resistance with applied gate voltage is verified. The channel resistance decreases with increasing gate voltage, which agrees with the characteristic n-type behaviour of α-MoO_3. In addition to the modulation of the channel resistance with gate bias, the transfer curves of the final device also reveal anticlockwise hysteresis effects, which were attributed to the adsorption/desorption process of oxygen molecules on the channel surface. When a negative gate voltage is applied, oxygen molecules are adsorbed on the channel surface, decreasing the number of free carriers in the channel. On the other hand, for positive gate voltages, the electrons trapped by the adsorbed oxygen molecules are released into the channel, resulting in an increase in its conductivity. As oxygen adsorption and desorption are slow processes, they do not respond instantaneously to changes in gate voltage, resulting in the observed anticlockwise hysteresis effects in the transfer curves. However, it is also important to emphasize that other factors, such as defects at the semiconductor/dielectric interface, defects in the dielectric layer, and/or the adsorption of other species on the surface/interface of the devices, may also contribute to the hysteresis effects.

Despite these hysteresis effects, the obtained α-MoO_3-FET device shows an electron mobility of 0.117 cm^2 V^{-1} s^{-1}. This value is notably higher compared to similar few-layer MoO_3 devices and is comparable to the mobility values reported for FETs based on single-layer MoS_2. This promising result paves the way for developing devices with enhanced performance, through the optimization of device geometry and microfabrication processes. Note that, due to the high permittivity of MoO_3, a minimization of the Coulomb scattering effects is expected, which leads to a lower degradation of charge carrier mobility caused by the presence of defects. In fact, unlike most materials, introducing defects in MoO_3 through ion implantation leads to a significant increase in its electrical conductivity.[20] This technique may be promising to reproducibly tune the conductivity in the center of the channel. In contrast, the modulation of the conductivity via surface defects employed in this work leads to a high chemical reactivity of the surface, which is probably responsible for the hysteresis effects and other underwhelming FET parameters related with the slow switching speed of the device.

4. Experimental Details

4.1. 2D-MoO_3 Synthesis and Transfer

α-MoO_3 lamellar crystals, with a typical thickness of (2-4) µm and lateral dimensions of 2×5 mm^2, were grown by an evaporation-solidification method, as described in detail in Refs.[20,40,51,52]. In summary, this growth method consists of evaporating a disc of compacted Mo powder, inside a horizontal tube furnace at 750°C for 10h, with a controlled air flux of 2 l/min. During this process, the evaporated Mo is oxidized by the surrounding atmosphere and transported to the cooler ends of the tube by the air flux, where it is deposited at a temperature around 400-450°C. After growth, MoO_3 lamellar crystals were mechanically exfoliated with a Kapton tape, to obtain nanoflakes with a high surface-to-volume ratio. The exfoliated crystals were then transferred from the tape to the SiO_2/Si substrate, using a two-step clean transfer process, as described in detail in Section 5 of the Supporting Information. In this process, the exfoliated crystals on the Kapton tape were initially transferred to an intermediate Si substrate, using a polydimethylsiloxane (PDMS) stamp. Subsequently, they were transferred from the Si to the SiO_2/Si substrate, using a PDMS-PC structure (a polycarbonate (PC) layer deposited on PDMS). This strategy was employed, because it allowed not only the selection of specific crystals but also control over their positioning on the final SiO_2/Si substrate, keeping the final substrate practically free of residue.

4.2. Device Fabrication

Using clean room facilities, MoO_3 exfoliated crystals were incorporated into Field Effect Transistors (FETs) with a bottom-gate top-contacts (BGTC) geometry - Figure 1(a) - according to the procedure described in detail in Sections 5 and 6 of the Supporting Information. In short, in this procedure, before transferring the exfoliated crystals to the final substrate (p-doped Si substrates with 300 nm of SiO_2 deposited on them), 150 Å thick TiW cross-shaped marks (12.5×12.5 μm^2) were defined at specific positions on the final substrate. This was achieved on the TiW thin film deposited by sputtering (Nordiko 7000 cluster tool, from a Ti10W90 target, at 500W DC, with 2.9 mTorr) by performing an optical lithography with a Direct Write Laser Heidelberg 2.0 system, followed by an ion milling etching step using a Nordiko 3600 machine (Argon broad beam with ~340 $\mu A/cm^2$, 1.4 mTorr with an etch rate ~1 Å/s). These TiW marks were used as reference points to determine the position of the exfoliated crystals on the final substrate, in a similar way to that realized by D. Verheij et al.[53]. Subsequently, the MoO_3 bulk crystals were exfoliated and transferred to the final substrate with the deposited TiW marks, according to the procedure described in detail in Section 4.1 and in Section 5 of the Supporting Information. Using optical microscopy and the TiW marks present on the substrates, the positions of the exfoliated crystals were determined, enabling the definition and deposition of the drain and source contacts on top. To achieve this, a photolithography process was carried out, followed by magnetron sputtering deposition of 200/1000 Å Ti/Au using an Alcatel SCM 450 machine (with a pressure of 3 mTorr and a DC power of 40 W for Ti deposition and a RF power of 20W for Au deposition). Before performing the lift-off process to remove the excess metal, the backside of the substrate was cleaned with acetone and isopropanol, and then placed again into the deposition chamber, where 50/800 Å Ti/Au was deposited to form the gate contact. Once the gate contact was deposited, the lift-off process was carried out in acetone to remove the metal outside the drain/source contact regions. As the exfoliated crystals showed degradation during long periods of exposure to the developer, the development time was reduced from 60 s (standard time) to 30 s. Figures 1(b) and 1(c) show optical microscopy images of two α-MoO_3-FET devices.

4.3. Modification and Characterization

Thermal treatments in a controlled atmosphere were carried out using a Rapid Thermal Annealing (RTA) furnace, specifically the ANNEALSYS AS-one 100 system. Initial annealing to increase the vacancy concentration and thus the conductivity of the channel was carried out in vacuum ($1x10^{-4}$ mbar) for 15/30 minutes at 350°C. Further treatments were performed in air, with temperatures ranging from 300°C to 400°C and duration between 5 and 30 minutes, in order to recover oxygen vacancies and tune the conductivity of the channel. The heating rate was set at 0.5°C/s for all treatments. The temperatures were chosen based on a previous study using the Perturbed Angular Correlation technique, which established a threshold temperature between 310°C and 400°C for the formation of oxygen vacancies during 10-minutes air annealing.[34]

Electrical characterization was performed using an Agilent B1500A Semiconductor Device Analyser that allows to measure maximum resistance values in the order of hundreds of megaohms. However, for these resistance values, the I-V curves exhibit high noise with currents in the nanoamperes range or below. To determine the MoO_3 channel thickness in the final devices, atomic force microscopy (AFM) measurements were performed using an Agilent 5500 (Picoplus) microscope. Both dynamic and contact modes were employed depending on the device under analysis. In dynamic mode, silicon cantilevers (TESP-V2, from Bruker) with a nominal spring constant of 37 N/m and a curvature radius of 7 nm were used. For contact mode, silicon nitride cantilevers (DNP-10, from Bruker) were used with a nominal spring constant of 0.12 N/m and a curvature radius of 20 nm. All AFM images were formed by 512 x 512 pixels.

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Supporting Information:

Field effect transistors based on α-MoO_3 exfoliated crystals: fabrication, functionalization and characterization

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1. Modification of the electrical properties of the final devices by thermal annealing

Figure S1 presents the I-V curves of different α-MoO_3-FET devices, before and after thermal treatments in air and vacuum atmospheres. These I-V curves are also shown in logarithmic scale in Figure 2 of the main manuscript. Based on Figure S1, an increase and decrease in the conductivity of the final devices, in several orders of magnitude, is observed after a vacuum and air annealing, respectively. Additionally, the ohmic behavior of the MoO_3-FET devices is preserved during the thermal treatment processes.

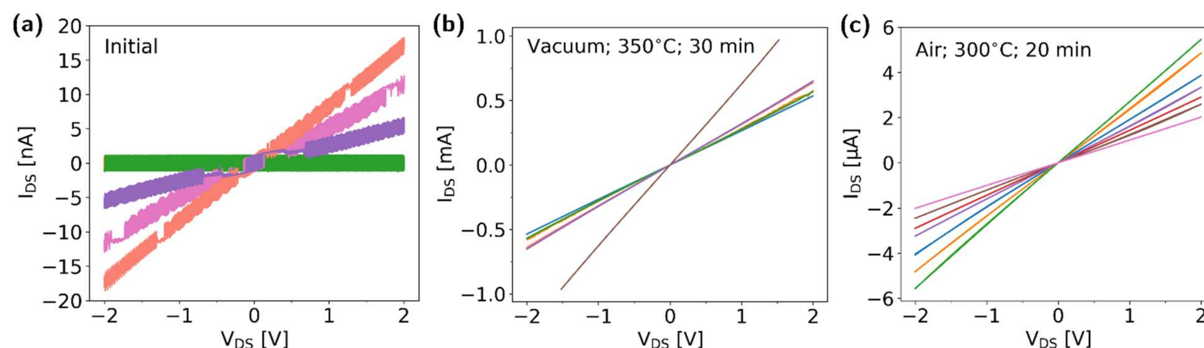

Figure S1 - Representative I-V curves of several α-MoO_3-FET devices processed simultaneously: (a) before any thermal treatment, (b) after vacuum annealing (1×10^{-4} mbar) at 350°C for 30 minutes, and (c) after vacuum annealing (1×10^{-4} mbar) at 350°C for 30 minutes, followed by air annealing at 300°C for 20 minutes. These I-V curves are also shown, in logarithmic scale, in Figure 2(a) of the main manuscript.

Figure S2 shows the evolution of the I-V curves for one α-MoO_3 FET device after different thermal treatments. In Figure S2(a), a significant increase in the conductivity of the device is observed, after vacuum annealing at 350°C for 15 minutes. After that, the device was subjected to multiple thermal treatments in air (1st → 6th) to gradually reduce its conductivity, as shown in Figure S2(b). The specific conditions of these thermal treatments are summarized in Figure 3(b) of the main manuscript. From Figure S2(b), a gradual decrease in the slope of the I-V curves is observed after each thermal treatment in air, indicating a progressive reduction in the conductivity of the devices. These results demonstrate that a more precise control over the electrical conductivity of the final devices can be achieved by combining thermal treatments in air and vacuum.

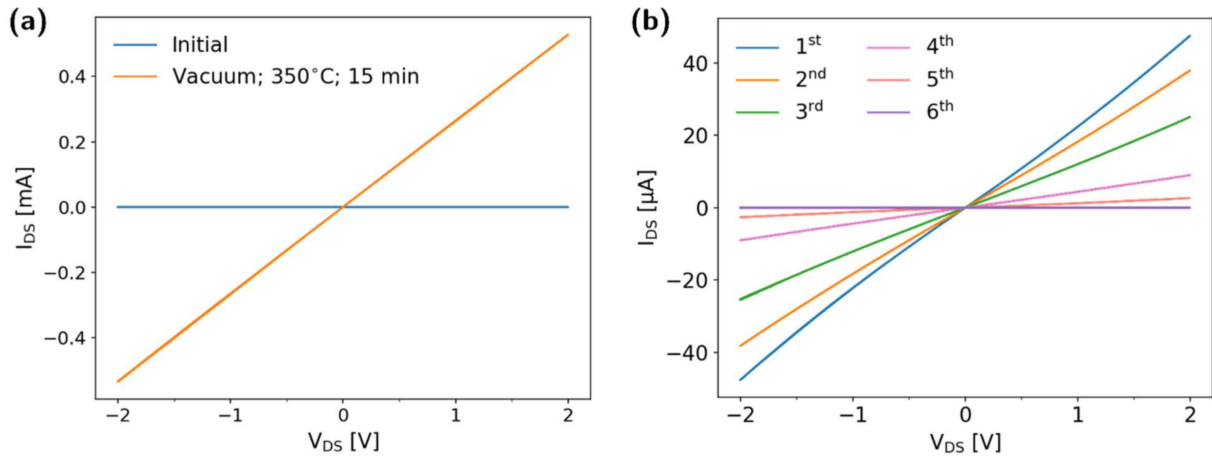

Figure S2 - I-V curves of a α-MoO_3-FET device: (a) before and after vacuum annealing at 350°C for 15 minutes, and (b) after vacuum annealing at 350°C for 15 minutes, followed by successive thermal treatments in air (1st → 6th). The conditions of the thermal treatments shown in (b) are summarized in Figure 3(b) of the main manuscript.

2. Micro-Raman Spectroscopy measurements

Figure S3(a) shows the normalized Raman spectra of an as-grown MoO_3 crystal and a crystal annealed in vacuum at 300°C for 30 minutes, both measured using a UV laser. Figures S3(b) and S3(c) highlight two distinct regions of the spectra shown in (a). The Raman spectrum corresponding to the as-grown sample – black line in Figure S3(a) – shows only bands characteristic of α-MoO_3 [1], i.e, bands centered at 996, 819, 666, 470, 365, 336, 291, 283, 216, 19 and 158 cm^{-1}. However, a broadening of the bands centered at 819 and 996 cm^{-1} is observed in the Raman spectrum of the vacuum-annealed crystal - Figures S3(b) and S3(c) - which reveal changes in the oxygen stoichiometry. [1] Thus, this result indicates the formation of oxygen vacancies in the MoO_3 crystals, as a result of the vacuum annealing performed.

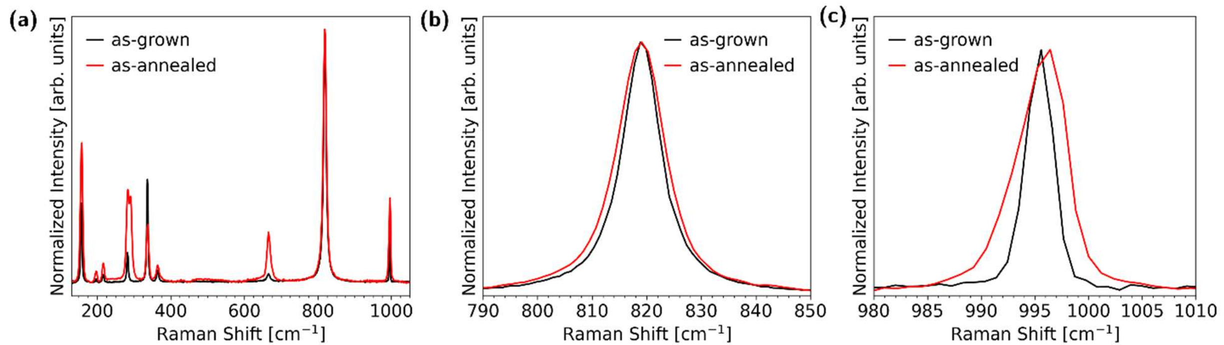

Figure S3 – (a) Normalized Raman spectra of an as-grown MoO_3 crystal and a crystal annealed in vacuum at 300°C for 30 minutes. For better visualization, the frequency ranges of 790-850 cm^{-1} and 980-1010 cm^{-1} are shown in detail in (b) and (c), respectively. These spectra were acquired with a UV laser.

3. Two-point probe (2PP) and Four-point probe (4PP) electrical measurements

To better understand the effects of thermal treatments on Ti/Au electrical contacts, 4PP electrical measurements were performed on the device shown in Figure S4(a). This device consists of an α-MoO_3 exfoliated crystal with six Ti/Au contacts deposited 10 µm apart. It is important to note that this type of device is extremely challenging to obtain, as most exfoliated crystals do not have the lateral dimensions required to deposit four electrical contacts. Figure S4(b) shows a schematic of the configuration used for the 4PP measurements on the device illustrated in Figure S4(a). In this schematic, the resistances R1-R5 represent the resistance of the crystal between the electrical contacts numbered from 1 to 6 in Figure S4(a). 4PP measurements were performed at two different positions on the crystal. In the first configuration (represented in grey in Figure S4(b)), the current was applied between contacts 1 and 4, while the voltage was measured between contacts 2 and 3. In the second configuration (represented in blue in Figure S4(b)), the current was applied between contacts 2 and 5, and the voltage was measured between contacts 3 and 4. Additionally, 2PP measurements were performed between contacts 2 and 3, and between contacts 3 and 4. Note that 2PP measurements provide the total resistance of the device, while 4PP measurements allow the determination of the channel resistance. By performing 2PP and 4PP measurements at different positions of the crystal, it was possible to obtain the total resistance of the device between contacts 2 and 3, and between contacts 3 and 4, as well as the channel resistance values, represented by R2 and R3 in Figure S4(b).

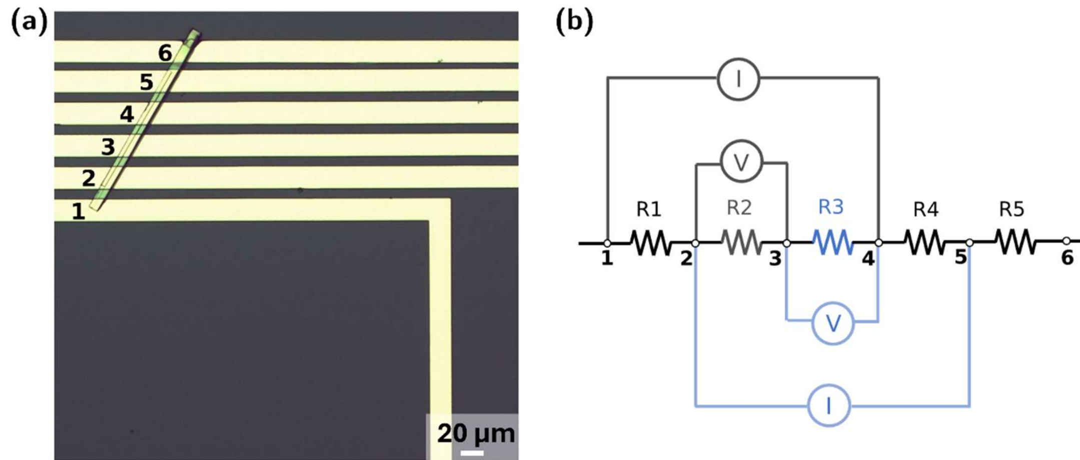

Figure S4 - (a) Image obtained by optical microscopy of an α-MoO_3 device used for four-point probe (4PP) electrical measurements. (b) Schematic of the configuration used for the 4PP measurements in two different positions of the crystal (represented in blue and grey). R1-R5 indicate the resistance of the crystal between the electrical contacts numbered from 1 to 6.

Figure S5 shows the I-V curves obtained using the 2PP and 4PP configurations at different positions on the crystal, after vacuum annealing at 300°C for 30 minutes - Figure S5(a)-(b) - and after vacuum annealing at 300°C for 30 minutes, followed by air annealing at 300°C for 20 minutes - Figure S5(c)-(d). As shown in Figure S5, the I-V curves obtained from the 2PP and 4PP configurations are very similar, regardless of the type of thermal treatment the device was subjected to, or the position on the crystal where the measurements were performed. Furthermore, it is also possible to verify that after vacuum annealing, the measured current is in the range of hundreds of microamperes - Figure S5(a)-(b) - decreasing to just a few microamperes after air annealing - Figure S5(c)-(d). This behavior suggests that the electrical contacts do not significantly contribute to the total resistance of the device, and therefore, the electrical changes induced by the annealing are directly related to the creation of defects in the crystal. Table S1 presents the resistance values (total resistance, channel resistance, and contact resistance) obtained from the I-V curves shown in Figure S5. These values indicate that the contact resistance is much lower than the channel resistance in all cases. However, a slight increase in the contact resistance is observed after air annealing, which may suggest a small modification of the electrical contact due to the annealing process, possibly due to the oxidation of titanium. Nevertheless, this change is not significant and does not compromise the overall quality of the contacts.

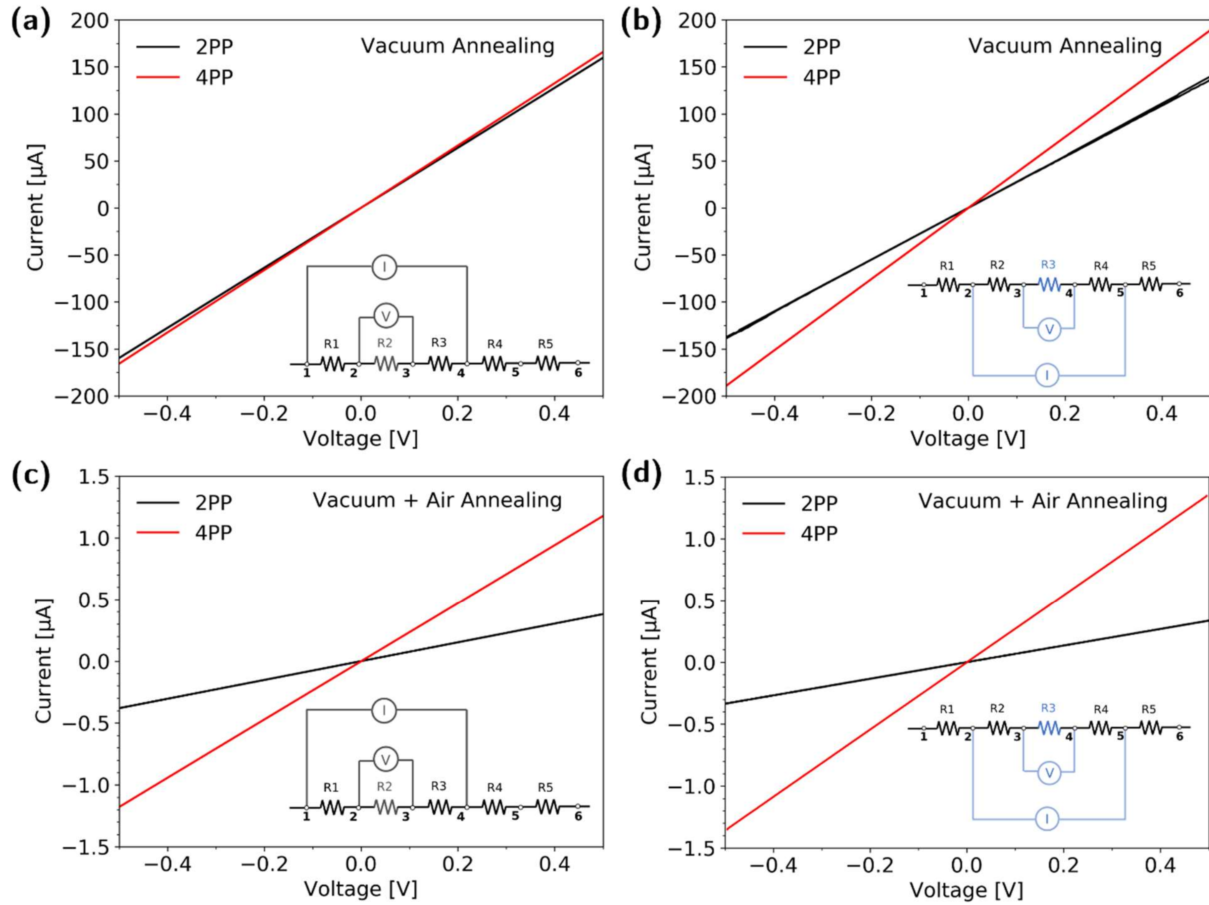

Figure S5 - I-V curves obtained using a two-point probe (2PP) and four-point probe (4PP) configuration on the device shown in Figure S4(a): (a)-(b) after vacuum annealing at 350°C for 30 minutes, and (c)-(d) after vacuum annealing at 350°C for 30 minutes, followed by air annealing at 300°C for 20 minutes. The position of the crystal where the measurements were performed is indicated in the lower right corner of each figure.

Table S1 – Summary of the total device resistance (R_T), channel resistance (R_{ch}), and contact resistance (R_C) values, obtained from the I-V curves shown in Figure S5.

	After Vacuum Annealing			After Vacuum + Air Annealing		
Resistance	R_T [kΩ]	R_{ch} [kΩ]	R_C [kΩ]	R_T [kΩ]	R_{ch} [kΩ]	R_C [kΩ]
R2	3.1	3.0	0.1	418.4	424.6	6.2
R3	3.5	2.6	0.9	365.8	368.3	2.5

4. Electrical characterization of the final FET devices

Figure S6 shows the evolution of the drain-source current (I_{DS}) over time, for both a fixed drain-source voltage (V_{DS}) of 1 V and gate voltage (V_G) of +50 V. Based on Figure S6, a gradual increase in the I_{DS} current over time is observed, followed by a I_{DS} current stabilization after 50 minutes. This behaviour demonstrates that the response of the channel to the applied gate voltage is relatively slow, requiring several minutes to reach an equilibrium state. A similar slow response was observed in vacuum-annealed MoO_3 crystals when irradiated with UV radiation and protons, where long response times and a high persistent photoconductivity were verified.[40] These two factors were explained by considering the adsorption and

desorption of oxygen molecules on the material's surface, which act as traps for the charge carriers generated by the irradiation.

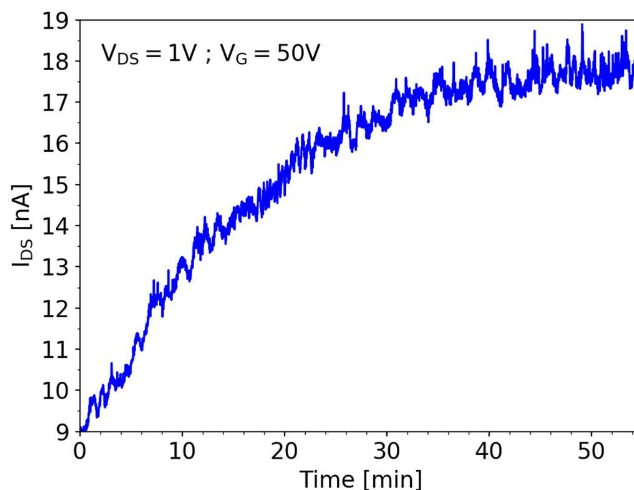

Figure S6 - Evolution of the I_{DS} current over time, for fixed V_{DS} and V_G voltages of 1 V and 50 V, respectively.

5. Clean Transfer Process of the α-MoO_3 exfoliated crystals

After mechanical exfoliation of the α-MoO_3 bulk crystals, several exfoliated crystals are obtained on both pieces of Kapton tape, which need to be transferred to a substrate. The main challenge in this process lies in minimizing the amount of residue transferred from the Kapton tape to the final substrate, as it can compromise the subsequent microfabrication steps and, eventually, the performance of the final device. In this sense, a two-step clean transfer process was adopted, using PDMS (polydimethylsiloxane) and PDMS-PC (polydimethylsiloxane-polycarbonate) structures to transfer the exfoliated crystals from the Kapton tape to an intermediate substrate, and then from the intermediate to the final substrate (Si/SiO_2), respectively. Note that, this method ensured a reproducible transfer of exfoliated crystals from the Kapton tape to the final substrate, while minimizing adhesive residues on the final substrate. To transfer the exfoliated crystals from the Kapton tape to the intermediate Si substrate – Figure S7 - a PDMS stamp was prepared by manually placing a ~1×1 cm^2 piece of PDMS on a glass slide, where it adheres - Figure S7(a). The Kapton tape, carrying the exfoliated crystals, was then placed in direct contact with the PDMS, facilitating the transfer of the crystals onto its surface - Figure S7(b). Upon removing the tape, some exfoliated crystals remained on the PDMS surface, allowing for their transfer to any desired substrate - Figure S7(b). Prior to the transfer, the PDMS structure was exposed to UV radiation for 10 minutes in a UV lamp chamber, followed by a 10-minute oxygen plasma treatment using a Harrick Plasma Cleaner (PDC-002-CE). These two treatments helped minimize adhesive residue on the PDMS and, eventually, on the crystals surface.

After the UV/O_2 treatment, the PDMS containing the exfoliated crystals was placed on a clean intermediate Si substrate and heated on a hot plate at approximately 140°C – Figure S7(c). At this temperature, the PDMS begins to detach from the Si substrate, leaving behind the MoO_3 exfoliated crystals, promoting the transfer of the crystals to the intermediate substrate – Figure S7(d). It is important to note that the transfer process is based on the reduction of the adhesion properties of PDMS as the temperature increases.[54,55]

Indeed, V. Barreau et al.[54] demonstrated that the adhesion of PDMS decreases by approximately 50%, when the temperature increases from 20°C to 120°C.

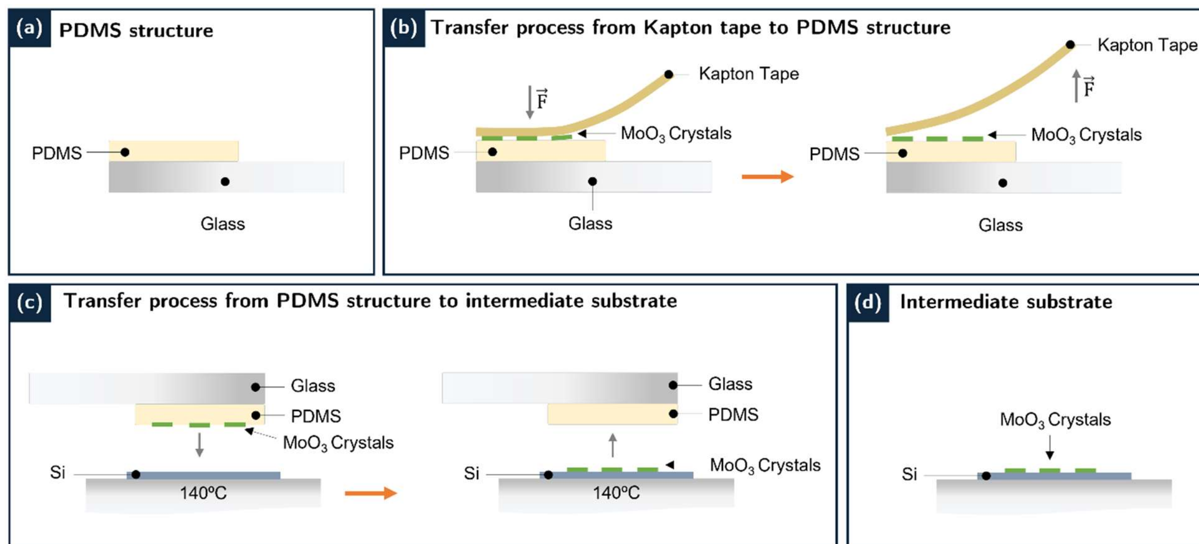

Figure S7 – Schematic illustrating the transfer process of the α-MoO_3 exfoliated crystals from the Kapton tape to the intermediate Si substrate, using a PDMS structure.

Once the MoO_3 exfoliated crystals were transferred to the intermediate Si substrate, a PDMS-PC structure was required for the second transfer step. This structure consists of a piece of PDMS adhered to a glass slide, with a PC film deposited on top. The PDMS serves solely as a support material in this configuration. The PC film was prepared by depositing a chloroform solution containing 2% polycarbonate (PC) onto a glass slide, followed by drying the coated slide at room temperature - Figure S8(a). After drying, the PDMS-PC structure was formed by transferring the PC film from the glass slide to the PDMS, using a transfer structure made of adhesive tape – Figure S8(a). The PDMS-PC structure was then placed in contact with the intermediate Si substrate, where the exfoliated crystals were transferred to the PC film upon removal of the structure – Figure S8(b). Then, the PDMS-PC structure was placed in contact with the final Si/SiO_2 substrate which was at a temperature of approximately 180°C. This temperature promotes the detachment of the PC film from the PDMS, transferring both the film and the exfoliated crystals onto the final substrate – Figure S8(c). Note that, before the transfer, the final substrate was subjected to a UV/O_3 treatment for 15 minutes in a Jelight UVO cleaner to enhance the adhesion between the exfoliated crystals and the substrate. Finally, the PC film was removed by immersing the final substrate in chloroform solution, followed by acetone and isopropanol– Figure S8(d). Figures S8(e) and S8(f) show images of the final substrate after the transfer of the crystals, and after the cleaning process, respectively. As shown in Figure S8(e)-(f), the cleaning process effectively removed most of the residues from the deposited PC film. Additionally, all exfoliated crystals that were transferred to the PC film were also transferred to the final substrate, resulting in a 100% transfer yield.

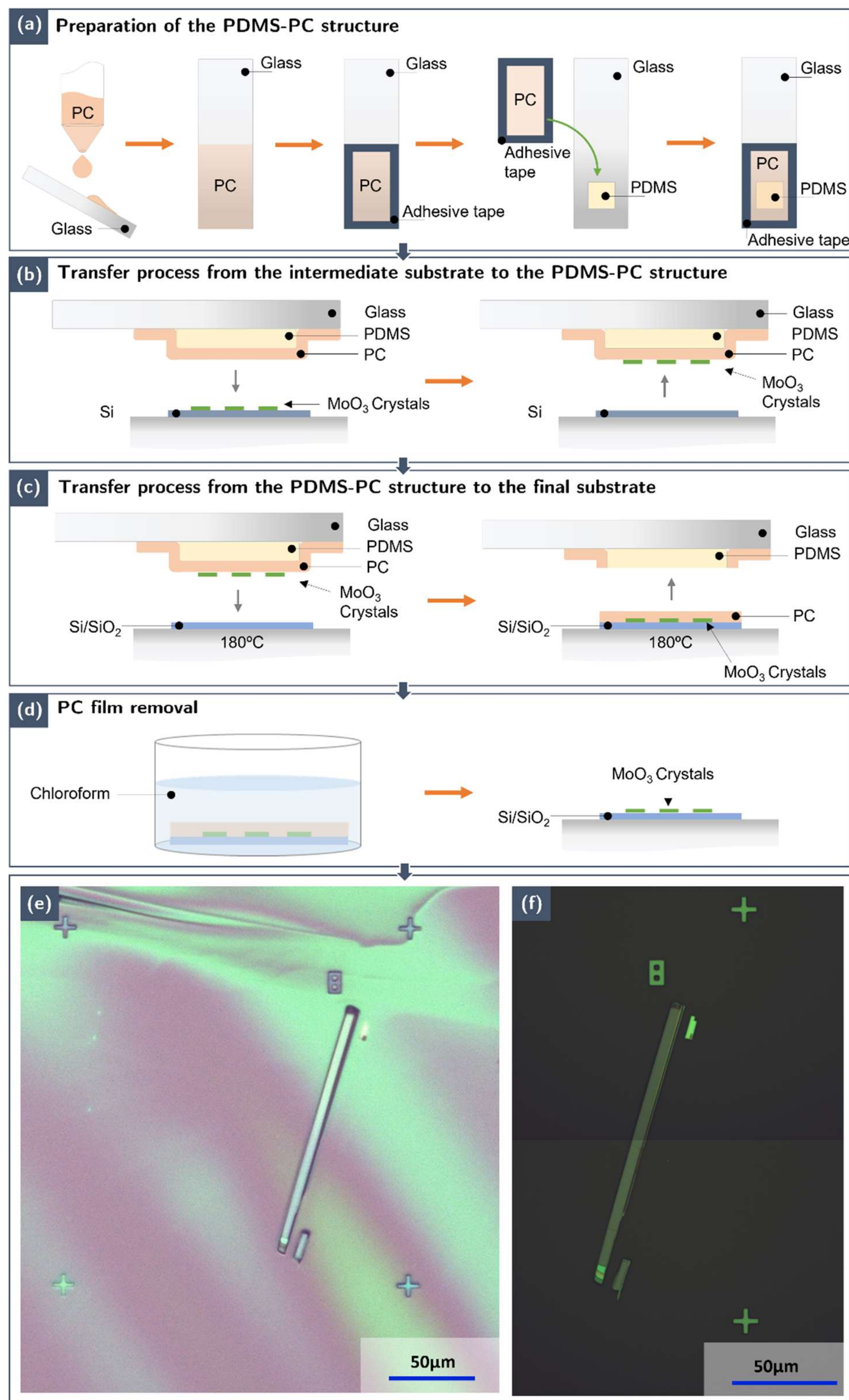

Figure S8 - (a) Schematic of the production process of the PC film. (b)-(d) Schematic of the transfer process of the α-MoO_3 exfoliated crystals from the intermediate Si substrate to the final substrate (Si/SiO_2), using a PDMS-PC structure. (e) and (f) Images obtained by optical microscopy of an α-MoO_3 exfoliated crystal after transferring to the final substrate, and after the cleaning process for the removal of the PC film, respectively.

6. Microfabrication process

The microfabrication process for producing α-MoO_3 FET devices with a BGTC geometry is divided in 5 distinct steps: (1) substrate preparation; (2) exfoliation of bulk MoO_3 crystals to obtain nanocrystals with a few hundred nanometers of thickness, which will form the FET channel; (3) transfer of the nanocrystals to the final substrate (Si/SiO_2); (4) deposition of the drain and source contacts on top of the exfoliated crystals; and (5) deposition of the gate contact on the backside of the substrate (corresponding to the p-type Si). Figure S9 summarizes the key steps involved in incorporating α-MoO_3 exfoliated crystals into FET devices.

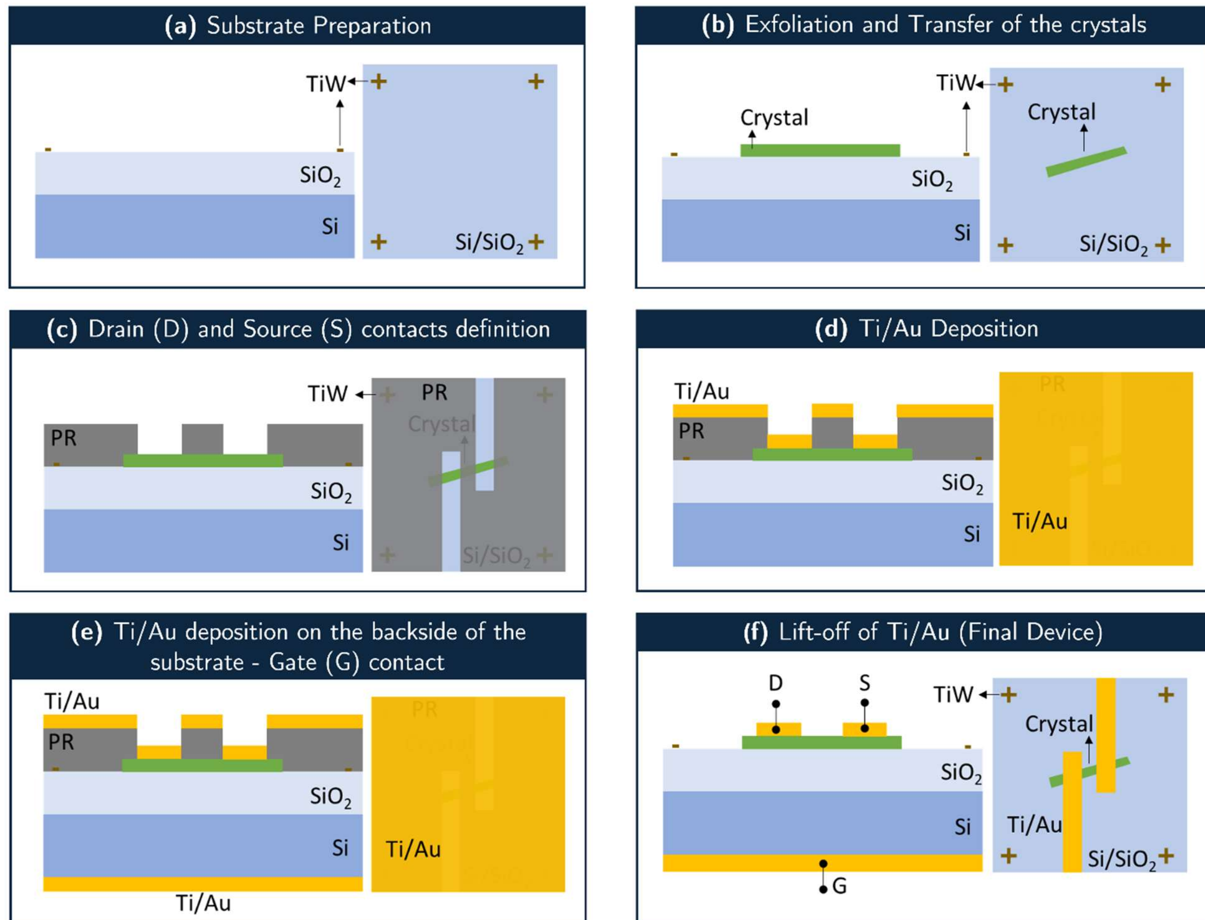

Figure S9 - Summary of the main microfabrication steps used in the incorporation of α-MoO_3 exfoliated crystals into FET devices. The letters D, S, and G in (f) indicate the drain, source, and gate electrical contacts, respectively. PR layer in the schematics corresponds to photoresist layer.

In the first step - Figure S9(a) - small cross-shaped marks were created at specific positions on the final substrate. These marks were used as reference points to determine the positions of the crystals on the substrate and, consequently, the positions of the drain and source contacts on top of them. This approach was adapted from the work carried out by D. Verheij et al.[53], where a similar process was used to identify the position of GaN microwires that were randomly deposited on Si/SiO_2 and sapphire substrates. To create these reference marks, a 150 Å thick TiW layer was deposited on a 6-inch Si/SiO_2 wafer (p-doped Si substrates with 300 nm of SiO_2 deposited on top) using magnetron sputtering in the Nordiko 700 machine. The TiW deposition was performed under the following conditions: $\emptyset_{Ar} = 49.9\ sccm$, $\emptyset_{N_2} = 9.9\ sccm$,

$p = 2.9\ mTorr$, $P = 0.5\ kW$, $U = 416\ V$ and $I = 1.22\ A$. After deposition, the shape of the marks was defined by photolithography, using the Direct Write Laser (DWL) II from Heidelberg Instruments (HeCd laser, λ = 442 nm). The mask, shown in the middle and right side of Figure S10, was exposed 32 times on a 1.45 µm thick positive photoresist, following the pattern represented on the left side of Figure S10. The mask is composed of four quadrants, each containing a square matrix of 12 by 12 cross-shaped marks – middle of Figure S10. As shown on the right side of Figure S10, each set of four crosses, which define a square, is labelled with a number.

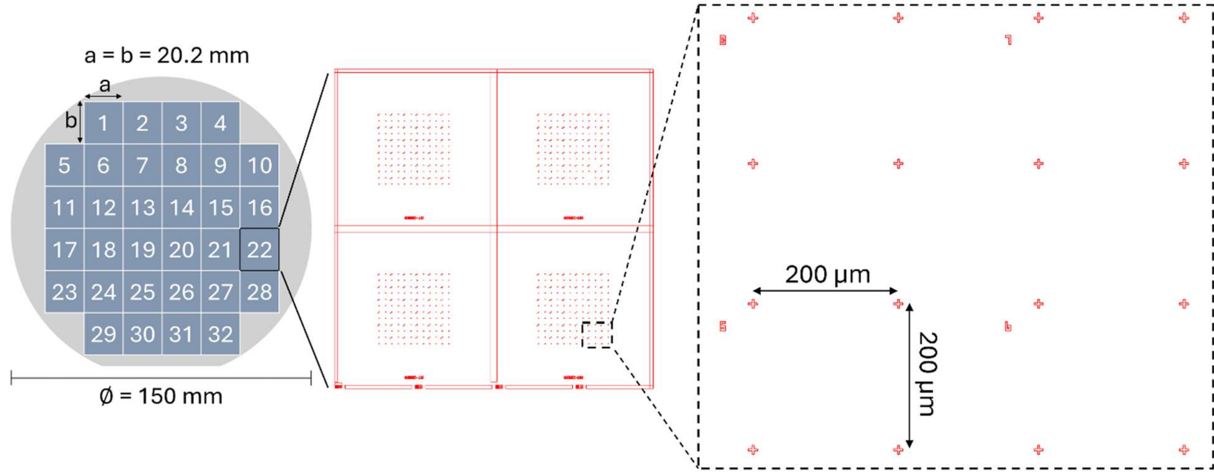

Figure S10 - (Left) Representative scheme of the map used in the photolithography process to define the TiW marks. (Middle and Right) Mask with the defined marks, designed in AutoCAD software and used in the photolithography process.

Following the photolithography process, ion milling etching was performed for 200 seconds at an angle of 60 degrees, using the Nordiko 3600 machine ($\emptyset_{Ar} = 14.7\ sccm$, $p = 1.19 \times 10^{-4}\ Torr$, $P_{Forward} = 179\ W$, $P_{Reverse} = 2\ W$ $U_{Grid_1} = 743\ V$, $I_{Grid_1} = 104\ mA$, $U_{Grid_2} = -347\ V$ and $I_{Grid_2} = -3\ mA$). Then, the photoresist was removed by immersing the Si/SiO_2 wafer in microstrip and placing it in an ultrasonic bath at a temperature of 65°C for 2 hours. The final result is shown in Figure S11, where it is possible to observe the 6-inch wafer after the etching process and the removal of the photoresist – Figure S11(a), as well as an image of the defined TiW marks – Figure S11(b). Finally, each die was individualized using the Disco DAD 321 cutting machine, to obtain individual substrates of 20.2 × 20.2 mm^2, with the TiW marks defined. These were the substrates used in the following steps.

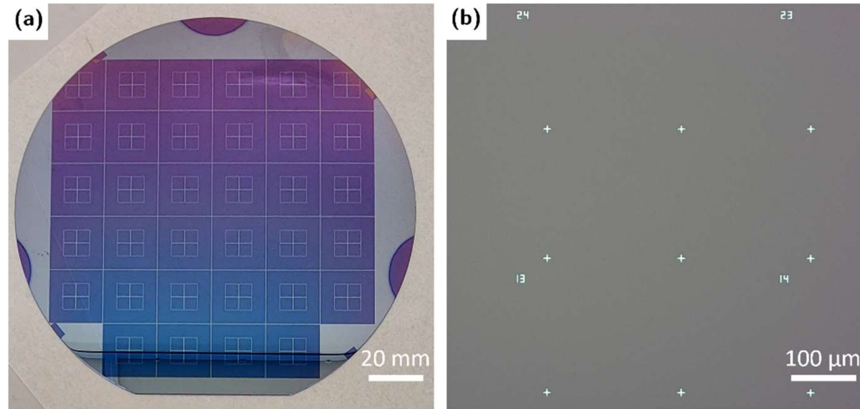

Figure S11 - (a) 6-inch Si/SiO_2 (300 nm) wafer after the entire microfabrication process, performed to define and deposit the TiW marks. (b) Image obtained by optical microscopy of the final TiW marks.

Once the TiW marks on the Si/SiO_2 substrates were defined – Figure S9(a) - the next step consists of exfoliating and transferring the crystals onto them - Figure S9(b) - following the procedure described in Section 5 and in Section 4.1 of the main manuscript. Using the TiW marks to locate the exfoliated crystals on the substrates, the positions of the drain and source contacts for each crystal were determined. The drain/source contacts were patterned on top of the crystals through a photolithography process - Figure S9(c), which included a pre-development step to facilitate the lift-off process after metal deposition. To minimize the degradation of the crystals caused by the developer exposure – see Section 7 for more information - the development time was reduced from the standard 60 seconds to 30 seconds. After photolithography, a 200/1000 Å Ti/Au layer was deposited by magnetron sputtering using the Alcatel SCM 450 machine - Figure S9(d). At the end of the deposition, the backside of the substrates was carefully cleaned with acetone and isopropanol. The samples were then placed back into the Alcatel SCM450 machine for the deposition of the gate contact, consisting of a 50/800 Å Ti/Au layer – Figure S9(e). The Ti layer was first deposited by DC sputtering ($\emptyset_{Ar} = 20\ sccm$, $P = 40\ W$, $p = 3.5\ mTorr$), followed by Au deposition via RF sputtering ($\emptyset_{Ar} = 20\ sccm$, $P = 20\ W$, $p = 3.5\ mTorr$). As the final step, a lift-off process was performed in acetone for 5 hours to remove the excess Ti/Au outside of the contact regions - Figure S9(f). This step was carried out at room temperature, without the use of ultrasounds. Two examples of the final FET devices obtained are shown in Figure 1(b)-(c) of the main manuscript.

7. Surface morphology of the MoO_3 exfoliated crystals

Figure S12(a) shows an AFM image of the surface of the MoO_3 exfoliated crystals after the entire microfabrication process, where several craters with a few nanometers in height, can be observed - Figure S12(b). These craters indicate the removal of material during the microfabrication process, likely due to the exposure of the crystals to the developer and/or photoresist. To minimize this degradation from developer exposure, the development time was reduced to 30 seconds, as detailed in Sections 5 and 6 and in Section 4 of the main manuscript. However, despite these efforts, some signs of degradation still persist on the crystal surface, likely contributing to the deterioration of the performance of the final devices.

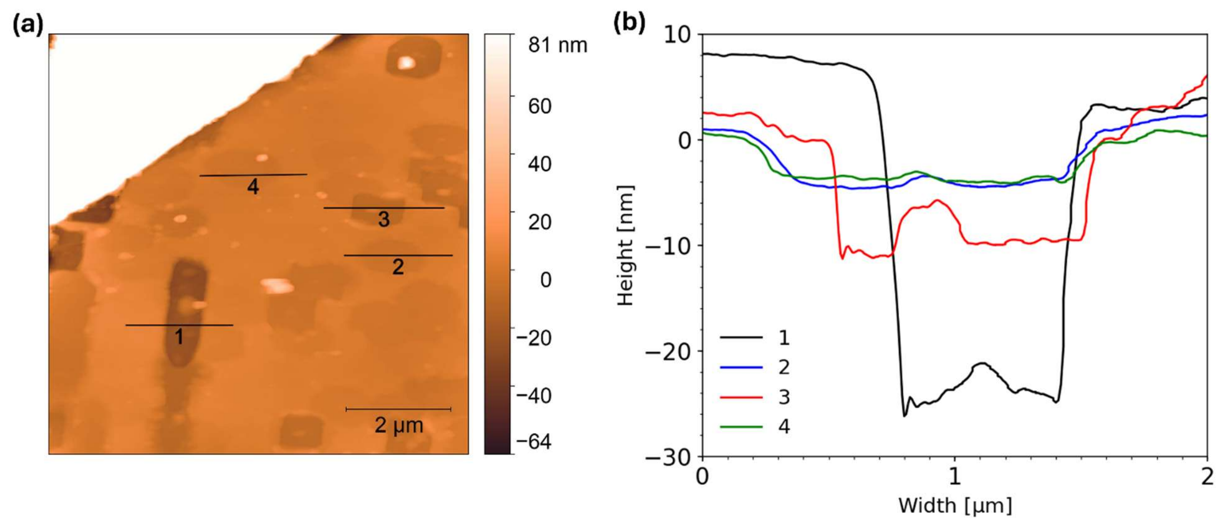

Figure S12 - (a) AFM image of the surface of an MoO_3 exfoliated crystal after the entire microfabrication process described in Sections 5 and 6 and in Section 4 of the main manuscript. **(b)** Height profiles of the craters 1-4 highlighted in (a).

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