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Electrical Characterization of Al/SiN_x:H/n and p-$In_{0.53}Ga_{0.47}As$ Structures by Deep-Level Transient Spectroscopy and Conductance Transient Techniques

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We have analyzed the influence of the dielectric composition and the post deposition rapid thermal annealing (RTA) treatment on the electrical characteristics of electron-cyclotron-resonance plasma-deposited SiN_x:H/n and p-$In_{0.53}Ga_{0.47}As$ interfaces. The devices are characterized by means of capacitance–voltage (C–V), deep-level transient spectroscopy (DLTS) and conductance transient analyses. Our results show that a simple cleaning step of the semiconductor surface prior to insulator deposition, and a post deposition RTA process are sufficient to obtain good-quality structures, the n-type being better than the p-type. In both cases, we conclude that a dielectric composition of $x = 1.50$ seems to be the best choice, and that the most adequate RTA temperature is between 500°C and 600°C.

KEYWORDS: interface states, insulator damage, $In_{0.53}Ga_{0.47}As$, plasma deposition, RTA, MIS, DLTS, conductance transients

1. Introduction

$In_{0.53}Ga_{0.47}As$ is a III–V ternary semiconductor, that has many interesting properties for optoelectronic device application. Because of its high mobility and electron velocity values, it is a very appropriate material for the fabrication of electronic devices such as a junction field effect transistor (JFET), a heterojunction bipolar transistor (HBT), and a modulation-doped field effect transistor (MODFET).[1,2] On the other hand, since it exhibits a 0.75 eV direct gap at room temperature, $In_{0.53}Ga_{0.47}As$ is useful for the development of integrated light emitters, modulators and detectors operating in the conventional communication transmission optical windows. Moreover, since this semiconductor has a lattice constant of 5.868 Å, it is grown lattice-matched to InP, whose higher gap (1.35 eV) is adequate to confine carriers and light in integrated optoelectronic devices.[3] $In_{0.53}Ga_{0.47}As$ can be epitaxially grown by means of such techniques as molecular beam epitaxy (MBE), metal organic vapour phase epitaxy (MOVPE) and chemical beam epitaxy (CBE).[4] Concerning the doping of $In_{0.53}Ga_{0.47}As$, ionic implantation (Si or Se for n-type, and Be, Mg, Zn or Cd for p-type)[5] is the most conventionally used method, and the results obtained for InP can usually be extended to $In_{0.53}Ga_{0.47}As$.

The $In_{0.53}Ga_{0.47}As$ surface, when air-exposed, does not present strong Fermi-level pinning as is usual in the GaAs surface, and its surface recombination velocity (5×10^3 cm s^{-1}) is also lower than that in GaAs (10^6 cm s^{-1}), making it a promising material for metal-insulator-semiconductor (MIS) device applications. However, in order to minimize interfacial defects, it is very important to realize a good coupling between $In_{0.53}Ga_{0.47}As$ and InP. On the other hand, it is necessary to use an insulator deposition technique that minimizes the semiconductor surface degradation during the insulator gate growth. The choice of the insulator is also an important issue in order to avoid insulator/semiconductor interface incompatibilities. There are reports on MIS devices with good-quality interfaces based on SiN_x:H/$In_{0.53}Ga_{0.47}As$ structures in which the insulator was deposited by the electron-cyclotron-resonance plasma method (ECR).[6,7] Indeed, this is a low-temperature deposition method (200°C or below) in which it is possible to reduce ion bombardment of the semiconductor surface during insulator deposition. However, ECR-deposited SiN_x:H films have a relatively high H-concentration, making them thermally unstable. The study of this instability is very important because rapid thermal annealing (RTA) treatment becomes necessary after ion implantation processes in order to recover surface crystallinity and to electrically activate the implanted atoms.

The aim of this study is to investigate the influences of dielectric composition and postdeposition RTA treatment on the electrical characteristics of ECR-deposited SiN_x:H/n and p-$In_{0.53}Ga_{0.47}As$ interfaces. This study will provide important information about the suitability of using ECR-deposited SiN_x:H layers as the gate dielectric in $In_{0.53}Ga_{0.47}As$ MIS devices.

2. Experimental

2.1 Sample description

$In_{0.53}Ga_{0.47}As$ epilayers of both n and p-type were grown by MOVPE lattice-matched to (100) InP and were supplied by Epitaxial Products International (EPI). We obtained n-type and p-type MIS-$In_{0.53}Ga_{0.47}As$ structures by directly depositing silicon nitride films on S-doped $In_{0.53}Ga_{0.47}As$ (6.6×10^{15} cm^{-3}) and Zn-doped $In_{0.53}Ga_{0.47}As$ (1.1×10^{16} cm^{-3}) substrates with the ECR plasma method. The gases we used to accomplish insulator deposition were N_2 and pure SiH_4, with four different values of the flux gas ratio, defined as $R = [N_2]/[SiH_4]$, ($R = 1$, 1.6, 5 and 9), which allowed us to obtain four different insulator compositions {$x = 0.97$ ($R = 1$), $x = 1.43$ ($R = 1.6$), $x = 1.50$ ($R = 5$) and $x = 1.55$ ($R = 9$)}. Substrates were heated at 200°C. The total pressure was kept constant at 0.6 mTorr during the deposition process, and microwave power was also kept constant at 100 W. In all cases, we adjusted the deposition time to obtain 500-Å-thick SiN_x:H films. Prior to dielec-

tric deposition, a simple cleaning step was applied: substrates were ultrasonically degreased in trichlorethylene, acetone and propanol and deoxidized in HCl : H_2O (1 : 3) for 1 min before drying in N_2. In our previous work,[7] we reported on small-frequency-dispersion, small-hysteresis and very low-interface-trap-density MIS structures that were obtained following this deposition procedure.

To study the effect of RTA temperature on interface quality, $SiN_{1.50}$:H/$In_{0.53}Ga_{0.47}As$ samples were subjected to Ar-atmosphere RTA processes for 30 s at temperatures between 400°C and 700°C. One sample of each type (n and p) was kept unannealed to be used as controls.

Next, Al dots (1.12×10^{-3} cm^2) were thermally evaporated through a shadow mask as gate electrodes. Finally, a 2500-Å-thick AuGe/Au (n-type substrate) or AuZn/Au (p-type substrate) back electrode was evaporated. Postmetallization annealing was performed in Ar atmosphere (300°C/20 min).

2.2 Electrical characterization

To study the interface quality of MIS structures, we applied the following techniques: capacitance–voltage (C–V), deep-level transient spectroscopy (DLTS) and conductance transient analyses.

C–V measurements were carried out at room temperature and at 78 K, putting the sample in a light-tight, electrically shielded box. The measurement setup involved a 1 MHz Boonton 72B capacitance meter and a Keithley 617 programmable electrometer. All the measurement runs were computer-controlled. Figure 1 shows room-temperature (a) and 78 K (b) C–V curves obtained for the unannealed Al/$SiN_{1.55}$:H/$In_{0.53}Ga_{0.47}As$ structure. Similar curves have been obtained for all samples. The C–V curves obtained at 78 K show a lower flat-band voltage displacement and a stretch-out with respect to room-temperature C–V ones, thus indicating that some traps in the material are frozen at low temperatures. However, both room-temperature and 78 K C–V curves obtained for all the samples clearly exhibit hysteresis, thus indicating that the interface state distribution follows the well-known disorder-induced gap-state (DIGS) model.[8,9] According to this model, the interface states are not only located at the interface but also distributed in both energy and space in the dielectric and in the semiconductor. The spatial extension of the disordered semiconductor region is very narrow, aproximatelly one to three monolayers. On the other hand, the disordered insulator region reaches more than 100 Å. Emission and capture of free electrons by states located in the insulator far from the interface can occur by means of tunnelling mechanisms. As emission and capture kinetics are slow and asymmetrical, the capacitance value depends on both the direction and the speed of the voltage variation and, thus, hysteresis effects are observed.

DLTS measurements were carried out, between 78 and 300 K, using the same 1 MHz Boonton 72B capacitance meter and an HP54501 digital oscilloscope to record capacitance transients. In these experiments, the Keithley 617 programmable electrometer was used together with an HP214B pulse generator to introduce the quiescent bias and the filling pulse, respectively. To obtain the interface trap distribution within the forbidden gap, the bias voltage was chosen so that the MIS capacitor was just at the limit between depletion and weak inversion. Also, a 200-μs-wide pulse that

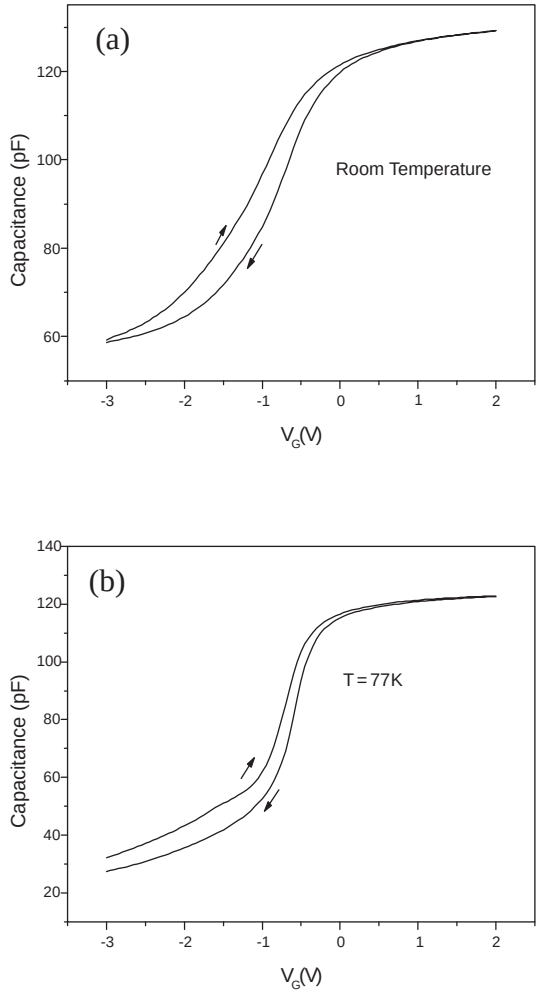

Fig. 1. 1 MHz-C–V curves obtained for the unannealed Al/$SiN_{1.55}$:H/$In_{0.53}Ga_{0.47}As$ sample: (a) room temperature, (b) 78 K.

was sufficiently high to drive the capacitors into accumulation was applied in order to fill all interface traps. The interface trap distribution (D_{it}) corresponding to one half of the forbidden gap (the upper half, E_c to midgap, in n-substrates, and the lower half, midgap to E_v, in p-substrates) was deduced from DLTS measurements by means of the expressions reported elsewhere,[10] by using an energy-independent capture cross section value of $\sigma_n = 1 \times 10^{14}$ cm^2, which is typically found in III–V semiconductor-based MIS structures.[11] Low-temperature transients provide information about interface states located near band edges, whereas high-temperature transients correspond to the emission of those located very near to the midgap. As is well known, the formation of the inversion layer leads to the formation of a dummy peak in the DLTS curves at high temperatures, which results in distortions of the true spectra, so the interface state density values corresponding to energy values near of midgap must be determined with caution.

We have also used the DLTS technique to detect the deep levels present in the semiconductor bulk.[12] In this case, the height of the pulse and the bias voltage are chosen so that the sample remains in strong inversion; therefore the interface states remain empty and do not contribute to the DLTS signal. The capacitance transients correspond in this case to changes in the occupation factor of the deep levels occurring when

bias pulses are applied.

As we will show bellow, the DLTS technique does not provide U-shaped interface state distribution having a minimum at or near the midgap, as is usually obtained by high- and low-frequency C–V techniques. Differences between high- and low-frequency C–V and DLTS results can be accounted for by the presence of slow states at the insulator/semiconductor interface, i.e., defects that are distributed away from the interface into the insulator. When the interface states are distributed in such a way, the electron emission and capture processes involve both thermal excitation and tunneling, producing a broad time constant dispersion, thus affecting the interface trap distribution obtained by high- and low-frequency C–V and DLTS measurements in different ways. As we have mentioned above, hysteresis observed in C–V curves should be related to this effect.

To further confirm the presence of such slow states, we performed conductance transient measurements of the devices. These transients appear over a wide temperature range (200 K to room temperature), and their shape is strongly dependent on the measurement frequency. Moreover, conductance transient measurements provide quantitative information about the disorder-induced gap states.[13,14] As has been published elsewhere,[15,16] from the experimental conductance transient, $G(t)$, we can obtain the DIGS state density (N_{DIGS}) as a function of the spatial distance to the interface (xc) and of the energy position, as follows:

$$N_{\mathrm{DIGS}} = \frac{\Delta G/\omega}{0.4qA} \tag{1}$$

$$x_{\mathrm{c}}(t) = x_{\mathrm{on}} \ln(\sigma_0 v_{\mathrm{th}} n_{\mathrm{s}} t) \tag{2}$$

$$E' - E(x_{\mathrm{c}}, t) = H_{\mathrm{eff}} + kT \ln\left(\frac{\sigma_0 v_{\mathrm{th}} N_{\mathrm{c}}}{\omega/1.98}\right) - kT\frac{x_{\mathrm{c}}(t)}{x_{\mathrm{on}}} \tag{3}$$

$$x_{\mathrm{on}} = \frac{\hbar}{2\sqrt{2m_{\mathrm{eff}}H_{\mathrm{eff}}}}, \tag{4}$$

where x_{on} is the tunnelling decay length, σ_0 is the carrier capture cross section value for $x = 0$, v_{th} is the carrier thermal velocity in the semiconductor, and n_{s} is the free carrier density at the interface. Finally, H_{eff} is the insulator-semiconductor energy barrier for minority carriers and E' means the carrier energy band edge at the insulator (E'_{c} for electrons and E'_{v} for holes).

3. Results and Discussion

3.1 SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ structures

Figure 2(a) shows the interface trap distribution, obtained by using DLTS, corresponding to unannealed Al/SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ samples, with x varying between 0.97 and 1.55. We can see that intermediate x values (1.43 and 1.50) provide better interfaces than the highest and lowest x values. Conductance transient measurements provide complementary information. In fact, in Fig. 2(b) we have plotted DIGS state density as a function of the distance from the interface and of the energy position measured from the insulator conduction band edge corresponding to the same samples. According to this figure, DIGS state density increases when x does. Hence, $x = 1.55$ seems to be the worst choice to improve the overall interface quality. In contrast, it is known that N-rich ECR SiN_x:H films exhibit optimum dielectric characteristics in terms of breakdown voltage and resistivity, as is commonly observed in III–V MIS devices.[17] The optimum dielectric characteristics can be explained in terms of the ratio of N–H bond to Si–H bond densities. Because N–H bonds have lower bond energy (4.05 eV)[18] than Si–H bonds (3.1 eV),[19] the probability of having dangling bonds is lower for N-rich than for Si-rich films, i.e., lattices having high nitrogen concentrations have higher electrical stability. Indeed, improved values of resistivity and breakdown field are obtained when x increases.[7] Hence, $x = 1.50$ and $x = 1.55$ are the most suitable values for improving the electrical properties of the insulator bulk. Thus, we have used $x = 1.50$ as the best choice for the trade-off between interface quality and insulator electrical properties.

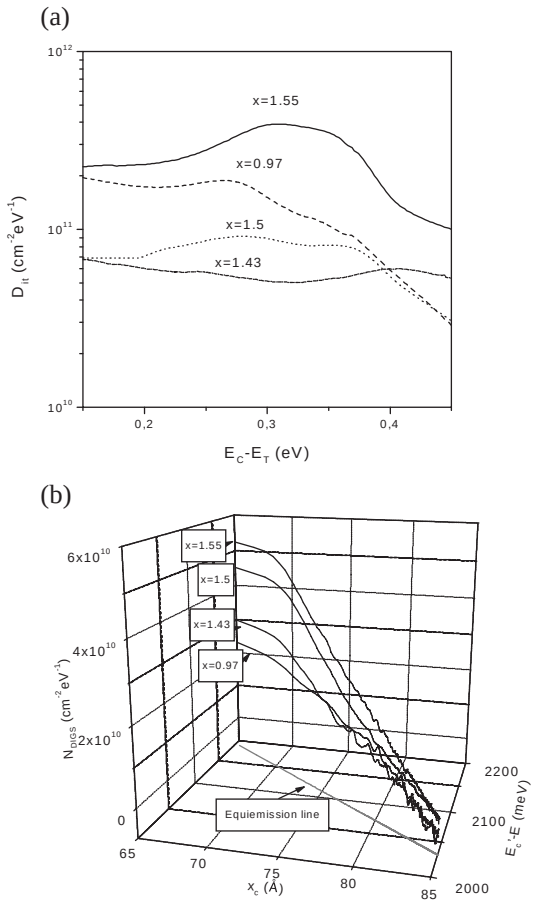

Fig. 2. Induced damage in unannealed Al/SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ MIS structures as a function of the insulator composition (x). (a) Interface state density measured by DLTS. (b) DIGS state density obtained from room-temperature–200 kHz conductance transient measurements.

Regarding the influence of RTA temperature on interface quality, in Fig. 3(a) we present DLTS results corresponding to samples with a dielectric composition of $x = 1.50$, unannealed and RT-annealed at different temperatures (400°, 500°, 550°, 600° and 700°C). These curves indicate that RTA temperatures between 500°C and 600°C decrease the interfacial state density of SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ samples, whereas annealing temperatures of 400°C and 700°C do increase it. On the other hand, conductance transient measurements [Fig. 3(b)] indicate that the evolution of DIGS state density with RTA temperature is exactly the opposite of that of interfacial state density, i.e., high and low temperatures diminish DIGS

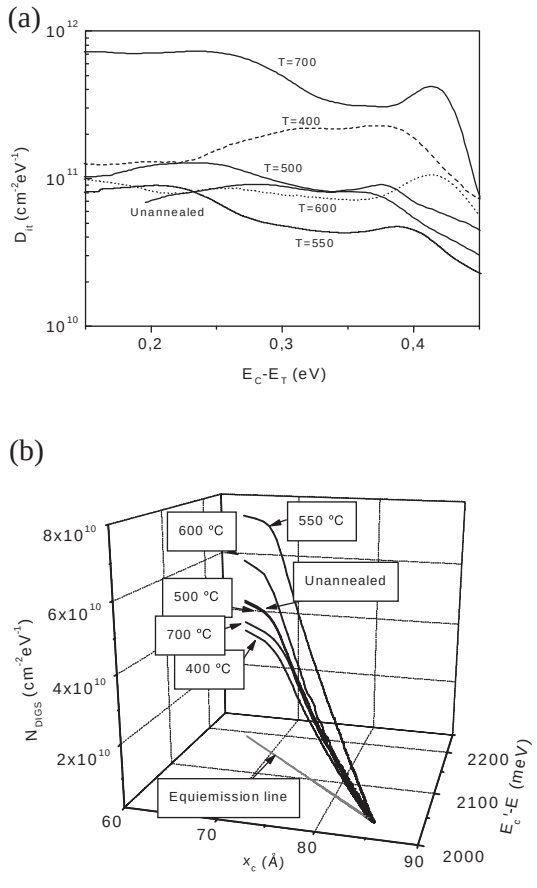

Fig. 3. Induced damage in $Al/SiN_{1.5}$:H/n-$In_{0.53}Ga_{0.47}As$ MIS structures at different RTA temperatures: (a) Interface state density measured by DLTS. (b) DIGS state density obtained from room-temperature–200 kHz conductance transient measurements.

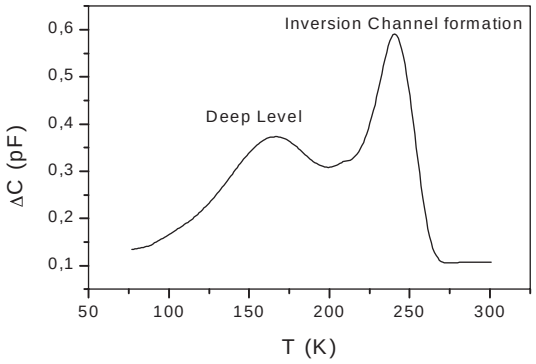

Fig. 4. Deep level located at 0.42 eV below the conduction band edge detected by DLTS for Al/SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ MIS structures.

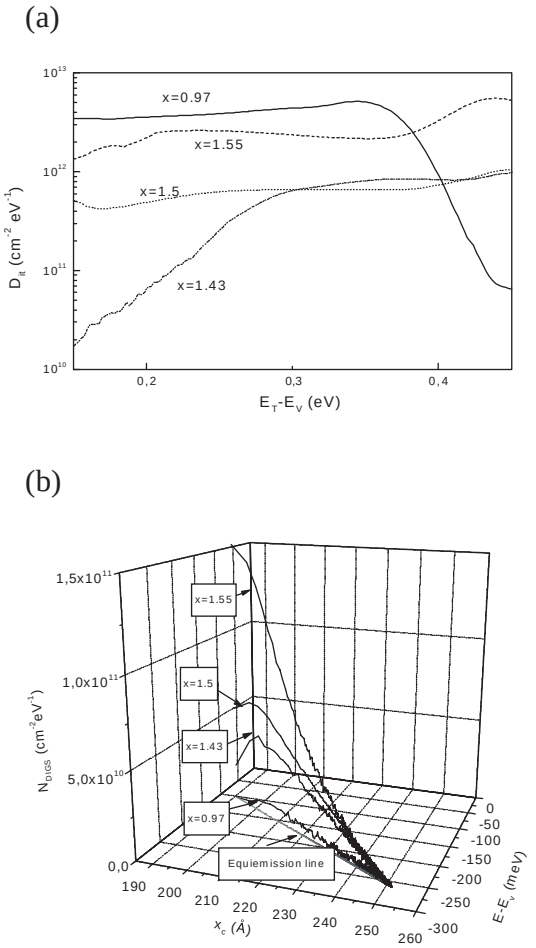

Fig. 5. Induced damage in unannealed Al/SiN_x:H/p-$In_{0.53}Ga_{0.47}As$ MIS structures as a function of insulator composition (x). (a) Interface state density measured by DLTS. (b) DIGS state density obtained from room-temperature–200 kHz conductance transient measurements.

state density, whereas intermediate temperatures increase it. This behaviour suggests some temperature activated defect exchange between the insulator and the interface. Moreover, previousbulk insulator resistivity ρ and breakdown field EB measurements[7] showed that between 500°C and 600°C, the maxima of ρ ($8 \times 10^{15}\,\Omega$cm) and E_B (7–8 MV cm^{-1}) are attained, and above 600°C, the insulator electrical properties sharply deteriorate. It is known that low-temperature annealing of SiN_x:H promotes a decrease of dangling bond density and a thermal relaxation and reconstruction of the lattice, both in the bulk and at the insulator-semiconductor interface, as was shown for SiN_x:H/n-InP[14,20–22] and SiN_x:H/n-Si capacitors.[23,24] In our case, temperature values between 500°C and 600°C are optimum. At temperatures above 600°C, the thermal stress on the structure is sufficiently high for the insulator and the interface properties to degrade rapidly.

Finally, from DLTS measurements, we have only detected a single deep level located at about 0.42 eV below the conduction band edge, for both unannealed and RT-annealed SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ samples, and it is probably related to a native center in the n-$In_{0.53}Ga_{0.47}As$ substrate. In the DLTS spectra of Fig. 4, corresponding to an emission time constant of 23.7 ms, we can observe the peak at 175 K related to this deep level.

Hence, we conclude that a simple cleaning step prior to the insulator deposition, and a postdeposition RTA process between 500°C and 600°C for 30 s are sufficient to achieve good-quality Al/SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ structures.

3.2 SiN_x:H/p-$In_{0.53}Ga_{0.47}As$ structures

In Fig. 5(a) we show DLTS results of the study of the insulator composition influence on the interface quality of SiN_x:H/p-$In_{0.53}Ga_{0.47}As$ structures. From this figure, we can conclude that extreme values of x (0.97 and 1.55) provide higher interface state density than intermediate values (1.43 and 1.50). On the other hand, from conductance transient

measurements [Fig. 5(b)] we conclude that higher DIGS state density values are obtained when a high x value (1.55) is used. Therefore, $x = 1.55$ seems to be the worst choice for improving the quality of SiN_x:H/p-$In_{0.53}Ga_{0.47}As$ interfaces. Taking into account, as we have said before, that N-rich films show optimum insulator electrical properties, such as resistivity and breakdown field, we can conclude that $x = 1.50$ is a good choice for the dielectric composition, in agreement with our results corresponding to SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ structures. However, we can see that D_{it} values obtained for p-structures are higher than those obtained for n-structures. This finding indicates that p-surface quality is worse than n-surface quality, and can be explained by taking into account the migration of Zn-dopant atoms to the surface in the case of p-structures.

In contrast, the influence of RTA temperature seems to be different for SiN_x:H/p-$In_{0.53}Ga_{0.47}As$ compared to that for SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ structures. Figure 6(a) shows the interface trap distribution obtained by DLTS for Al/$SiN_{1.5}$:H/p-$In_{0.53}Ga_{0.47}As$ samples unannealed and RT-annealed at temperatures of 400°, 500° and 600°C. The 700°C-DLTS curve is not shown because interface quality sharply degrades at temperatures above 600°C. We can see that RTA improves interface quality, and that interfacial state density decreases as temperature decreases. On the other hand, DIGS state density also decreases with RTA treatment, as we can see in Fig. 6(b). Therefore, the best RTA temperature seems to be 400°C. The differences observed between the n- and p-structures may be due to the fact that unannealed p-structures show higher D_{it} values than n-structures, as we have said before, and therefore a 400°C-RTA treatment is sufficient to promote a significant decrease of dangling bond density in the p-type structures, whereas in the n-type structures a temperature of about 500°–600°C is necessary. However, since resistivity and breakdown field reach their optimum values between 500° and 600°C, we can conclude that the optimum RTA temperature is 500°–600°C, in agreement with our results for n-type structures.

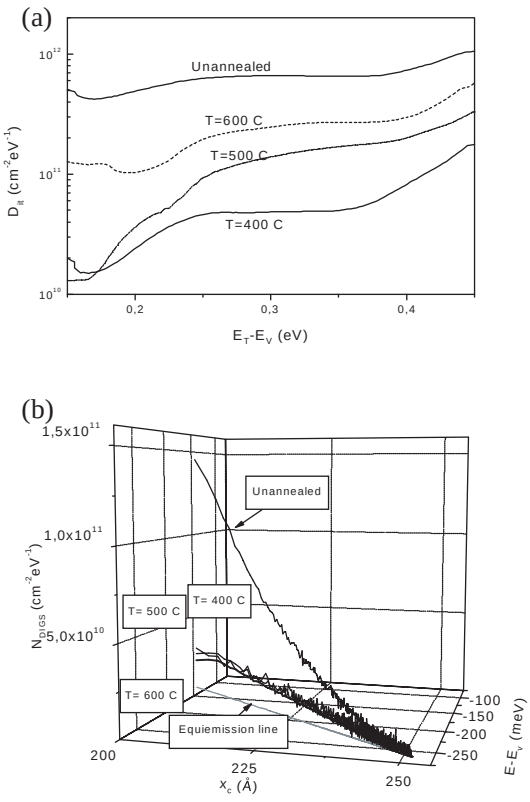

Fig. 6. Induced damage in Al/$SiN_{1.5}$:H/p-$In_{0.53}Ga_{0.47}As$ MIS structures at different RTA temperatures. (a) Interface state density measured by DLTS. (b) DIGS state density obtained from room-temperature–200 kHz conductance transient measurements.

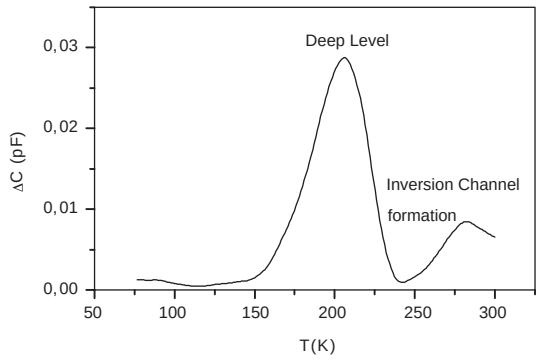

Fig. 7. Deep level located at 0.32 eV above the valence band edge detected by DLTS for Al/SiN_x:H/p-$In_{0.53}Ga_{0.47}As$ MIS structures.

For deep levels in the semiconductor substrate, in Fig. 7 we show the DLTS spectrum corresponding to an emission time constant of 18 ms. The presence of a maximum at a temperature of about 200 K is related to the existence of a deep level located at 0.32 eV above the valence band edge. This deep level, which has been previously observed by us in n^+p junctions fabricated on the same substrates, can be attributed to a native center in p-$In_{0.53}Ga_{0.47}As$.

4. Conclusions

We have carried out the electrical characterization of ECR *ex situ* deposited Al/SiN_x:H/n and p-$In_{0.53}Ga_{0.47}As$ structures using C–V, DLTS and conductance transient techniques. Our results show that excellent MIS structures have been obtained, and that better interface quality is achieved for n-type than for p-type capacitors, probably due to the absence of the migration of Zn-dopant atoms to the surface in the former case.

Regarding the dielectric composition, our experimental results indicate that $x = 1.50$ (corresponding to a gas flow ratio of $R = [N_2]/[SiH_4] = 5$) is the best choice for the insulator composition in order to obtain a good compromise between interface trap density and dielectric properties. On the other hand, we have observed that RTA treatment between 500° and 600°C after dielectric deposition clearly improves MIS quality, thus indicating that a decrease of dangling bond density, thermal relaxation and reconstruction of the lattice are promoted. Moreover, we have only detected deep levels associated with native centers in the semiconductor bulk, so we can conclude that ECR-CVD and RTA processes are sufficiently "soft" to be used in $In_{0.53}Ga_{0.47}As$-based MIS device fabrication.

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