Exploration of Ring Oscillator Based Temperature Sensors Network Accuracy on FPGA

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***Abstract*— During the last decades, technology scaling in reconfigurable logic devices enabled implementing complicated designs which results in higher power density and on-chip temperature. Since higher operating temperature of chips is a critical problem in electronics devices, thermal management techniques are highly required. To provide a thermal map of reconfigurable logic devices, a network of sensors is needed. In this work, a ring-oscillator-based temperature sensor is used to create a sensor network. Then, a design space exploration is done among several sensor networks with the various sensor configurations including different ring oscillator length, the number of sensors in the examined network and various sampling time. We propose three criteria for exploring and comparing the efficiency of sensors network based on the thermal overhead and also measurement accuracy and precision among plenty of configurations on the Virtex-6 FPGA.**

Keywords— Sensor network, Ring oscillator, Accuracy, Precision, Sampling time, Thermal overhead, FPGA.

I. INTRODUCTION

In the recent years, as transistors are shrinking in the reconfigurable embedded devices, there has been a noticeable increase in power consumption and especially in operating temperature. Since power consumption and temperature can interact with each other, the designers have to minimize the power consumption, the on-chip rising temperature and improve the performance and reliability of the system during the entire design flow [1].

Accurate thermal measurement techniques can improve the performance of chips particularly for multi-core system-on-chips (SoCs) [2]. To address these issues, the researchers must have a precise thermal map of chips to estimate and predict the die temperature in order to apply dynamic thermal management (DTM) techniques to maintain the operation of systems safe and reliable. In some modern field programmable gate arrays (FPGAs), i.e. Xilinx Virtex-5 and Virtex-6, there is one built-in thermal diode that gets the die temperature only in a fixed location (usually at the center of the die) [3], [4]. In the last years, the designers have paid a lot of attention to soft sensors. They have proposed different designs for soft sensors [5-17]. Some researchers utilize an array of temperature sensors based on a ring oscillator (RO). These sensors are reconfigurable and can be inserted or removed at run-time [5]. Also one of the most difficult challenges in the case of on-chip measurement is errors related to wire crosstalk and thermal noise. Hence, the accuracy and precision in soft sensors should be taken into account [11]. Design space exploration (DSE) can assist the designer to find an optimal configuration of the sensor network. In this paper, several platforms are implemented that differ in RO length and sampling time. We examine and evaluate the thermal overhead, the accuracy and precision. This work investigates the influences of different parameters on the examined sensors network.

The rest of the paper is organized as follows. Section 2 gives an overview on the related work. Section 3 presents the architecture of the measurement system. In section 4, basic parameters for evaluating the sensors network are illustrated. Experimental Results and analysis are discussed in section 5. Finally, in Section 6, the paper is concluded.

II. RELATED WORK

This section demonstrates the related work in temperature sensor designs, sensor calibration, array of thermal sensors and heat-generating techniques.

A. Temperature Sensor Designs

A thermal sensor based on an RO is constructed conventionally using an odd number of inverters in a loop and an AND gate for avoiding of counter overflow and reducing the self-heating effects. Also there is a counter that captures the oscillations of the RO at a fixed interval time, called as sample time or sample period, as depicted in Fig. 1.

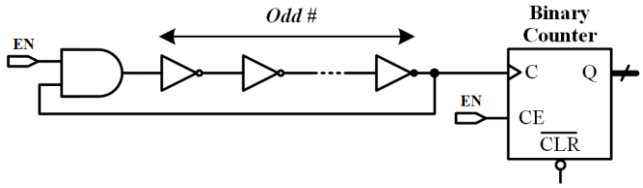

Fig.1. Conventional RO-based temperature sensor [15].

The number of inverters and interconnections delay defines the oscillation frequency as in (1):

$$f = \frac{1}{t_p} = \frac{1}{n \times t_D} \quad (1)$$

where t_p is the oscillation period, t_D is the propagation delay of one inverter, and n is the number of inverters in the loop.

Note that, the researchers usually use different types of counters, i.e., binary counter and residue number system (RNS) ring counter. The RNS ring counter is utilized by [7, 15], in order to make the sensor more compact. Also, the researchers design various sensors using different RO configurations. For instance, Payá-Vayá et al. propose a novel temperature sensor, which uses only 3 digital signal processor (DSP)-slices and one look-up table (LUT) on a Xilinx Virtex-6 FPGA [16]. In [11], the authors design a novel intra-chip physical sensor that relies on the setup and hold time conditions of a flip-flop on the Altera Cyclone II. The researchers in [15] introduce a fully digital temperature sensor that occupies 37.5% fewer resources compared to other compact design (i.e. [7]) and obtains 2.72 times more sensitivity.

B. Sensor Calibration

One of the most popular approaches for measuring the die temperature is to construct a temperature-dependent circuit, i.e., a ring oscillator and calibrate its output. Due to the fact that the oscillation frequency of an RO is temperature-depend, the system needs to calibrate the sensor to convert the measured frequencies to the corresponding temperature. Different calibration techniques are presented in the literature. Some designs are based on the built-in thermal diode [3], [4] which use the system monitor in Xilinx FPGAs and intellectual property (IP) cores in Altera FPGAs [18]. Among other alternative methods, some designers utilize external devices such as temperature probe, oven, and chamber which are applied as a reference for calibration [7], [9].

C. Sensors Network

For measuring and preparing an accurate thermal distribution on FPGA-based systems, an array of temperature sensors based on the RO is proposed by [1-5]. In [10], the authors design an array of 4×8 sensors to demonstrate the temperature gradients and finding hotspots. Zick and Hayes present a network with over 100 sensors for measuring variations in some parameters, such as delay and IR drop caused by switching activity [7]. A thermal sensing network that has been composed of 6×8 arrays of sensors is proposed by [19] to capture the on-chip thermal map using fuzzy clustering map.

D. Heat-Generating Methods

One of the most important challenges to measuring the on-chip temperature is the restriction on the temperature ranges. Agne et al. [20] introduce seven ways to make the high-tech FPGAs heat using available internal resources. In this paper, we use the heat generator circuit that has been designed in [20], i.e., the one-level LUT-based heater.

III. The Architecture of the Measurement System

The basic architecture of our sensors network platform is shown in Fig. 2. The system setup of all experiments consists of the main parts [15].

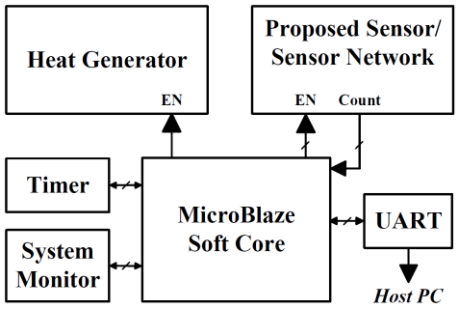

Fig. 2. Block diagram of the system architecture.

A. MicroBlaze Core

The MicroBlaze soft-microprocessor core that controls and manages all components and also run the software written in C for reading the sensors' data and activates/deactivates the heat generators. The MicroBlaze and all of its components operate at 100 MHz.

B. Array of Temperature Sensors

The array of temperature sensors is utilized in order to measure the temperature on different parts of the chip. The sensors are constructed using the binary counter and the RO. The construction of the RO includes a NAND gate and an even number of inverters as depicted in Fig. 3. Note that, the width of the binary counter is 15 bits.

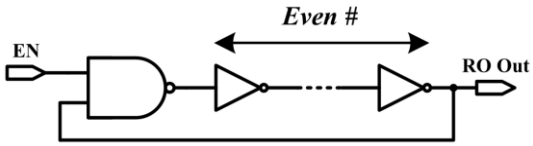

Fig. 3. Ring oscillator with an even number of inverters and a NAND gate.

C. Heat Generator Circuits

The heat generators are used to increase the on-chip temperature from 30°C to 60°C. The processor local bus (PLB) connects the heater circuit to the MicroBlaze. The heat generator circuit consists of 10,000 one-level LUT-based oscillator which enables the maximum toggling frequency [20]. Fig. 4 shows the schematic of the one-level LUT-based heater.

D. Timer

The timer IP core is instantiated in order to set a fixed sampling rate, allowing counting the number of clock cycles of the RO. In this work, we explore different sampling time from 40 µs to 120 µs.

E. System Monitor

The system monitor IP core supports the 10-bit resolution, 200 kilo-samples per second (KSPS) analog-to-digital converter (ADC) [4]. It is used to measure the temperature as well as core voltage values of the Xilinx Virtex-6 FPGA.

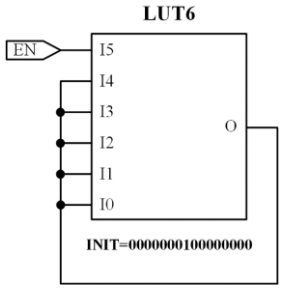

Fig. 4. Schematic of the one-level LUT-based oscillator heater.

F. Universal Asynchronous Receiver/Transmitter

In this paper, we use the universal asynchronous receiver/transmitter (UART) IP core for logging the sensors' values through RS232 to a host PC. It reports the temperature and core voltage values.

IV. Basic Parameters for Evaluating the Sensors Network

The sensors network enables to measure the temperature of different locations of a FPGA, however, it has area, power and temperature overheads. What is clear is that there are trade-offs between the accuracy of the sensors network and overheads. In this section, we define three main metrics to evaluate different designs of sensors network. These metrics help to explore better designs in large design space.

A. Thermal Overhead

Sensors impose a thermal overhead on the design when they are activated due to the RO oscillations which vary with respect to the length of the oscillator, sampling rate and sensor configuration. As a result, calculating the thermal overhead is one of the influential factors that the designer should take into account at the design stage.

In order to measure the thermal overhead, it is necessary that all sensors are initially deactivated and then the temperature increases by activating the heat generators from 30°C to 60°C. Assume it takes t_m seconds. The temperature after t_m seconds is called $T_{withoutnet}$. Then, the sensors and the heat generators are activated for t_m seconds. In this case the temperature after t_m seconds is called $T_{withnet}$ [15]. The thermal overhead T_{OH} is calculated as in (2):

$$T_{OH} = T_{withnet} - T_{withoutnet} \quad (2)$$

B. Accuracy

The measurement accuracy of a sensor or a sensor network is one of the most frequently used characteristics. To calculate the accuracy for the sensor network, the well-known root-mean-squared error (RMSE) is used to measure the error *E*. The RMSE is calculated as in (3):

$$E = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(P_i - A_i)^2} \quad (3)$$

where P_i is predicted value for data point *i*. A_i is actual value for the data point *i* and n is total number of data points.

C. Precision

The measurement precision illustrates the distribution of samples [11]. In this case, if the values are close together, then it has a high degree of precision. The measurement precision is calculated by the standard deviation in different sampling time. The standard deviation σ is defined as in (4):

$$\sigma = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(P_i - \mu)^2} \quad (4)$$

where *Pi* is values for the data point *i*, μ is mean of all values and *n* is total number of data points.

V. Experimental Results

In this section, we introduce the specification of the utilized FPGA and then discuss about calibration of the examined sensors network and analysis of the presented results.

A. System Setup

For experimental measurements, we used the Xilinx Virtex-6 ML605 FPGA development board. According to the design, the MicroBlaze soft-microprocessor operates at 100 MHz. In all our platforms, we partitioned the FPGA containing 160×239 slices into a regular grid of 10×9 tiles where each sensor is located at its center. The range of operating temperatures is from T_{min}=30°C to T_{max}=60°C. The design consists of 5 heat-generators with 10,000 LUTs and 140 sensors in the network. We implemented different platforms with various RO lengths and sampling rates.

B. Calibration Sensor Network

Due to the different nondeterministic routing algorithms and process variation in modern technologies, the calibration of the sensors should be done separately [8]. For this reason, in order to map the measured frequencies of the RO to chip temperature, i.e., the frequency to temperature converter equation (FTC) can be obtained by regression analysis. Using the Xilinx FPGA Editor tool, we fixed the routing in RO in order to minimize the routing effects. For estimating temperature based on counter values, we use a regression based model. To determine the regression coefficients, we design and implement a sensor as close as possible to the system monitor and record the values of counters for different temperatures. According to the coefficients that obtained, we calibrate other sensors. However, this method results in a high RMSE. To solve this issue, each sensor is calibrated individually. Using this approach the RMSE value improves about 50%.

The frequency of an RO is a function of temperature and supply voltage [21]. In this paper, a quadratic polynomial model is used to calibrate each sensor, according to equation (5):

$$T(x,y) = c_1 f^2(x,y) + c_2 {V_{DD}}^2 + c_3 f(x,y) \times V_{DD} + c_4 f(x,y) + c_5 V_{DD} + c_6 \quad (5)$$

where $f(x,y)$ and $T(x,y)$ are the frequency and the temperature of the sensor at location (x,y), respectively. V_{DD} is the core voltage, and c_i is the calibration coefficient. The RMSE is provided for every sensor in various platforms.

C. Evaluation Results and Analysis

To evaluate the performance of different configurations of the sensors network, 9 different experiments were performed and each experiment was repeated 5 times. In these experiments, we explore to study the effects of the RO length and sampling period on the important metrics (thermal overhead, accuracy and precision). In all experiments, the width of the 15-bit counter and the number of sensors (140) are constant. Using the Xilinx FPGA PlanAhead tool, the floorplan of the sensors' placement with 5 heat generators and 140 sensors was designed. The layout of the examined sensor network is shown in Fig. 5.

According to equation (2), we calculate the thermal overhead for different configurations of sensors in the network in the range of 30°C to 60°C. The results are shown in Table I. As expected, with the increase of the RO length, the thermal overhead is reduced. In the other words, thermal overhead increase due to higher oscillation frequency of the shorter RO. For example, 7-stage RO in 80 µs generates heat about 27% more than 17-stage RO with the same sampling period. It can be seen that the difference of the RO frequency between the slowest (248.925 MHz) and the fastest frequency (268.425 MHz) that occur in the maximum (60°C) and the minimum (30°C) of temperature respectively, in 7-stage RO in 40 µs reaches about 20 MHz. As a result, each sensor generates the different amount of heat [15]. It should be considered to get accurate results in thermal overhead, the mean of oscillation frequencies of ROs [15]. Fig 6 demonstrates the average oscillation frequency of 9 different designs.

To study the influences of the sampling time on the networks efficiency, we tried three different sampling rates including: 40 µs, 80 µs and 120 µs. We found that thermal overhead metric increases due to higher sampling time. Because in higher sampling period, the RO will be active longer and counts more that it results more thermal overhead, and also this affects to increase the length of the counter. For instance, respect to results presented in Table, it can be compared to the sensor network with 7-stage ROs in 40 µs, the T_{OH} is 20.7% less than the sensor network with the same length but in 120 µs.

In [15], the authors implement 35 sensors in a network and in presented work the number of sensors is 140. We increase the number of sensors by 4 times, since the size of the Virtex-6 is about 5 times larger than the Virtex-5 FPGA that is utilized by [15]. According to Table II, there is a more temperature overhead in Virtex-5 LX50T, 65-nm process technology, compared to the Virtex-6 ML605, 40-nm process technology. For example, in the RO with 7 stages, the thermal overhead reduces about 88%. Also in the experiments, the fan of the Virtex-6 FPGA cooling element

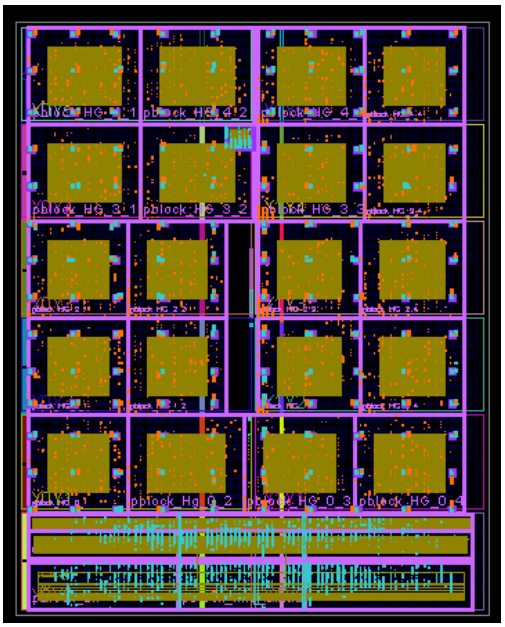

Fig 5. The floorplan of the sensor's placement (140 sensors) as shown from Xilinx PlanAhead tool.

Table I. RO-based temperature sensor designs in the network for variant RO length and sampling time in terms of the thermal overhead.

RO Length	Sampling Time (µs)	T_{OH} (°C)	Accuracy	Precision
7	40	0.112	4.09	0.787
	80	0.148	3.972	0.748
	120	0.319	4.098	0.668
17	40	0.087	4.091	0.718
	80	0.108	3.918	0.643
	120	0.089	3.48	0.572
31	40	0.0078	3.697	0.657
	80	0.079	3.466	0.588
	120	0.09	3.185	0.563

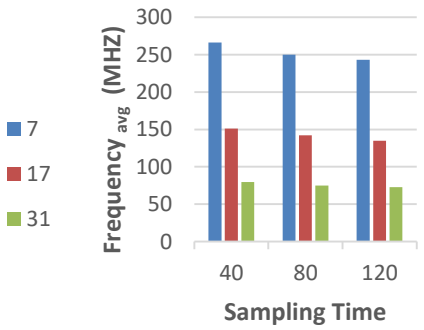

Fig 6. Average oscillation frequency of 140 sensors.

Table II. Comparison between thermal overhead in 40 µs with different stages in RO in Virtex-5 and Virtex-6.

RO length	Virtex-5 LX50 T [15]	Virtex-6 ML605
7	1	0.112
17	0.763	0.087
31	0.548	0.078

is active. It seems that even with a 4X increase in the number of sensors, due to the larger area of the Virtex-6, being activated the fan and technology variation, there is less overhead in Virtex-6.

In [13] has been suggested that with increasing the number of RO's stages, the sensor sensitivity becomes higher. It has proven that for a single sensor with different stages, the precision is better for shorter ROs. We extend this concept for a network of sensors in the Virtex-6.

In order to measure the accuracy of different sensor network, according to (3), the temperature of each sensor is estimated at 30°C to 60°C and the total RMSE is reported for all 140 sensors. By calculating the average RMSEs of all sensors, the error the network can be calculated in MATLAB, as depicted in Fig 7.

To calculate the precision of the network, after sensor calibration, we obtain a standard deviation of the estimated temperatures for 140 sensors in different sampling period at a certain temperature (55°C) using equation (4) that P_i is the estimated temperature of *i*th sensor and *n* is 140. Fig. 8 shows the comparison results between the standard deviation of sensors network against measurement duration.

As shown in Figs. 7 and 8, the accuracy and precision improve for higher sampling periods. One of the results that can be obtained from these graphs is that for the fewer number of stages and the lower sampling rates, higher RMSE and the standard deviation can be obtained. For instance, 7-stage RO in 40 µs sampling period, we see an increase of 10% in RMSE and 16% in standard deviation compared to 31-stage RO with the same sampling period. Also, the RO with 31-stage in 120 µs has the least error and

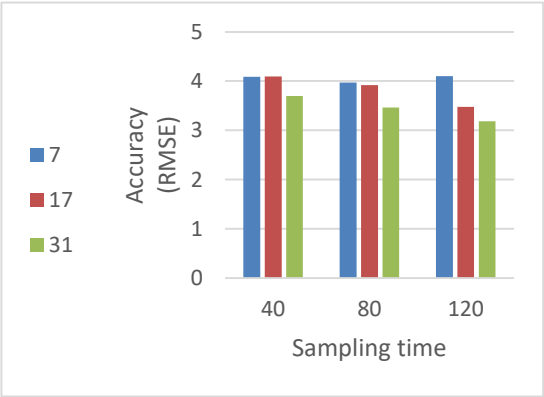

Fig 7. Accuracy of temperature measurements of sensors network.

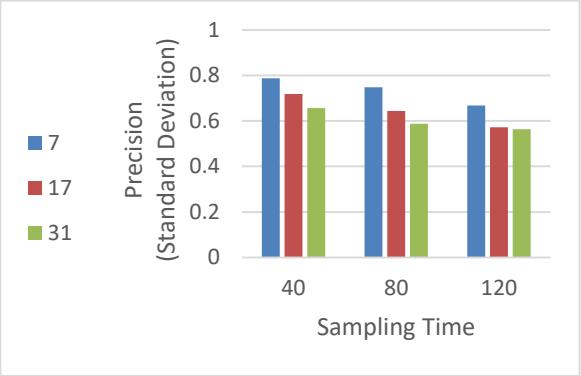

Fig 8. Precision of temperature measurements of sensors network (at 55°C).

standard deviation.

VI. Conclusion and Future Work

To measure the behavior of the on-chip temperature of the FPGA at runtime, a sensors network is needed. We presented an array of 140 sensors with different configurations. In comparison with [15], it has been found that due to changes in process technology, the thermal overhead has reduced about 88%. One of the significant metrics in thermal overhead, accuracy and precision is the sampling period. In our experiments, the system with higher sampling rate and RO length has more precision and accuracy and also thermal overhead. However, it is seen in some sampling rates (i.e. 80 µs) that there is opposite results due to alternation in frequency oscillations of the RO. These experiments show that the process variation plays a more significant role than routing among state-of-the-art technologies. Although, increasing the sampling time and the counter's width, more thermal overhead and accuracy are expected.

In the future work, we intend to consider and implement the platforms with different configurations for the counters and ROs. Particularly in modern FPGAs with new technologies, the raising the sampling period (i.e. about millisecond) results the higher counter width that can have a significant effect on increasing the accuracy and thermal overhead.

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