UNIVERSIDAD COMPLUTENSE DE MADRID
FACULTAD DE INFORMÁTICA

TESIS DOCTORAL

Analysis of the Effects of Natural Radiation on Commercial-Off-The-Shelf (COTS) Memories

Análisis de los Efectos Frente a la Radiación Natural en Memorias Comerciales

MEMORIA PARA OPTAR AL GRADO DE DOCTORA

PRESENTADA POR

Golnaz Korkian

DIRECTORES

Dr. Juan Antonio Clemente Barreira
Dr. Juan Carlos Fabero Jiménez

© Golnaz Korkian, 2023

UNIVERSIDAD COMPLUTENSE DE MADRID

Facultad de Informática

TESIS DOCTORAL

Analysis of the Effects of Natural Radiation on Commercial-Off-The-Shelf (COTS) Memories

Análisis de los Efectos Frente a la Radiación Natural en Memorias Comerciales

Memoria que presenta para optar al título de Doctora en Informática

PRESENTADA POR

Golnaz Korkian

D9BK - DOCTORADO EN INGENIERÍA INFORMÁTICA

Dirigida por

Dr. Juan Antonio Clemente Barreira

Dr. Juan Carlos Fabero Jiménez

Febrero 2023

Dedication

Dedicated to Him, who is a savior, whom the world is waiting for to establish love, mercy, justice, and peace.

And

To my parents

Acknowledgments

In the name of Allah, Most Gracious, Most Merciful

Read! In the Name of your Lord Who has created (all that exists). He has created man from a clot (a piece of thick coagulated blood). Read! And your Lord is the Most Generous. Who has taught (the writing) by the pen. He has taught man that which he knew not. (the Qur'an, Surah Al-'Alaq, verses 1-5)

Praise be to the Almighty God, who has given man thought and action by His grace so that he can explore, understand, and contribute to developing new knowledge. Everything I have is from him.

I wish to express my warmest gratitude to the following people; without their help and support, I was not able to complete my Ph.D. dissertation: First and foremost, I would like to express my deepest gratitude and appreciation to my honorable supervisor, Dr. Juan Antonio Clemente for his invaluable support and attempts to trigger interest in me in pursuing research, and for his guidance and patience over the past five years. Second, I am grateful to my advisors, Dr. Juan Carlos Fabero, Dr. Hortensia Mecha, and Dr. Francisco Javier Franco, for their constant care and attention while conducting my Ph.D. dissertation, which has been a way to illuminate the dark aspects of the research for me. All of you are the light of the darkness of thought.

Also, I would like to thank Dr. Hamid Noori, a professor at the Ferdowsi University of Mashhad in Iran, for guiding me to get the Ph.D. position at UCM and supporting me through everything.

Thanks to all Ph.D. committee members, Dr. Narciso Martí Oliet and Dr. Daniel Mozos, for providing me with guidance. I express my sincere gratitude to CNA, ILL, and PTB laboratories for collaborating with us in our experiments. My thanks go to Mr. Carlos Roa, technical support, for all the efforts that he has made for us. Also, I would like to thank all my colleagues at FDI, particularly Conserjería, for collaborating with me to come to the university on holidays and weekends.

Also, I would like to say my gratitude to my family and friends for their prayers, kindness, and encouragement. In the end, I hope that the scientific achievements of this research will be used to help Humanity for having a better world.

Abstract

In New Space, the need for reduced cost, higher performance, and more prompt delivery plans in radiation-harsh environments have motivated spacecraft designers to use Commercial-Off-The-Shelf (COTS) devices. This Ph.D. thesis investigates the behavior of state-of-the-art memories and FPGA manufactured in emerging technologies, including nv-SRAM, Ferroelectric Random-Access Memory (FRAM), Resistive Random-Access Memory (ReRAM), Magnetic Random-Access Memory (MRAM), and a 28-nm bulk Xilinx Artix-7 FPGA against radiation effects. Radiation-ground tests were conducted under 15-MeV and 1-MeV protons, thermal, and 14.8/14.2-MeV neutrons, leading to various categories of radiation effects.

Experimental results will be presented and discussed with the CY14V101QS and CY15B101J nv-SRAMs, the CY15B102Q and CY15B104Q FRAMs (manufactured by Infineon Technologies), the MB85AS4MT and MB85AS8MT ReRAMs (manufactured by Fujitsu), and the MR10Q010CSC and MR25H40CDF MRAMs (manufactured by Everspin), and the Artix-7 XC7A100T Xilinx FPGA.

The results obtained in nv-SRAMs and the Artix-7 XC7A100T FPGA indicate that these devices are susceptible to radiation effects. On the other hand, experimental results will show clear evidence of the robustness of bitcells manufactured using the rest of emerging technologies, including FRAMs, ReRAMs, and MRAMs against radiation, but at the same time, some susceptibility in these devices when working in dynamic mode. It also is well known that the angle of incidence of impinging particles against the surface of the operating devices has significant effects on their sensitivity. Thus, this thesis will discuss the sensitivity of the CY14V101QS nv-SRAM and the Artix-7 XC7A100T Xilinx FPGA and their dependency on the incident angle of impinging particles.

Finally, a modeling tool called MUSCA-SEP3 was used to predict the sensitivity of the Artix-7 XC7A100T Xilinx FPGA under thermal and fast neutrons, as well as the CY14V101QS nv-SRAM under 14.2-MeV neutrons. These predictions will be compared with experimental results issued from radiation-ground campaigns. The latter will show a good agreement with the predicted ones.

Resumen

En lo que se ha venido a llamar "Nuevo Espacio", la necesidad de reducir costes, aumentar el rendimiento y planes de entrega más rápidos en proyectos destinados a entornos sometidos a radiación han motivado que los diseñadores de naves espaciales utilicen dispositivos comerciales no diseñados específicamente para espacio (COTS, *Commercial Off The Shelf*). Esta tesis investiga sobre el comportamiento frente a los efectos de la radiación de FPGA y memorias disponibles en la actualidad que han sido fabricadas con tecnologías emergentes, como RAM estáticas no volátiles (nv-SRAM), RAM ferroeléctricas (FRAM), RAM resistivas (ReRAM), RAM magnéticas (MRAM) y una FPGA Artix-7 de Xilix con tecnología de 28 nm. Se han realizado experimentos de radiación en instalaciones terrestres con protones de energías de 15 y 1 MeV, así como con neutrones térmicos y con energías de 14.8 y 14.2 MeV, lo que ha provocado varios tipos de efectos. Se presentarán y discutirán los resultados experimentales para las nv-SRAM CY14V101QS y CY15B101J y las FRAM CY15B102Q y CY15B104Q, todas ellas fabricadas por Infineon Technologies; para las ReRAM MB85AS4MT y MB85AS8MT, fabricadas por Fujitsu, y para las MRAM MR10Q010CSC y MR25H40CDF de Everspin. Asimismo, se presentarán los datos obtenidos para la FPGA Artix-7 XC7A100T de Xilinx.

Los resultados que se han visto para las nv-SRAM y la FPGA Artix-7 XC7A100T indican que estos dispositivos son sensibles a los efectos de la radiación. Por otro lado, los experimentos muestran claramente que las celdas de memorias fabricadas con las otras tecnologías, esto es, FRAM, ReRAM y MRAM son muy robustas frente a la radiación aunque, al mismo tiempo, estos dispositivos son susceptibles de fallo al trabajar en modo dinámico. Además, se sabe que el ángulo de incidencia de la radiación influye significativamente en la sensibilidad de los dispositivos. De este modo, en esta tesis se hablará de la susceptibilidad de la memoria nv-SRAM CY14V101QS y de la FPGA Artix-7 XC7A100T y su dependencia con el ángulo de las partículas incidentes.

Por último, se ha usado la herramienta de modelado MUSCA-SEP3 para predecir el comportamiento de la FPGA Artix-7 XC7A100T sometida a neutrones térmicos y rápidos, así como el de la memoria nv-SRAM CY14V101QS bajo neutrones de 14.2MeV. Estas predicciones se comparan con los resultados de las campañas de radiación en las instalaciones, mostrándose una buena concordancia entre las predicciones y los resultados experimentales.

Contents

Abstract vi

Resumen vii

List of figures xiv

List of tables xvi

Abbreviations xvii

1 Introduction 1

1.1 New Space 1

1.2 COTS devices in New Space 1

1.3 Objectives of this thesis 2

2 Radiation environments and effects on electronic systems 5

2.1 Radiation Environments 5

2.1.1 Radiation environments for New Space 6

2.1.2 Atmospheric neutrons 9

2.1.3 Terrestrial radiation sources 10

2.2 Interaction of Radiation with Matter 10

2.3 Useful concepts for radiation experiments 13

2.4 Radiation Effects 15

2.4.1 Cumulative effects 16

2.5 Single Event Effects (SEEs) 17

2.5.1 Single-Event Transients (SETs) 18

2.5.2 Single-Event Upsets (SEUs) 18

2.5.3 Single-Bit Upsets (SBUs), Multiple-Bit Upsets (MBUs) and Multiple-Cell Upsets (MCUs) 19

2.5.4 Single-Event Functional Interrupts (SEFIs) 19

2.5.5 Single-Event Latchups (SELs) . . . 20
2.5.6 Single-Event Burnouts (SEBs) . . . 20
2.5.7 Single-Event Gate Ruptures (SEGRs) . . . 20

3 Memory devices and FPGAs **21**
3.1 General Principals . . . 21
3.1.1 Volatile vs. non-volatile memories and memory hierarchy . . . 21
3.1.2 Memory architecture of Solid State Storages (SSS's) . . . 22
3.1.3 Memory operation . . . 23
3.2 Memory cell technologies . . . 24
3.2.1 Static Random-Access Memories (SRAMs) . . . 24
3.2.2 SRAM-based Field Programmable Gate Arrays (FPGAs) . . . 26
3.2.3 Non-Volatile Static Random-Access Memories (NV-SRAMs) . . . 27
3.2.4 Ferroelectric Random-Access Memories (FRAMs) . . . 28
3.2.5 Magnetoresistive Random-Access Memories (MRAMs) . . . 32
3.2.6 Resistive Random-Access Memories (ReRAMs) . . . 34
3.3 Communication protocols . . . 37

4 Experimental setup **39**
4.1 Selected devices and test setups . . . 39
4.1.1 nv-SRAM (CY14V101QS) . . . 39
4.1.2 nv-SRAM (CY14B101J) . . . 40
4.1.3 FRAMs (CY15B102Q and CY15B104Q) . . . 41
4.1.4 MRAMs (MR10Q010CSC and MR25H40CDF) . . . 41
4.1.5 ReRAMs (MB85AS4MT and MB85AS8MT) . . . 42
4.1.6 Artix-7 XC7A100T FPGA . . . 43
4.2 Test methods . . . 43
4.3 Test facilities . . . 45
4.3.1 GENEPI2 facility at the LPSC . . . 45
4.3.2 Cyclotron at the CNA . . . 46
4.3.3 Tandem laboratory at the CNA . . . 47
4.3.4 TENIS facility at the ILL . . . 47
4.3.5 PTB Ion Accelerator Facility (PIAF) . . . 49
4.4 Data processing . . . 50
4.4.1 Extracting SBUs and MCUs from a large set of results . . . 50

4.4.2 Estimating the number of "false" multiple events by accumulation of simpler ones 51

5 Test results and discoveries **54**

5.1 Infineon nv-SRAM (CY14V101QS): Experimental results and discussion 54

5.1.1 CY14V101QS: Experimental results under 14.2-MeV neutrons 54

5.1.2 CY14V101QS: Experimental results under 15.3-MeV protons 58

5.1.3 CY14V101QS: Experimental results under thermal neutrons 59

5.1.4 CY14V101QS: Comparison of taken results under 14.2-MeV neutrons, 15.3-MeV protons, and 25-meV thermal neutrons 60

5.1.5 CY14V101QS: Discussion of experimental results 62

5.2 Infineon nv-SRAM (CY14B101J): Experimental results and discussion 68

5.2.1 CY14B101J: Experimental results under 15.3-MeV protons 68

5.2.2 CY14B101J: Experimental results under thermal neutrons 70

5.2.3 CY14B101J: Experimental results under 14.8-MeV neutrons 71

5.2.4 CY14B101J: Discussion of experimental results 72

5.2.5 Comparison of taken results of the CY14V101QS and CY14B101J memories with each other 73

5.3 Infineon FRAMs (CY15B102Q and CY15B104Q): Experimental results and discussion 74

5.3.1 CY15B102Q and CY15B104Q: Experimental results under 15.3-MeV protons 74

5.3.2 CY15B102Q and CY15B104Q: Experimental results under 1-MeV protons 77

5.3.3 CY15B102Q and CY15B104Q: Experimental results under thermal neutrons 78

5.3.4 CY15B102Q and CY15B104Q: Experimental results under 14.8-MeV neutrons 79

5.3.5 CY15B102Q and CY15B104Q: Discussion of experimental results 79

5.4 Fujitsu ReRAMs (MB85AS4MT and MB85AS8MT): Experimental results and discussion 81

5.4.1 MB85AS4MT and MB85AS8MT: Experimental results under 1-MeV protons 81

5.4.2 MB85AS4MT and MB85AS8MT: Experimental results under thermal neutrons 82

5.4.3 MB85AS4MT and MB85AS8MT: Experimental results under 14.8-MeV neutrons 83

5.4.4 MB85AS4MT and MB85AS8MT: Discussion of experimental results . . . 83
5.5 Everspin MRAMs (MR10Q010CSC and MR25H40CDF): Experimental results and discussion . . . 85
5.5.1 MR10Q010CSC and MR25H40CDF: Experimental results under thermal neutrons . . . 85
5.5.2 MR10Q010CSC and MR25H40CDF: Experimental results under 14.8-MeV neutrons . . . 85
5.5.3 MR10Q010CSC and MR25H40CDF: Discussion on experimental results . 86
5.6 Artix-7 XC7A100T FPGA: Experimental results and discussions . . . 87
5.6.1 Artix-7 XC7A100T FPGA: Stages to run each test . . . 87
5.6.2 Artix-7 XC7A100T FPGA: Extraction of the bitflips . . . 88
5.6.3 Artix-7 XC7A100T FPGA: Extraction of SBUs and MCUs . . . 89
5.6.4 Artix-7 XC7A100T FPGA: Experimental results under 14.2-MeV neutrons 90
5.6.5 Artix-7 XC7A100T FPGA: Experimental results under thermal neutrons 94
5.6.6 Artix-7 XC7A100T FPGA: Comparison between of experimental results under thermal neutrons with MUSCA-SEP3 predictions . . . 100
5.6.7 Artix-7 XC7A100T FPGA: Comparison between thermal and 14.2-MeV neutrons . . . 102

6 Conclusions and future work **103**
6.1 Summary of the thesis . . . 103
6.2 Future work . . . 106

7 List of publications **108**
7.1 Journals . . . 108
7.2 Conferences . . . 109

Bibliography **109**

List of Figures

2.1 Van Allen radiation belts [ESA11]. 8
2.2 The SAA region. 8
2.3 Types of orbits 9
2.4 Schematic view of an extensive air shower (EAS) 12
2.5 Illustration of the process of 10B fission 14
2.6 Deposited energy with a θ incident angle [ESA11]. 14
2.7 Bragg curve for protons. 16
2.8 SEE mechanisms 17
2.9 Classification of SEEs. 18
2.10 Explanation of an SRAM cell being struck by an ion and suffering an SEU. . . . 19
2.11 Explanation of MBU and MCU 19

3.1 Memory hierarchy. 22
3.2 Bit cell of an SSS. 23
3.3 Schematic of an SRAM memory cell composed of 6 transistors. 24
3.4 NV-SRAM Cell Architecture. 28
3.5 Structure of Perovskite ferroelectric crystal and two polarization states 29
3.6 Hysteresis curve of ferroelectric materials. 30
3.7 Structure of a) 1T1C and b) 2T2C ferroelectric memory cells. 30
3.8 Illustration of an MRAM cell 32
3.9 Schematic of a 1-transistor-1-resistor (1T1R) configuration 35
3.10 Virtual 16-bit circular shift register of an SPI communication 38
3.11 Example of a Quad SPI setup with single slave 38

4.1 Experimental setup for the CY14V101QS nv-SRAM. 40
4.2 Experimental setup of CY14B101J nv-SRAM and FRAMs. 41
4.3 Experimental setup for the MRAMs 42
4.4 Layout and schematic of the memory cells of the MB85AS4MT 43
4.5 GENEPI2 neutron source. 46

4.6 Setup for the irradiation of the nv-SRAM and FRAMs at the CNA. 47
4.7 Neutron energy spectrum on the TENIS at the ILL 48
4.8 Setup for the irradiation of the FPGA at the ILL. 48
4.9 Setup for the irradiation of the memory chips at the PIAF. 49
4.10 An interleaving model. 50
4.11 Dependence of the influence area of three flipped cells. 53

5.1 Beam incident angles that were tested for the CY14V101QS memory. 54
5.2 SBU cross-sections for the CY14V101QS memory under 14.2- MeV neutrons. . . 56
5.3 2-bit MCU cross-sections of the CY14V101QS memory under 14.2-MeV neutrons. 57
5.4 Experimental and estimated number of 2-bit MBUs for the CY14V101QS memory. 58
5.5 SBU cross-sections of the CY14V101QS memory under 15.3-MeV protons. . . . 59
5.6 SBU cross-sections of the CY14V101QS memory under thermal neutrons. 61
5.7 Comparison of static SBU cross-sections of the CY14V101QS memory 61
5.8 Comparison of MCU cross-sections from MUSCA-SEP3 vs. experimental results. 63
5.9 Emission angle frequency of secondary ions induced 64
5.10 Distribution of secondary ion range and alpha particles 66
5.11 Spherical coordinate system and passivation / metallization layers. 66
5.12 2-bit MCU cross-sections obtained with MUSCA-SEP3 from the CY14V101QS . 67
5.13 SBU cross-sections of the CY14B101J memory under 15.3-MeV protons. 69
5.14 SBU cross-sections of the CY14B101J memory under thermal neutrons. 70
5.15 SBU cross-sections of the CY14B101J memory under 14.8-MeV neutrons. 71
5.16 All static experimental SBU cross-sections of the CY14B101J memory. 72
5.17 All dynamic experimental SBU cross-sections of the CY14B101J memory. 72
5.18 Comparison of results of CY14V101QS and CY14B101J under 15.3-MeV protons. 73
5.19 Comparison of the CY14V101QS and CY14B101J memories under fast neutrons. 73
5.20 Comparison of the CY14V101QS and CY14B101J memories under thermal neutrons. 74
5.21 Errors observed on the CY15B102Q FRAM under 15.3-MeV protons 76
5.22 Observed SBUs on the CY15B104Q FRAM under thermal neutrons. 79
5.23 Observed errors on the CY15B102Q FRAM under 14.8-MeV neutrons. 80
5.24 Location of a cell with address in the Artix-7 XC7A100T FPGA. 90
5.25 Artix-7 XC7A100T FPGA and control system. 90
5.26 Obtained cross-sections for 14.2-MeV neutrons in the Artix-7 XC7A100T FPGA. 92
5.27 Observed shapes for 2-bit MCUs under 14.2-MeV neutrons in the Artix-7 FPGA. 93
5.28 Observed shapes for 3-5 bit MCUs under 14.2-MeV neutrons in the Artix-7 FPGA. 93
5.29 The setup of Artix-7 XC7A100T FPGA under thermal neutrons 94

5.30 2- and 3-bit MBU cross-sections the Artix-7 FPGA under thermal neutrons. . . 95
5.31 2- and 3-bit MCU cross-sections of the Artix-7 FPGA under thermal neutrons. . 97
5.32 SBU cross-sections for the FFs and the CRAM of the Artix-7 FPGA. 97
5.33 Possible shapes of the 2-bit MCUs in the Artix-7 FPGA under thermal neutrons. 98
5.34 Abundance and classification of the 3-bit MCUs observed in the Artix-7 FPGA. 98
5.35 Shapes of the 3-bit MCUs and their signatures in the Artix-7 FPGA under thermal neutrons. 99
5.36 Abundance and classification of the 3-bit MCUs observed in the Artix-7 FPGA. 99
5.37 Shapes of 4- to 12-bit, 128-bit and 384-bit MCUs on the Artix-7 FPGA. 100
5.38 Abundance of 4- to 12-bit MCUs in the Artix-7 FPGA under thermal neutrons. 100
5.39 Comparison of MCU cross-sections from MUSCA-SEP3 vs. experimental results on the Artix-7 FPGA. 101
5.40 Comparison of cross-sections of thermal and fast neutrons in the Artix FPGA. . 102

List of Tables

3.1 Comparison I^2C and SPI protocols 38

4.1 Tested devices 39
4.2 Rounds of irradiation carried out in different facilities 45
4.3 Informational data on the monoenergetic neutron field used at the PIAF 49
4.4 List of parameters of the memory and radiation-ground experiment 52

5.1 Rounds of irradiation for the CY14V101QS memory under 14.2- MeV neutrons . 55
5.2 Rounds of irradiation for the CY14V101QS memory under 15.3-MeV protons . . 59
5.3 Rounds of irradiation for the CY14V101QS memory under thermal neutrons . . 60
5.4 2-bit MCU cross-sections (cm^2/bit), obtained with MUSCA-SEP3 67
5.5 Rounds of irradiation for the CY14B101J memory under 15.3-MeV protons . . . 69
5.6 Rounds of irradiation for the CY14B101J memory under thermal neutrons . . . 70
5.7 Rounds of irradiation for the CY14B101J memory under 14.8-MeV neutrons . . 71
5.8 Rounds of irradiation for the FRAMs under 15.3-MeV protons 75
5.9 Rounds of irradiation carried out for the FRAMs under 1-MeV protons 77
5.10 Rounds of irradiation for the FRAMs under thermal neutrons 78
5.11 Rounds of irradiation for the FRAMs under 14.8-MeV neutrons 79
5.12 Rounds of irradiation for the MB85AS4MT ReRAM under 1-MeV protons . . . 82
5.13 Rounds of irradiation for the MB85AS4MT ReRAM under thermal neutrons . . 83
5.14 Rounds of irradiation for the MB85AS8MT ReRAM under thermal neutrons . . 84
5.15 Rounds of irradiation for the ReRAMs under 14.8-MeV neutrons 84
5.16 Rounds of irradiation for the MRAMs under thermal neutrons 86
5.17 Rounds of irradiation for the MRAMs under 14.8-MeV neutrons 86
5.18 An overview of the detected SEEs on FRAMs, ReRAMs, and MRAMs 87
5.19 Irradiation rounds of the Artix-7 FPGA, under 14.2-MeV neutrons 91
5.20 Characteristics of MBUs detected of the CRAM in the Artix-7 XC7A100T FPGA 91
5.21 Number of MCUs extracted by using the statistical approach in the Artix-7 FPGA. 92
5.22 Rounds in the Artix-7 FPGA under thermal neutrons 94

5.23 Characteristics of MBUs in the Artix-7 FPGA under thermal neutrons 95
5.24 Characteristics of MCUs in the Artix-7 FPGA under thermal neutrons 96

Abbreviations

BEOL	Back-End-Of-Line
BL	Bit Line
BRAM	Block RAM
CS/SS	Chip/Slave Select
CLB	Configurable Logic Blocks
CMOS	Complementary Metal-Oxide-Semiconductor
CNA	Centro Nacional de Aceleradores
CRAM	Configuration RAM
COTS	Commercial-Off-The-Shelf
GENESIS	GEnerator of NEutrons for Science and IrradiationS
DCM	Digital Clock Manager
DD	Displacement Damage
DRAM	Dynamic Random Access Memories
DSP	Data Signal Processor
DV	Difference Vector
DUT	Device Under Test
ECC	Error Correction Code
EDAC	Error Detection And Correction
ELF	Extremely Low Frequency
FN	Fowler-Nordheim
FPGA	Field Programmable Gate Array
FTJ	Ferroelectric Tunnel Junction
FWHM	Full Width at Half Maximum
FRAM	Ferroelectric Random-Access Memory
GDS	General Design Specification
GMR	Giant MagnetoResistance

GPIO General Purpose Input Output

HDD Hard Disk Drive

HfO_x Hafnium Oxide

HPC High-Performance Computing

HRS High Resistance State

I2C Inter Integrated Circuit

IC Integrated Circuit

ILL Institut Laue-Langevin

IOB Input/Output Blocks

IOT Internet-of-Things

IR InfRared

IRDS International Roadmap for Devices and Systems

ITRS International Technology Roadmap for Semiconductors

LAr Liquid Argon

LELAPE Listas de Eventos para Localizar Anomalías Preparando Estadísticas

LEO Low Earth Orbit

LET Linear Energy Transfer

LPSC Laboratoire de Physique Subatomique et de Cosmologie

LRS Low Resistance State

LUT Look-Up Table

MBU Multiple-Bit Upset

MCNP Monte-Carlo N-Particle

MCU Multiple-Cell Upset

MD Manhattan Distance

MFST Metal-Ferroelectric-Semiconductor-Transistor

MISO Master In, Slave Out

MRAM Magnetic Random-Access Memory

MOS Metal-Oxide-Silicon

MOSI Master Out, Slave In

MOSFET Metal–Oxide–Semiconductor Field-Effect Transistor

MTJ Magnetic Tunnel Junction

MW MicroWave

NV Non-Volatile

nv-SRAM Non-Volatile Static Random-Access Memory

PAC-G Platform for Advanced Characterisation of Grenoble

PCB Printed Circuit Board

PCM Phase-Change Memory

P-D Polarization–Displacement

PIAF PTB Ion Accelerator Facility

PKA Primary Knock-on Atom

PLL Phase-Locked Loop

POS Positive Subtraction

Qcrit Critical Charge

QSPI Quad SPI

RF Radio Frequency

ReRAM Resistive Random-Access Memory

SAA South Atlantic Anomaly

SBU Single-Bit Upset

SCL Serial Clock line

SDA Serial Data line

SEB Single Event Breakdown

SEE Single Event Effects

SEFI Single Event Functional Interrupt

SEGRT Single Event Gate Rupture

SEL Single Event Latch-up

SER Soft-Error Rate

SET Single Event Transient

SEU Single Event Upsets

SL Source Line

SONOS Silicon - Oxide - Nitride - Oxide - Silicon

SPI Serial Peripheral Interface

SRAM Static Random Access Memory

SSS Solid State Storage

STI Shallow-Trench Isolation

STT	Spin-Torque Transfer
TaO$_x$	Tantalum Oxide
TAS	Thermal-Assisted Switching
TENIS	Thermal and Epithermal Neutron Irradiation Station
TID	Total Ionizing Dose
TiO2	Titanium Oxide
TNID	Total Non-Ionizing Dose
USB	Universal Serial Bus
UV	UltraViolet
WOx	Tungsten Oxide

Chapter 1

Introduction

1.1 New Space

The democratization of space is an ongoing event involving the introduction of new marketing opportunities. It provides a comprehensive combination of space into society in a tolerable style, either environmentally or economically. Today, large businesses and startups use space as a precious resource to modernize research procedures. The entrepreneurial and financial projects in space introduce a new term called "New Space." The New Space ecosystem emphasizes novel research, development models, economics, and management at a reduced cost [ESA11].

Space is aggressive to electronics due to the existence of galactic cosmic rays, which are composed of streams of charged particles (protons, electrons, heavy ions...). Their interaction with electronic devices impacts their performance, and this might occasionally result in a critical failure of an entire system. In addition, increasing miniaturization and complexity of such devices pose additional challenges, such as radiation data analysis and prediction of Single Event Effects (SEE) / Total Ionizing Dose (TID) trends for devices in the International Technology Roadmap for Semiconductors (ITRS) / International Roadmap for Devices and Systems (IRDS).

New Space and aerospace missions demand fast growth and lowered costs. The need to reduce expenses and increase reliability for spatial projects in harsh environments has pushed engineers to use Commercial-Off-The-Shelf (COTS) systems in the New Space era. COTS devices are used in an extensive range of embedded system products, autonomous driving, and High-Performance Computing (HPC) applications, among others. The following section discusses COTS devices and the need to use them in space.

1.2 COTS devices in New Space

Engineers currently employ radiation-hardened devices to withstand radiation effects for space applications. As space missions commercialized, COTS devices have become more common.

They are increasingly adopted in safety-critical applications because of their low cost and high performance [Tsi+20].

One of the critical difficulties of using COTS devices in space derives from the data storage requirements. In recent years, COTS non-volatile memories have been one of the fundamental components of most digital systems due to decrease circuit leakage power and their small size. Said memories can keep the stored data after disconnecting the power signals. Among these, Magnetic Random-Access Memories (MRAMs), Ferroelectric Random-Access Memories (FRAMs or FeRAMs), Phase-Change Memories (PCMs), and Resistive Random-Access Memories (RRAMs or ReRAMs) have been recently proposed as innovative solutions to keep more data reliable against radiation effects at less expense than traditional rad-hard solutions. However, COTS devices are not developed to assure an accurate operation in such harsh conditions; therefore, they should be evaluated before using them as avionics or on space missions.

The recent releases of emerging memories and their application in New Space highlight the considerable importance of knowing more about these state-of-the-art products. This thesis endeavors to provide background and a description of the functionality of these memories against 14.2/8-MeV and thermal neutrons, and 15.3-MeV and 1-MeV protons.

1.3 Objectives of this thesis

The main objective of this thesis is the investigation of SEEs provoked by radiation on new types of emerging non-volatile memory technologies. Also, a detailed analysis of the physical processes that result in device failure is carried out.

Thus, the SEE sensitivity against radiation of the following memories has been carried out: Non-volatile Static Random Access Memories (nv-SRAMs), Ferroelectric Random-Access Memories (FeRAMs, F-RAMs, or FRAMs), Resistive Random-Access Memories (ReRAMs or RRAMs), Magnetoresistive Random-Access Memories (MRAMs), and finally a bulk 28-nm CMOS Xilinx Artix-7 FPGA. These devices were tested under 1 and 15-MeV protons, thermal and 14.2/8-MeV neutrons. In addition, the nv-SRAM and the Artix-7 FPGA were tested under thermal and 14.2-MeV neutrons with different angles of incidence of impinging particles in order to study the device orientation dependence with respect to the radiation source. The comparison of emerging memories and Artix-7 behavior against different particles will be made. Furthermore, the observed bitflips were analyzed using a statistical method for SEE categorization according to their multiplicity that was developed previously in our research group. This will be explained in detail in Chapter 4 of the thesis.

This study is based on data obtained over five years on several irradiation campaigns. The results presented in this thesis can be used to enhance the reliability of existing memory technologies or to create new ones that can be operated properly in space missions. To the best of the author's knowledge, the radiation effects of thermal neutrons on COTS FRAMs and MRAMs have not been studied so far and also, this thesis is the first research that has tested ReRAMs with thermal and 14.8-MeV neutrons, and 1-MeV and 15.3-MeV protons. In addition, there have been made very few experimental tests made on COTS nv-SRAMs up to this point.

Thus the specific objectives of this thesis are:

1. To explore angular effects and their contribution to the total SEE sensitivity on a nv-SRAM working with Serial Peripheral Interface (SPI) protocol under 14.2-MeV neutrons. Also, the memory was tested under 15.3-MeV protons and thermal neutrons.
2. Subsequently, to predict the effects of 14.2-MeV neutrons on the same nv-SRAM described above by using a simulation tool called Multi-Scales Single Event Phenomena Predictive Platform (MUSCA-SEP3) [Hub+09a]. This tool can be used to extrapolate radiation effects to a realistic environment, where a plethora of angles of incidence is possible.
3. To test and study another nv-SRAM that works with Inter-Integrated Circuit (I^2C) protocol under 14.8-MeV and thermal neutrons, and 15.3-MeV protons.
4. To compare the obtained results of both nv-SRAMs.
5. To evaluate the SEE sensitivity of two kinds of FRAMs, MRAMs, and ReRAMs under different radiation sources.
6. To explore the sensitivity of a Xilinx 28-nm SRAM-based Artix-7 FPGA under 14.2-MeV neutrons, as well as thermal neutrons impinging at different incident angles.
7. To compare Artix-7 FPGA's sensitivity between thermal neutrons and 14.2-MeV neutrons.
8. To validate the experimental data obtained with the Artix-7 FPGA with predictions issued by MUSCA-SEP3.

This thesis can be separated into two parts: the first one (which covers the first three chapters) provides the basic perceptions. The second part presents the results of the research activity, and it comprises the last three chapters. In particular, the thesis is organized as follows:

- Chapter 1 introduces the New Space concept, the application of COTS memories in New Space, and the objectives of this Ph.D. thesis.

- Chapter 2 presents the radiation environments, discusses interaction of radiation with matter, as well as practical concepts for radiation tests. Besides, it considers cumulative effects and SEEs.
- Chapter 3 presents memory cell technologies and communication protocols.
- Chapter 4 presents the experimental setup, including data processing, test methods, test setup, and test facilities of the experiments carried out for this PhD thesis.
- Chapter 5 gives a detailed analysis of the SEEs on emerging memories, which involves nv-SRAMs, MRAMs, FRAMs, and ReRAMs with 14.2/8-MeV and thermal neutrons, 1 and 15-MeV protons. Also, the results of Artix-7 FPGA under 14.2-MeV and thermal neutrons are provided.
- Chapter 6 presents the conclusion and refers to future work in this field.

Chapter 2

Radiation environments and effects on electronic systems

This chapter addresses essential radiation concepts and radiation environments, discusses interaction of radiation with matter, and describes radiation's different effects in integrated circuits.

2.1 Radiation Environments

Radiation is around us all the time and appears in various forms with different properties and effects. It is the process of transmitting energy as particles, rays, or electromagnetic waves. There are two main types of radiation: non-ionizing and ionizing [ESA11; J B99; Nat16b].

Non-ionizing radiation exists from various sources that do not have enough energy to ionize atoms or molecules. That means it can not remove electrons from atoms and molecules. Non-ionizing radiation covers the spectrum of ultraviolet (UV), visible light, infrared (IR), microwave (MW), radio frequency (RF), and extremely low frequency (ELF).

On the other hand, any radiation capable of knocking electrons out from atoms is known as ionizing. The ionizing radiation includes alpha and beta particles, neutrons, gamma, and X-rays [ESA11; Nat16b]. These are described in detail below:

- Alpha particles (α) are with a positive charge, two protons and two neutrons from the atom's nucleus. Alpha particles originate from the collapse of the heaviest radioactive elements, including uranium, radium, and polonium. They are very energetic and heavy, so they travel only a short distance (a few centimeters) in air.

- The second kind of ionizing radiation is beta particles. During radioactive breakdown, an atom's nucleus releases a beta particle. It can be either an electron or a positron [β^-] and [β^+] decay, respectively. Beta particles are small, fast-moving with high energy, and can travel further in the air (up to a few meters) than alpha particles.

- Gamma rays (γ) are created by the universe's hottest, most violent, and energetic objects and events, including regions around black holes, neutron stars and pulsars, and supernova eruptions. Gamma rays are also generated on Earth by natural radioactive decay, nuclear explosions, and lightning in thunderstorms. They do not contain any particles; instead, they are weightless packets of pure energy termed photons. Gamma-ray wavelengths are the shortest of all electromagnetic waves, around the size of an atom's nucleus [Nat16a].
- X-rays are similar to gamma ones since they have the same basic features; but the factor that makes a difference is their origin. Energy changes in an electron produce X-rays, such as going from a higher energy level to a lower one, provoking the excess energy to be released. X-rays have very short wavelengths, between 0.03 and 3 nano meters, with high energy. They come from hot objects such as pulsars, black holes, supernovas, or the plasma in our Sun's corona [Nat16c].
- Neutron radiation is created when high-energy particles from the Sun and outside the solar system interact with other particles or materials. Hence, neutron radiation is indirectly ionizing radiation. Since neutrons are high-speed nuclear particles and have an exceptional ability to penetrate other materials, they can travel great distances in air and need very thick hydrogen-containing materials (such as concrete or water) to block them [ESA11].

The natural radiation environment needs to be determined when electronic equipment is sent into space. Radiation sources vary: some originate in the Sun (e.g., solar flares, coronal mass ejection, and solar wind), and others derive from outside the solar system. These environments are classified into atmospheric neutrons, Van Allen belts, and terrestrial radiation sources. All environments will be explained below concerning their nature and properties [ESA11; J B99].

2.1.1 Radiation environments for New Space

To guarantee the proper functionality of the devices in space missions, the radiation environment for New Space applications has been subject of interest by researchers. It is divided into three main classes [Ada+81]:

1. Particles deriving from the Sun, including protons, electrons, and heavy ions.
2. Galactic Cosmic Rays (GCRs), which contain of protons and heavy ions.
3. Particles trapped in the Earth's magnetic field, or Van Allen belts, consisting of electrons and protons.

Solar particles:

The major source of interplanetary radiation is the Sun. Solar energetic particles are able to get to all areas of near-Earth space, containing the lunar surface, except for low-altitude and low-latitude Earth orbit. Solar flares happen randomly. They emit mainly electrons [Pet11], but also energetic protons, alpha particles, and heavy ions with all wavelengths of electromagnetic radiation.

Galactic Cosmic Rays (GCRs):

The second radiation source is due to GCRs deriving from outside the solar system but primarily from within the Milky Way galaxy. GCRs are high-energy ions of elements whose electrons have been lost as they traveled through the galaxy at almost the speed of light. They form an isotropic of protons (85%), alpha particles (14%), and heavy ions (1%) at very high energies (in the order of tens of MeV/nucleon to hundreds of GeV/nucleon and above). Also, the GCR energy spectrum is moderated by the Sun activity; the higher the Sun activity, the lower the GCR intensity. This is justified because the increase in the activity of the Sun causes to increase in the intensity of the solar wind, and it leads to better protection of the lower Earth's environment against incoming GCRs [DAl16]. When heavy ions and GCR protons reach the ground, they interact with oxygen and nitrogen atoms and generate a cascade of events at different atmospheric altitudes and ground levels. The secondary particles include neutrons, protons, electrons, muons, pions, photons, and gamma rays.

GCR particles at high latitudes lead to increasing radiation exposures for humans. These particles can also travel through or stop in satellite systems, and deposit enough energy to damage spacecraft and electronic systems.

Particles trapped in the Earth's atmospheric field:

These particles mainly coming from the Sun, or GCRs, are trapped in the magnetic field produced by the Earth. Thus, they provide the possibility of creating radiation fields around the Earth. These fields are commonly known as the Van Allen belts as they were discovered by James Van Allen in 1958. It includes two areas of the magnetosphere with high-energy protons and electrons trapped by the Earth's magnetic field. The inner belt extends from 100 km to 10,000 km over the Earth's surface. It mainly traps high-energy protons (up to several 600 MeV), and electrons (up to several MeV) originating from the solar wind or protons produced by collisions between galactic cosmic ions with the atmosphere.

The range of the outer belt varies from 13,500 km to about 65,000 km, and is mainly formed of electrons (up to 7 MeV) [HA93]. Alpha particles and heavy ions are also in both

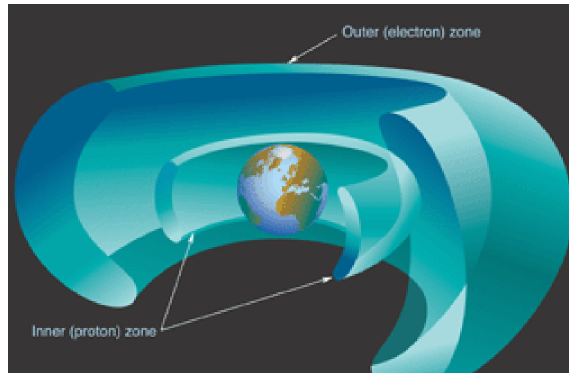

Figure 2.1: *Van Allen radiation belts [ESA11].*

belts; however, their proportion is negligible as well as their energies (in the order of tens of MeV/nucleon) [Ree08]. Figure 2.1 displays Van Allen radiation belts. The most significant characterizations are listed the below [ESA11]:

- The Van Allen belts are symmetrical with the magnetic axis of the Earth.
- There is an inclination of 11° between the magnetic axis and the rotation axis of the Earth.
- There is a 500 km offset from the magnetic axis of the Earth toward the Pacific Ocean north-south.
- Due to high flux, detectors in satellites are turned off or set in safe mode while moving across this region.

Due to the fact that the terrestrial magnetic field is tilted with respect to its rotation axis, the inner Van-Allen belt is closer to the terrestrial surface in a region located in the South Atlantic and the coast of Brazil, Argentina, and Uruguay. This leads to a considerably higher particle flux than the rest of the Earth at the same altitudes and latitudes, in a region called "South Atlantic Anomaly" (SAA), which can be seen in Figure 2.2.

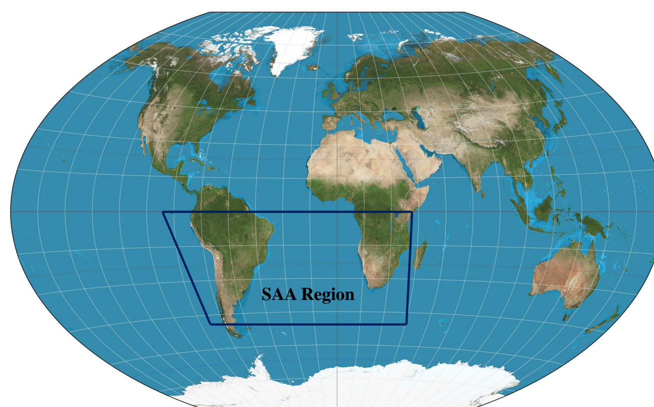

Figure 2.2: *The SAA region.*

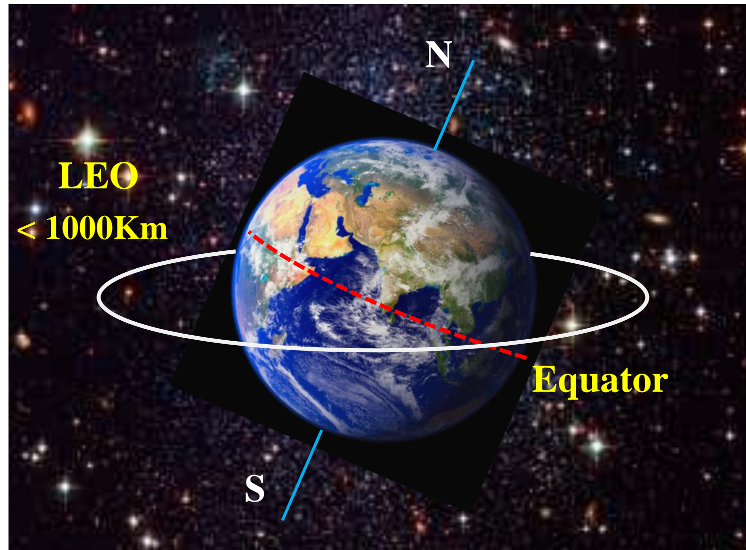

Figure 2.3: *Low Earth Orbit (LEO) is an orbit close to Earth's surface. It is at an altitude of less than 1000 km but could be as low as 160 km above Earth. It is used for communication, the International Space Station (ISS), and Hubble Space Telescope.*

One of the orbits above the Earth is Low Earth Orbit (LEO). It is at an altitude of less than 1000 km, as shown in Figure 2.3. LEO is the main environment where New Space devices are deployed. Thus, it is usually used for satellite imaging to take higher resolution images and also for the International Space Station (ISS). An LEO satellite interacts with the inner belt particles, particularly in the SAA region, since it is responsible for most of the trapped radiation obtained in this orbit. The radiation environment of LEO is a complex combination of GCRs, particles trapped in the radiation belts and secondary particles that resulted from the interaction from GCRs and the Earth's atmosphere. High electron fluxes can also be met in LEO, especially at the polar regions.

Totally, upsets that occur in the low-latitude region are the result of the penetration of high-energy protons (more than 50 MeV) of the Earth's inner radiation belt. Also, for the LEO space environments, neutrons are the predominant inner energetic particle source and should be assessed when evaluating part performance [Red+17; Red+15; SL04]. In addition, the function of low-energy protons in space environments and near-earth orbits like the LEO has been investigated. Recent measurements on SRAMs indicate that low-energy protons play a critical role, especially in increasing the SEE rate in COTS memories in the LEO [Aus+17; Rod20].

2.1.2 Atmospheric neutrons

Atmospheric neutrons result from high-energetic cosmic ray particle (mostly protons) interactions through spallation reactions on atmospheric nuclei. Since the atmospheric neutron

flux is fully impacted by geomagnetic covering, it can be six times higher at the poles than at the equator. Therefore, the presence of neutrons is also relevant at LEO. The neutron peak flux reaches the maximum value at around 20 km of altitude. Below 20 km, the atmosphere's density effectively declines the flux, as it is two to three orders of magnitude lower than its peak value at ground level [Ong77; EDN04].

Contrary to protons and heavy ions, neutrons are not able to provoke failures in integrated circuits via direct ionization. However, they are capable of inducing errors if the deposited charge is sufficient to trigger an event via nuclear reactions with silicon [ESA11; Nat08].

2.1.3 Terrestrial radiation sources

The Earth is the origin of terrestrial radiation. There are radioactive materials such as uranium and its decay products, such as thorium, radium, and radon, naturally present everywhere, like soil and rock [ESA11]. These materials are either ingested with food (that contains carbon-14 and potassium-40), water (radon dissolved in water), or air (radon coming out from the ground) [ESA11].

2.2 Interaction of Radiation with Matter

This section aims at introducing the different ways subatomic particles interact with electronic devices. Interaction in a natural environment depends on the radiation type, the particle type, and its energy. There are four different types of incident radiation: charged particles, electrons, photons, and neutrons.

1. The charged particles include alpha particles, beta particles, protons, and ions. These particles lose their kinetic energy while traversing the medium through the ionization and excitation of atoms. When a charged particle penetrates the matter, it uses electromagnetic forces on electrons and nuclei and transmits its energy to them. The energy will cause ionization and create ion-electron pairs in the medium [Tur07]. It is worth mentioning that 90-nm bulk Complementary Metal-Oxide-Semiconductor (CMOS) technologies and the below can be ionized directly by protons [ESA11].

2. Electrons penetrating matter lose energy and are scattered. Changes also occur in the penetrated medium, resulting in excitation or ionization that includes the ejection of electrons (i.e., the production of secondary electrons) [Chu+16]. These interactions are categorized into two different types: elastic and inelastic. In elastic interactions, no energy is transferred from the electron to the matter. In inelastic interactions, if energy is

conveyed from the incident electrons to the sample, the electron energy is lessened after interaction with the medium [Kru15].

3. Photons are electromagnetic radiation and massless. They act differently than charged particles because of having no electrical charge and interact with the material in various ways, depending on their energy and the nature of the matter. Photons move in a straight line with a velocity that is the speed of light. Compared to charged particles, photons do not continuously lose energy when they travel within matter. They can interact with the nuclei or with the shell electrons. The probability of a photon interaction can change concerning these criteria [Tav10; Vér+03; Bas11]:

   - The photon energy.
   - The atomic number and density of the medium (electron density of the absorbing matter).

   The three main types of photon interactions are detailed below:

   (a) Photoelectric Effect: The photoelectric effect is a phenomenon in which matter releases electrons after absorbing energy from a photon emitted by an electromagnetic beam. All the photon energy is given to this electron; for that reason, the photon disappears. When this happens, the electron is expelled from the atom. Therefore, this event causes a vacancy in the shell that the electron initially occupied. An electron falling from a higher energy shell fills the generated vacancy in the electron shell [ESA11; PN07].

   (b) Compton scattering: In Compton scattering, a photon hits an electron and transmits some of its energy to the outer shell electron of an atom. The photon yields its energy and is scattered in a different direction [Vér+03; Bas11]; this photon is known as a recoil electron or a Compton electron. The Compton effect is the dominant photon process having an energy between tens keV and several MeV [ESA11].

   (c) Pair Production: If the photon's energy is at least two times greater than the mass of an electron, 1.022 MeV, the photon's energy can create an electron and positron pair. In this process, a photon interacts with the electric field of the nucleus of an atom. The photon entirely disappears while an electron and a positron are formed. Pair production is possible with rising photon energies and a high atomic number of materials (larger nuclei) [Tav10; Bas11].

4. Neutrons are a notable category of radiation that consists of uncharged particles. Neutral particles such as neutrons can not lose energy by ionization; hence, they interact with the nuclei of atoms of the absorbing material. The neutron shower from cosmic rays catches the atmosphere with a broad spectrum of energies, but they quickly lose energy. When a very heavy nucleus is broken up in a crash with a high-energy proton, the fragments will quickly remove their excess neutrons, creating many secondary neutrons [Tav10], as shown in Figure 2.4. The probability of a reaction happens to depend on [Mey76]:

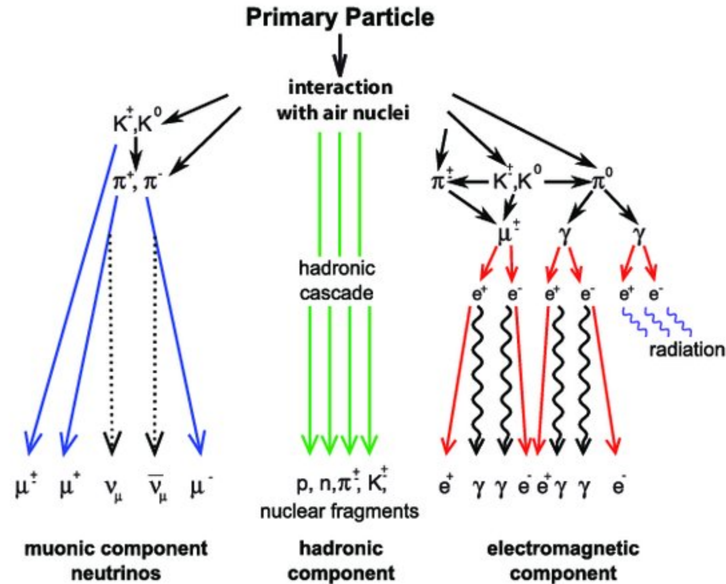

Figure 2.4: *Schematic view of an extensive air shower (EAS) [Hau+18].*

(a) The neutron kinetic energy

(b) The identity of the target nuclide

Neutrons are categorized according to their energy:

(a) Thermal ($\sim$ 0.025 eV)

(b) Slow ($<$ 10 eV)

(c) Intermediate (10 eV – 100 keV)

(d) Fast ($>$ 100 keV)

A neutron might be scattered from the nucleus or combined with it. Accordingly, two reactions can occur when a neutron interacts with a nucleus: scattering or absorption. In the scattering reactions, a neutron emerges from a nucleus. The speed and direction of a neutron change when a nucleus scatters it. But the nucleus remains with the same number of protons and neutrons that it had before the process. Scattering phenomena are classified into elastic and inelastic. They are described below [ESA11]:

- Elastic Scattering: Elastic scattering is the most crucial process for slowing down neutrons compared to inelastic scattering. A neutron hits a nucleus, and a fraction of the neutron's kinetic energy is conveyed to the nucleus during the interaction. If the nuclei obtain enough energy from the neutron, it can quit the crystalline silicon network [ESA11].
- Inelastic Scattering: When the scattering is inelastic, some of the neutron's kinetic energy is internally conveyed to the target nucleus. The nucleus remains in an excited and unstable state which causes it to emit some radiation quickly to yield it to a stable state. Then it degrades by releasing neutrons, gamma/alpha/beta radiation, and protons [PN07; Cha19].
- Thermal Neutron Capture (Absorption): Boron is used broadly as a p-type dopant in CMOS technology. It naturally occurs as isotopes ^{11}B (80.1% abundance) and ^{10}B (19.9% abundance). The problem that leads to SEEs is that ^{10}B is unstable when exposed to thermal neutrons. Thus, ^{10}B atoms can react with impinging thermal neutrons by absorbing them. Consequently, a nucleus fission reaction occurs: a Li recoil nucleus, a gamma photon, and an alpha particle are generated as secondary products (Figure 2.5). The alpha particle and the lithium recoil are able to yield soft errors in electronic devices (the gamma photon is capable of induce charge, although its cross-section is much smaller). It should be mentioned that the third considerable source of causing SEEs is the secondary radiation caused by thermal neutrons [BS00].

2.3 Useful concepts for radiation experiments

This section gives an overview of basic and practical concepts in radiation environments.

1. Linear Energy Transfer (LET): When the particle interacts with the material, it transfers its energy (E) to the matter. The LET refers to the charge deposition or the amount of energy transmitted through ionization per unit of length over the target. Usually, it is expressed concerning the density (ρ) of the traversed material, so it is presented in

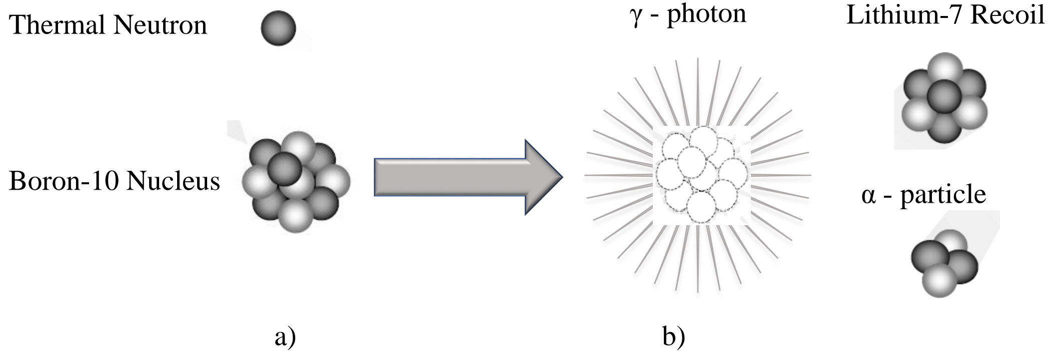

Figure 2.5: *Illustration of the process of ^{10}B fission. a) Neutron capture b) Products issued from the fission of an unstable ^{10}B nucleus that absorbed a neutron: a Lithium-7 recoil nucleus, a gamma photon, and an alpha-particle.*

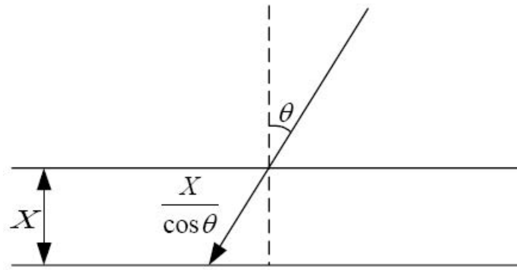

Figure 2.6: *Deposited energy with a θ incident angle [ESA11].*

MeV/mg/cm^2, Eq. 2.1. ΔE is the energy variation of the particle, and ΔX is the traversed distance inside the matter [ESA14].

$$LET = \frac{1}{\rho} \cdot \frac{\Delta E}{\Delta X} \tag{2.1}$$

If ΔE > E_{C} (critical energy), an SEE might happen. A LET threshold (LET_{th}) is the minimum LET that provokes an upset effect. Accordingly, if components have a high LET_{th}), they would have high tolerance against soft errors. As well as, there is another definition that the most often used. The deposited energy is equivalent to:

$$\Delta E = \frac{dE}{dX} \cdot \frac{X}{\cos\theta} \tag{2.2}$$

where θ is the particle incident angle. Figure 2.6 shows deposited energy for a heavy ion with a θ incident angle [ESA11].

2. Critical Charge (Q_{crit}): The Q_{crit} is the lowest charge that a particle must deposit in a node of an integrated circuit to invert its state and to provoke malfunction [ESA11].

3. Cross-Section: The cross-section, σ, quantifies the sensitivity of a device against a certain source of radiation. It is the ratio of the number of single events detected in the device by the particle fluence (i.e., particles per cm^2) that hit the component under test. Thus, the cross-section can be interpreted as an impinging particle's probability of provoking an SEE. Eq. 2.3 defines metric of cross-section [ESA11]:

$$\sigma = \frac{\#\ of\ observed\ events}{fluence} \tag{2.3}$$

If the device is tilted at an angle θ, the fluence must be corrected by multiplying it by $\cos\theta$ [ESA14]:

$$\sigma = \frac{\#\ of\ observed\ events}{(fluence \times \cos\theta)} \tag{2.4}$$

When $\theta = 0$, the device surface is normal to the beam axis.

In addition, if the cross-section is divided by the capacity of the memory (number of bits), it can be used for a comparison of the radiation sensitivity of memory devices in different sizes:

$$\sigma = \frac{\#\ of\ observed\ events}{(fluence \times \#\ of\ bits)} \tag{2.5}$$

It should be mentioned that if events with different multiplicities are observed during radiation experiments, the cross-section should be calculated for each multiplicity individually for a detailed and precise analysis of the SEE sensitivity of the device. With nuclear reactions that involve neutrons, the cross-section highly depends on the target isotope and the energy of the incident neutrons.

4. Bragg peak: When the particle penetrates the medium, it loses its energy per unit length. Along the path and close to the end, it reaches a maximum energy loss, referred to as the "Bragg peak" [Tav10], as depicted in Figure 2.7 [Grd15].

2.4 Radiation Effects

Both charged particles and non-charged particles, when interacting with matter, can provoke undesired effects in semiconductor devices. We will classify radiation-induced effects into two categories: Cumulative effects and SEEs [ESA11].

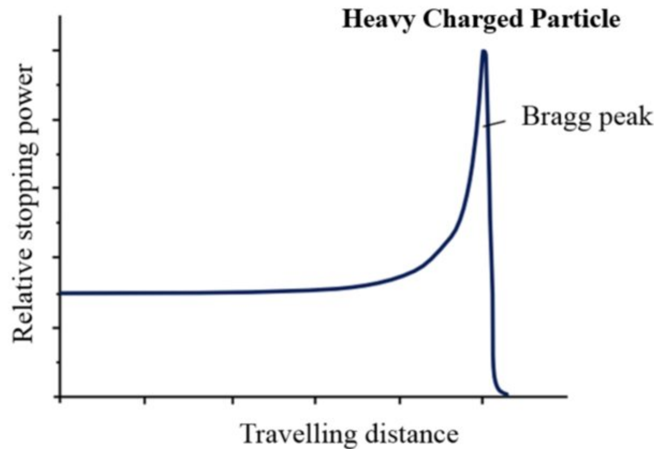

Figure 2.7: *Bragg curve for protons.*

2.4.1 Cumulative effects

Radiation exposure generates stable and permanent changes in devices and circuit features that may cause malfunction. TID effects are produced by ionizing particles, and non-ionizing ones will provoke displacement damage effects, also called Total Non-Ionizing Dose (TNID) [ESA11].

- **Total Ionizing Dose (TID)**

  The total ionizing dose effect causes cumulative persistent ionizing damages. It affects insulating layers with trapping charges or makes interface changes. Trapped positive charges shift the gate threshold voltages in Metal-Oxide-Silicon (MOS) devices. Interface states significantly raise device leakage currents (which increases power consumption). TID also affects optical components such as cover glasses, fiber optics, and passive materials such as plastics [ESA10].

- **Displacement damage (DD)**

  Displacement damage (DD) is a cumulative and persistent destruction effect that damages the crystalline structure of semiconductors and some optical materials by energetic particle collisions. Particles crossing crystalline materials can store sufficient energy in a collision with an atom to relocate the atom from its lattice position, forming an interstitial defect. The position left by the atom is pointed to as a vacancy. Interstitials and vacancies are movable and can gather or react with impurities existing in the lattice structure, generating stable faults [ESA10].

2.5 Single Event Effects (SEEs)

Energetic ions passing over integrated circuits generate a trail of ionization; hence, they induce a variety of physical phenomena known as SEE [ESA10]. Contrary to TID effects, which emerge after long periods of radiation exposure and need charge build-up, SEEs are immediate phenomena that take place on a timescale commonly estimated in nanoseconds. Figure 2.8 illustrates the occurrence of SEEs.

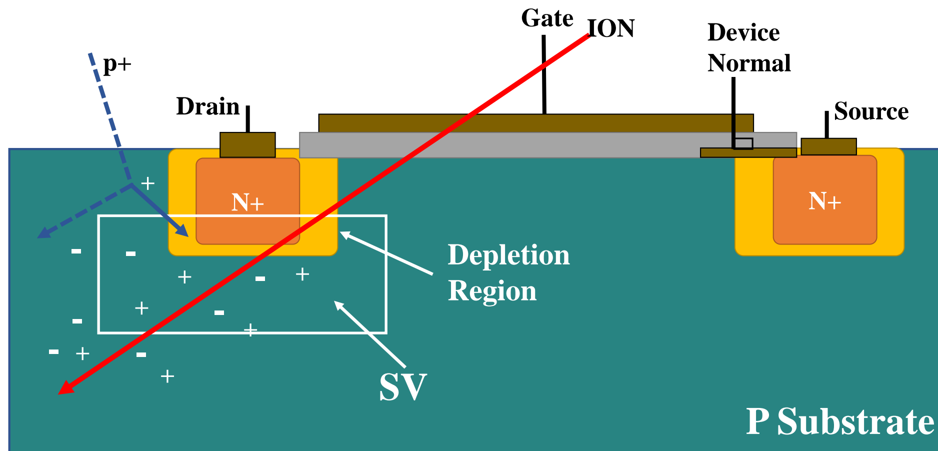

Figure 2.8: *SEE mechanisms are provoked by an ionizing particle passing through a sensitive volume (SV) in an active (semiconductor) device. The ionizing particle might be a heavy ion from the primary radiation environment (red line) with enough energy to pass through the entire material (displayed by the thick red arrow). On the other hand, it can be a recoil ion (short and blue arrow) created by a proton (thin dashed arrow) and an atom in the semiconductor lattice [NM18].*

A number of factors raise the probability of causing a SEE on a microelectronic device. Some works have shown that the sensitivity depends on the power supply values; the lower the power supply, the higher the probability of an SEE [Haz+03; GGO03; ASP04]. Also, other research found dependences on temperature [Geo+03]. Furthermore, the clock frequency has been taken into account to influence the SER value [IF04].

Finally, SEEs can be classified into two sub-groups [Bos17; DM03], Figure 2.9 shows the classification of SEEs:

- Non-destructive SEEs that are temporary and recoverable, such as Single Event Transient (SETs), Single Event Upsets (SEUs), and Single Event Functional Interrupt (SEFIs).
- Those which are destructive, such as Single Event Latch-up (SEL), Single Event Gate Rupture (SEGR), and Single Event Breakdown (SEB).

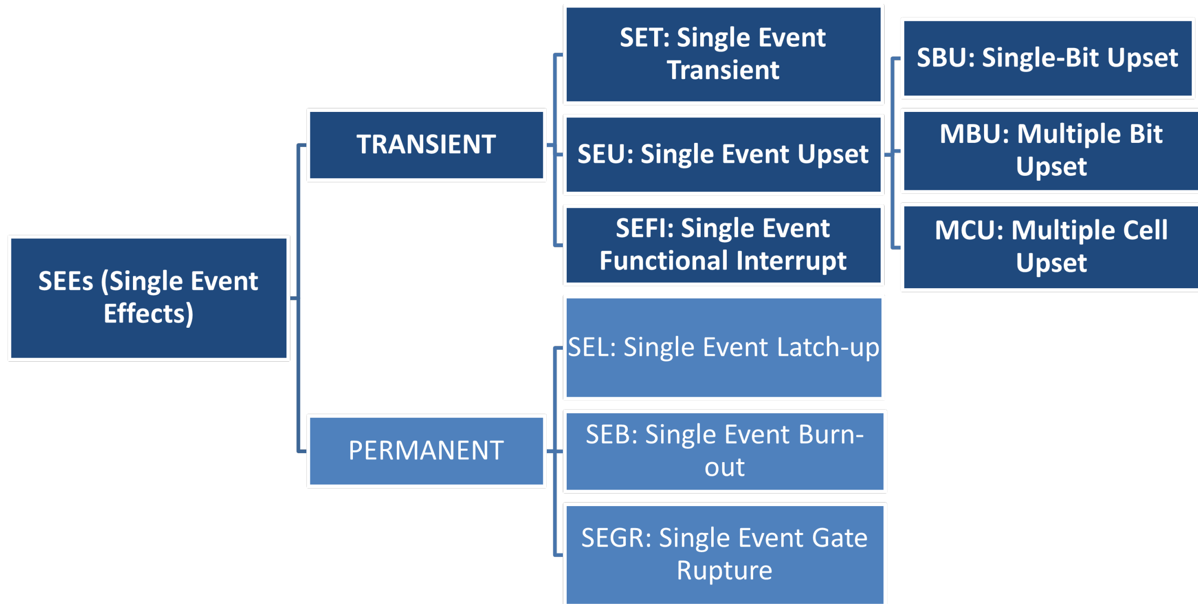

Figure 2.9: *Classification of SEEs.*

2.5.1 Single-Event Transients (SETs)

A Single Event Transient (SET), occurs when a transient voltage pulse propagates to the device's output. SETs can also broadcast in a combinational circuit and are captured by a memory element during a clock edge [ESA11; Bos17; Poi+03].

2.5.2 Single-Event Upsets (SEUs)

Single Event Upsets (SEUs) occur when single charged particles impact at sensitive nodes of storage elements such as flip-flops, latches, SRAM cells, etc. When a single charged particle strikes such an element in a digital circuit, it loses its energy by creating electron-hole pairs resulting in a compact ionized track in the local region. This ionization induces a transient current pulse [Bes93]. The consequence of the SEU phenomenon is called bit-flip. They can also result from a SET occurring in the peripheral logic during a write operation. The mechanisms at play behind SEUs vary depending on the memory cell technology [ESA11; Bos17].

Figure 2.10 explains the events when an SRAM cell is upset by a particle strike. The first schematic describes the initial state of an SRAM cell: blue marks are at a high potential and red ones at a low potential; for each transistor, ON or OFF modes are specified in the figure.

The central schematic represents the effect of hitting an ion on the M_1 transistor, which is in state OFF. The transistor would be ON as the charge collection causes a current pulse. Its inverter is excited, and its output is temporarily changed to a potential between the ground and VDD. Since its output is connected to the second inverter's (M_3+M_4) input, the second inverter might be disturbed; so the output falls to an unstable state, provoking positive feedback on

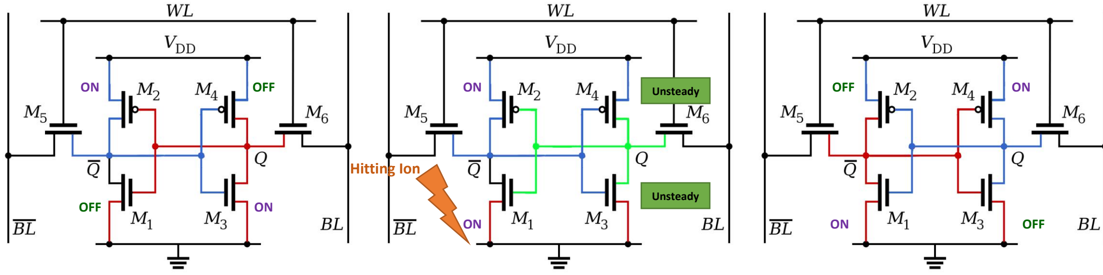

Figure 2.10: *Explanation of an SRAM cell being struck by an ion and suffering an SEU.*

the first inverter ($M_1 + M_2$). The two uncertain inverters may recover their initial states or maintain opposite states (right-hand schematic); in the last case, the cell is affected, leading to data corruption [Bos17].

2.5.3 Single-Bit Upsets (SBUs), Multiple-Bit Upsets (MBUs) and Multiple-Cell Upsets (MCUs)

When one particle flips only one cell, it is known as a Single Bit Upset (SBU). Otherwise, if the charge generated by impinging particles is shared by adjacent cells, this event is identified as a Multiple Cell Upset (MCU). If the cells affected by multiple events belong to the same word, the phenomenon becomes a Multiple Bit Upset (MBU) [ESA11]. Figure 2.11 displays the occurrence of an MBU and MCU.

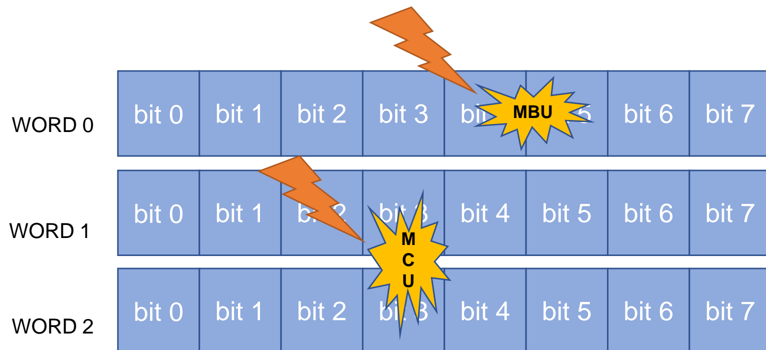

Figure 2.11: *Explanation of MBU and MCU, two or more upsets in the same word and in the neighbor words, respectively, induced by a single particle.*

It should be mentioned that Error Correction Codes (ECC), like Hamming codes, is used to mitigate SEUs as correction of errors in a word [LC04; NJS15].

2.5.4 Single-Event Functional Interrupts (SEFIs)

A SEFI is a soft error due to a particle hit or nuclear interaction which results in to reset, temporary hang, or malfunction of the affected component. It can also lead to several tens

or even hundreds/thousands of bitflips in the memory elements. It is worth mentioning some important points about SEFIs:

1. A SEFI is often often (but not always) related to an SBU/MBU in a control bit or register, or to a SET in a clock line.
2. Variations in functionality might need a reset of the device, reprogramming of the control registers, or power cycling.
3. Because of a period of high current, SEFI can present hidden reliability issues. SEFIs that cause permanent damage are defined as single-event hard errors [Sta17].

2.5.5 Single-Event Latchups (SELs)

A Single-Event Latchup is the effect of the triggering of a parasitic thyristor (PNPN structure) existing within the component and potentially in bipolar circuits. When it occurs, a current flows and raises the die's local temperature, destroying the structure. This effect can be ended by switching the circuit off. A particular case of latchup, named micro-latchup, occurs when the internal device circuitry limits the current. Since the current is limited, the micro-latchup is not harmful, although the loss of functionality of the device might be partial or total [ESA11].

2.5.6 Single-Event Burnouts (SEBs)

Another type of catastrophic effect, called Single-Event Burnout (SEB), happens principally in power MOSFETs. At the same time, the source gets forward-biased, and the drain-source current is higher than the breakdown voltage of the parasitic structures. The high current might evoke a local overheating capable of destroying the device [ESA11].

2.5.7 Single-Event Gate Ruptures (SEGRs)

SEGRs are events in which a particle strike results in a breakdown in the gate oxide of a MOSFET transistor or increases leakage current [ESA11]. A SEGR can result in either the device's degradation or complete failure.

Chapter 3

Memory devices and FPGAs

3.1 General Principals

3.1.1 Volatile vs. non-volatile memories and memory hierarchy

Memories are essential components of modern computer architectures to store data for later use by processors, displays, and input/output devices [HH07; Yua13; Aye03]. John Von Neumann [Von93] addressed a memory hierarchy design that includes several levels according to speed, cost, density, performance, and endurance. It consists of embedded memories (such as SRAMs and Dynamic Random Access memories (DRAMs)) as on-chip caches, DRAM as main memory, and magnetic Hard Disk Drive (HDD) as the storage. On the other hand, depending on their storage mechanism, memories are classi ed into two groups:

- Volatile memories can keep the information only when the system or power is switched on. Some examples of volatile memory technologies are SRAMs and DRAMs.
- Non-volatile memories do not lose their contents without power. These memories need power while saving the data; however, after the data are stored, they do not require power to keep data integrity. Some examples of non-volatile memories are FLASH and HDDs.

Volatile memories work typically quicker than non-volatile ones. Sometimes, volatile memories produce a more complex operation with lower storage density. On the other hand, retaining data in volatile memories consists of refreshing their data contents, which dissipates signi cant power. In this case, the information is read and then written back in a cycle. On the other hand, non-volatile memory technologies o er high storage density at low costs per bit, while their common disadvantages are slow operation with relatively poor read/write endurance.

Figure 3.1: Memory hierarchy.

Figure 3.1 depicts the typical memory hierarchy in modern computer architectures. Each level closer to the microprocessor has a higher speed and bandwidth but is smaller than the next level, one step down in the hierarchy.

This Ph.D. thesis focuses on studying the reliability of SRAM-based FPGAs and Solid State Storages (SSS's) with fault-tolerant manufacturing technologies, namely: FRAMs, nv-SRAMs, ReRAMs, and MRAMs.

3.1.2 Memory architecture of Solid State Storages (SSS's)

Typically, a SSS is composed of a control unit and memory arrays. The primary memory segment in an SSS was traditionally a DRAM volatile memory, but since 2009, it has been more commonly a NAND ash non-volatile one. Most solid-state memories present a similar architecture:

- Memory arrays are built of bit cells; each of them stores 1 bit of data. Each bit cell is related to a wordline and a bitline. Wordlines are assigned to the control lines running horizontally along the rows of the array to activate/deactivate the operation of the cells. In contrast, bitlines indicate the control/data lines running vertically along with the columns connected to the cells' inputs and outputs, as shown in Figure 3.2 ([HH07]).

Figure 3.2: Bit cell of an SSS.

- Peripheral circuitries are placed around the memory array to write to and read from it. They are implemented employing CMOS technology, which is the most common technology for integrated circuits due to its low static power consumption.

From another point of view, the physical position of a bit inside the memory relies on two agents:

- Scrambling: Scrambling means that the logical formation, as seen by the user from the outside of the chip, varies from the chip's physical structure. The outcome is that logically adjacent addresses might not be physically adjacent (this is named address scrambling) and that logically adjacent data bits are not physically adjacent (this is called data scrambling) [Bos17; Shi+14].
- Bit interleaving: An interleaved memory is a design that spreads memory addresses evenly across memory banks. By using bit interleaving, bits of similar weight are placed next to each other. Interleaving provides higher protection to MBUs, since a single particle is less likely to a ect several bits of the same word if their memory cells are further from each other.

3.1.3 Memory operation

Typically, memories implement two primary operations: read and write. These processes need a memory address and the write operation also requires speci c data. The memory states a single wordline that activates the bit cells in that row. The stored bit is connected to the bitline when the wordline is high; in the case that wordline is low, the bitline is disconnected from the bit cell [HH07]. These operations are discussed in detail below:

- Read: The bitline is initially left oating (Z). Then the wordline is switched ON, and the stored value drives the bitline to 0 or 1.
- Write: Depending on the desired value, the bitline is driven to 1 or 0. Next, the wordline is turned ON, and the bitline values in that row of bit cells are stored.

Each one of the types of emerging non-volatile memories studied in this PhD thesis has its particular way of reading/writing information, which will be discussed in detail in the following section.

3.2 Memory cell technologies

In this section, rst, volatile memory technologies will be explained; then, the structure and characteristics of non-volatile SRAMs (nv-SRAMs), FRAMs, ReRAMs, and MRAMs will be presented.

3.2.1 Static Random-Access Memories (SRAMs)

Features of SRAMs

SRAMs were released to the market by Intel in 1969. These memories are commonly employed in embedded systems due to their fast read/write performance (as low as 10 ns), low power consumption (particularly when idle), superior endurance, and easy production compatibility with standard CMOS manufacturing processes. They are termed static because stored bits do not need to be renewed. A typical SRAM cell consists of six transistors; two are used as access transistors, while four transistors make two cross-coupled inverters with a stable and complementary structure. The two possible inverter con gurations express the data stored in the cell, as shown in Figure 3.3. This type of memory takes up a large part of the area of the device, so they cannot reach very high densities, which makes them expensive to manufacture.

Figure 3.3: Schematic of an SRAM memory cell composed of 6 transistors.

Another disadvantage of SRAMs is their vulnerability to radiation. Primitive SRAMs were more robust because of high operating voltage and two large cross-coupled inverters, as each of them strongly drives the other to hold the bit in its programmed state [Bau05]. Further evolutions in SRAMs revealed an increase in the single-bit Soft-Error Rate (SER) due to

the shrinking cell sensitive volumes, considerable reductions in operating voltage and node capacitance [Sch+03]. Overall, the SER of SRAM-based systems increases with technology scaling and has become a signi cant reliability concern [Joh00].

Radiation e ects on SRAMs

Many investigations have been carried out on radiation e ects on SRAMs. Reed et al. [Ree08] showed that radiation can induce SBUs and MCUs on this kind of device. In recent technologies, reducing the cell area decreases the number of SBUs observed but increases the number and multiplicity of MCUs [Tip+06]. The authors in [Tsi+14b] discussed and categorized radiation e ects on a 90-nm COTS bulk SRAM under heavy ions, protons, and neutrons. They showed that SBUs, MCUs, and even some large-scale errors were observed.

Besides, other factors can increase the SEE sensitivity of devices, including incident angle of particles and bias voltage of the device. Clemente et al. [Cle+17] made a SEE sensitivity characterization of the COTS CMOS 16-Mbit SRAM CY62167EV30LL-45ZXI manufactured by In neon Technologies when turned on at ultra-low bias voltage under 14.2-MeV neutrons. Results showed an increase in the cross-section, signi cantly below 1.3V. The same research group has studied the response of three successive COTS SRAMs (130-nm, 90-nm, and 65-nm), manufactured by In neon Technologies, against 14.2-MeV neutrons at ultra-low bias voltage [Cle+18]. SBUs and multiple events with di erent multiplicities were observed. Another work investigated the behavior of the CY62167GE30-4 5ZXI bulk 65-nm COTS SRAM when powered up at low bias voltages at static and dynamic tests under 15.6-MeV protons [Rez+20]. Results indicate that the number of detected errors exponentially increases at bias voltages below 1V. SBUs and MCUs were observed in all the bias voltages.

One of the most important aspects that critically a ects the signature and typology of the events observed under radiation is the incident angle of the particles against the surface of the device. Indeed, several studies in the literature have reported that impinging particles (coming from di erent sources of radiation) at large incident angles feature a higher probability of provoking MCUs and MBUs. Thus, it has been largely proven that heavy ions [Hut+09; Tip+08a; Lee+15], low-energy protons [Dod+15; Hei+08; Ike+05] and neutrons [Tip+08b; Kat+19; Hir+15; Abe+19] produce a strong angular dependence of on SEU cross-sections of modern microelectronic devices, including SRAM-based ones.

3.2.2 SRAM-based Field Programmable Gate Arrays (FPGAs)

Features of SRAM-based FPGAs

Field Programmable Gate Arrays (FPGAs) are widely deployed in satellites and other spacecraft. Some reasons that explain this interest are the high performance, exibility, low cost, and long-term availability of such devices. FPGA technologies on the market are divided into three signi cant groups: SRAM-, Flash-, and Antifuse-based. Altera and Xilinx are the major manufacturers in developing SRAM-based FPGAs. The fundamental building blocks of Xilinx FPGAs are Con gurable Logic Blocks (CLBs), based on a matrix of CLBs connected through programmable interconnections. Among di erent FPGAs, SRAM-based ones are the most common in the market. They can contain up to several millions of logic cells and thousands of I/O pins [Xil18]. An essential aspect is that SRAM-based FPGAs are fabricated in standard CMOS processes that provide high-density devices at low cost and can be reprogrammable inde nitely. Hence, many resources are placed on the chip, including Digital Clock Managers (DCM), Phase-Locked Loops (PLL), Block RAMs (BRAMs), Data Signal Processors (DSPs), and Input/Output Blocks (IOBs). According to said features, this type of FPGA is a reasonable choice for space applications.

Radiation e ects on SRAM-based FPGAs

Several types of research in the literature have reported the e ect of radiation on COTS SRAM-based FPGAs. Authors in [Tam+15] present results for a Zynq-7000 to measure cross-section values vs. heavy-ion LET for its Con guration RAM (CRAM) and BRAM. In [Ton+17], the main contribution is the analysis of the angular e ects with low-LET heavy ions on the SRAM cells of a 28-nm SRAM-based Artix-7, which is the same device that we have used in this Ph.D. thesis. Signi cant di erences were also reported in the MBU cross-sections of CRAM and BRAM memory cells under particles hitting the device with di erent incident angles. Lee et al. [Lee+15] describe angular direct ionization events on SER predictions for a Xilinx Kintex-7 XC7V325T FPGA. Du et al. [Du+19] carried out tests on the same device by employing an ultrahigh energy heavy-ion beam available at CERN. The results reveal clusters of multiple large-scale events with di erent multiplicities occurring in the device's CRAM. Researchers in [Vla+21] also performed experiments on a Xilinx Zynq-7000 under very-high energy heavy-ion radiation and provided an analysis of the SEE vulnerability. The research demonstrated various SEE phenomena.

Experiments using high-energy electrons have also been conducted on FPGAs. In [Gad+17], authors investigated the electron-induced soft errors in a 28-nm bulk SRAM-based FPGA with energies above 9 MeV. The cross-section for the memory cells in the FPGAs was between 10^{-20}

and 10^{-17} cm^2/bit. The same authors also considered the sensitivity under 20-MeV electrons of different FPGAs (a Xilinx 45-nm Spartan-6 XC6SLX16 and a 28-nm Artix-7 XC7A100T) at the LINAC facility [Gad+15]. The electron-induced SEU cross-section for the memory cells in the FPGAs was found to be between 10^{-18} and 10^{-17} cm^2/bit.

Neutron-induced SEEs on this kind of FPGAs have also been studied. For instance, Bruni et al. [Bru+14] have studied the effect of power dissipation on a Xilinx 28-nm Zynq-7000 XC7Z020-CLG484-1. Experiments showed that the temperature variation induced by a higher operating frequency impacts the CRAM cross-section. Researchers in [WTH14] examined a Kintex-7 FPGA in the ATLAS Liquid Argon (LAr) Calorimeter at CERN against a broad spectrum of neutrons, protons, heavy-ions, and high-energy hadrons. The obtained results demonstrate that upsets occur at a rate of 1.1×10^{-10} upsets/bit/s in the CRAM and 9.6×10^{-11} upsets/bit/s in the BRAM. Rezzak et al. considered the SEE response of a 28-nm PolarFire MPF300TS FPGA, under neutrons and protons [Rez+18]. PolarFire is Microsemi's 5th generation, non-volatile SONOS[1]-based FPGA fabric. The response of this device against neutrons and protons showed immunity against SELs and no configuration upsets.

3.2.3 Non-Volatile Static Random-Access Memories (NV-SRAMs)

Features of nv-SRAMs

The nv-SRAMs are a category of NV-memory that merges SRAM characteristics with nonvolatility (providing more than 20 years of data retention). An nv-SRAM can grab and keep a duplicate of the SRAM data into an nv-memory when there is a loss of electric supply. One of the leading companies in the manufacture of such memories is Infineon Technologies. SONOS nonvolatile cells are built on a standard SRAM cell that uses standard CMOS process technology with another EEPROM cell to get the high performance of standard SRAMs, and non-volatility of data [Pra16], as shown in Figure 3.4 [Pra16].

SONOS technology uses Fowler-Nordheim Tunneling (FN Tunneling) to keep data by trapping charges in a sandwiched nitride layer. There are several key advantages of FN tunneling, including higher non-volatile (NV) endurance, much slower wear out, and ease of integration in CMOS. Each NV cell is located adjacent to a 6T SRAM cell, the transfers between the SRAM layer to the NV one all happen in parallel and at very low power levels. So-called "Store" and "Recall" operations are also implemented in these devices that can move data from the SRAM layer to the NV one and vice versa, respectively, as follows:

- Store: At power down, the data on the SRAM layer is automatically transferred to the non-volatile one.

[1] Short for Silicon - Oxide - Nitride - Oxide - Silicon

Figure 3.4: NV-SRAM Cell Architecture.

- Recall: Data are restored to the SRAM from the non-volatile layer at power up.

Radiation e ects on nv-SRAMs

A few researchers have studied the radiation e ects on nv-SRAMs. In [Liu+18], a DS1225 nv-SRAM manufactured by Dallas Semiconductor was tested under X-ray irradiation. Results yielded various errors regarding their exposure time. No e ect was observed on the data stored in the memory with an exposure time of less than 5 minutes. Longer times showed soft and hard failures. The device was recovered from soft errors when reprogrammed, while in hard errors, after power cycling, the memory was not recovered. Fullem et al. tested a 130-nm COTS non-volatile SRAM (CY14B104N) from In neon Technologies using heavy ions [FLC07]. Results showed that peripheral circuits induce a slight increase in upset cross-section. Also, SELs and SEFIs for 6T SRAM cells were seen. In the SONOS layer of the device, hard errors were observed at high LET conditions; and it was discovered that these errors can be annealed out after some time.

3.2.4 Ferroelectric Random-Access Memories (FRAMs)

Features of FRAMs

The concept of producing a memory based on ferroelectric materials rst emerged in the master thesis of an MIT student in 1952 [Buc52]; however, the rst implementation of a Metal-Ferroelectric-Semiconductor-Transistor (MFST) appeared in 1974. A common misunderstanding is that Ferro implies iron; in reality, ferroelectric memories employ no iron. Ferroelectric properties are available only below a speci c threshold temperature, named Curie temperature , and the material becomes paraelectric above it [Set+06]. The ferroelectric property is marked in a category of materials such as Lead Zirconate Titanate, $Pb(Zr_xTi_{1-x})O$,

Figure 3.5: Structure of Perovskite ferroelectric crystal and two polarization states a) on and b) o .

in short PZT. The PZT material can switch between two steady states by applying an electric eld. As depicted in Figure 3.5, the cation at the top and bottom is referred to as up and down polarization, respectively, thus making a memory bit [GP10].

After eliminating the electric eld, ferroelectric materials reveal a remanent polarization [Mik+01]; therefore, FRAM cells are non-volatile and they are able to keep the information in the memory without refreshing it. A higher electric eld and dielectric constant can yield a higher polarization e ect. Figure 3.6 depicts a typical polarization displacement (P D) hysteresis curve as a function of the electric eld. Some signi cant points can be noted from the curve: the permanent polarization points (P_R) exist where the applied electric eld is zero. V_C refers to the coercive eld, which is the eld to move the polarization to zero. P_S means the highest polarization. The two blue circles in the diagram demonstrate stable states with opposite polarization when the electric eld is null, representing 0 and 1 bits [GP10].

State-of-the-art FRAMs utilize two-transistor, two-capacitor (2T2C) memory cells. Such memory cells provide robust data retention reliability. The one-transistor, one-capacitor (1T1C) technology is an alternative that appeared in the market in 2001. It signi cantly improves the cost-per-bit ratio and uses a reference voltage in the architecture. Simpli ed schematics of 1T1C and 2T2C cells are displayed in Figure 3.7. Ferroelectric memories based on hafnium oxide (HfO_2) and Ferroelectric Tunnel Junction (FTJ) are objects of ongoing research [Mar21; CML94; MB95; BDC99].

In summary, the advantages and features that characterize FRAMs are:

- Read access time = write access time < 100 ns.

- Read energy = write energy.
- High write endurance 10^{14} cycles.
- Low power.

Figure 3.6: Hysteresis curve of ferroelectric materials.

Figure 3.7: Structure of a) 1T1C and b) 2T2C ferroelectric memory cells.

Besides, an extensive application base exists for FRAMs, such as in the automotive market, power metering systems, the business printer market, industrial applications, as well as wearable electronics and other energy-e cient applications [Cyp15].

Radiation e ects on FRAMs

Many researchers have investigated the radiation e ects on FRAMs quite extensively. Among these, one can classify the contributions discussing the e ects of heavy ions, protons, and TID e ects.

Devices FM1806 and FM1808, manufactured by Ramtron, were tested against heavy ions in [SG+02]. Wei et al. studied a 90-nm COTS FRAM (the FM28V100) manufactured by In neon Technologies, using heavy ions and a pulsed laser [Wei+19]. Stable upsets, transient upsets, and transient micro-latch-ups in peripheral elements were observed. Stable data upsets concerned several rows, and transient data upsets impacted from hundreds to thousands of rows. Zhang et al. [Zha+15] researched SEEs in two COTS FRAMs, the 256-kbit FM18W08 and the 4-Mbit FM22L16, again under heavy ions and a pulsed laser. This study reported at least six SEE classes: SBUs, MBUs, soft SEFIs, hard SEFIs, soft SELs, and hard SELs. The majority of the errors occurred in the peripheral circuitry. The impact of heavy ions was also analyzed on a 4-Mbit asynchronous FRAM manufactured by In neon Technologies (FM22L16) in a 130-nm CMOS process [Gup+15]. Results showed that this memory is susceptible to transient e ects in the peripheral circuitry. A team of NASA also investigated the Ramtron FM22L16 under heavy ions between a range of LETs from 2.7 to 54.1 MeV cm^2/mg at the TAMU Cyclotron [OBr+08]. The results indicate that SEUs and SEFIs happened during these tests. Also, the failure modes of a COTS 130-nm FM22L16 FRAM under heavy ions and pulsed focused X-ray beams were executed in [Bos17]. Mixed failure modes were observed in several types involving individual bits, isolated words, groups of pages, 1-bit-wide columns, entire regions of the memory array, and SEFIs.

Other research has focused on evaluating the SEE sensitivity of these memories under protons. Authors of [OBr+08] tested ve samples under protons with three energies (198, 140, and 89 MeV), where SEUs and SEFIs were detected. Zanat et al. also executed tests on several FM18L08 memories exposed to X-rays, and protons [ZWC08]. The authors detected stuck bits (or persistent SEUs) without any data failure at doses up to 9 Mrad (Si). Also, this study shows that the failure deeply depends on the irradiation temperature. Nuns et al. [Nun+07] tested the FM20L08 under 200-MeV protons, where some isolated SEUs were observed.

TID e ects on FRAMs have also been studied in the literature. Thus, Shen et al. [SLZ17] studied the e ects of TID on a 1-Mb parallel FRAM against Cobalt-60 rays, X-rays, and electrons. It was shown that the peripheral CMOS circuits were more sensitive to TID than the FRAM memory cells. Nuns et al. studied the behavior of the FM20L08 FRAM against TID at a Cobalt-60 facility [Nun+07]. Results revealed that failures happen because of using CMOS processes in the control circuitry. Ji et al. also researched the impact of TID in a Cobalt-60 source on the SEE sensitivity of 130-nm FRAMs [Ji+19a]. They reported that the detected errors in dynamic and static modes are grouped into ve categories: single bit errors, multiple bit errors, upsets in sequential (or similar) addresses, and long bursts of errors. Gu et al. [Ke+15] investigated the TID e ect on a 1-MB parallel FRAM prototype fabricated in

Figure 3.8: Illustration of an MRAM cell: a) structural perspective; b) schematic view (BL: bit line, WL: word line, SL: source line).

a 130-nm CMOS process. The function blocks, including the memory array, sense ampli ers, row decoder, column decoder, and I/O ports, were tested using an X-ray microbeam. This study revealed that the ferroelectric part is more robust against TID than the peripheral control circuitry. Also, the authors showed that the most sensitive part of the FRAM was associated with the sense ampli er.

Finally, in [Wei+19], a group of Devices Under Test (DUTs) was irradiated under 1-MeV neutrons with a uence of 5 10^{13} n=cm^2. After exposure, they operated normally. The ndings revealed that none of the direct and alternating currents (DC and AC) parameters were degraded using neutron irradiation.

3.2.5 Magnetoresistive Random-Access Memories (MRAMs)

Features of MRAMs

In MRAMs, bits are stored through Magnetic Tunnel Junctions (MTJs). An MTJ comprises a magnetoresistive layer with a xed polarization and an additional layer with a variable magnetic polarization (or free layer). Both layers are split by a thin dielectric tunnel that operates as a tunnel barrier [Mar13]. The design of an MRAM cell is illustrated in Figure 3.8 ([Yua13]).

An external magnetic eld can orient the free layer, whereas the reference one remains in a xed polarization. If the two layers of the MTJ are polarized in the same direction, the resistance of MTJ is low, indicating logic 0 ; in the case that the layers have di erent directions, the resistance of MTJ is high, showing logic 1 . When it comes to writing, for a reset operation, the di erential voltage between SL and BL is positive; and vice versa for a set operation [Yua13]. The read operation is accomplished by measuring the current magnitude via the access transistor at a given gate and drain voltage [SZ02].

The idea of storing data by magnetic polarization in memories dates back to the 1950s [Hon15]. In 1988, Grunberg et al. discovered giant magnetoresistance (GMR) [Grü+86], and the rst commercial MRAMs were invented as an improved version of the structure known as toggle MRAM in 2003 [Dur+03; Eng+05]. In recent years, considerable research on this technology has been conducted, including on toggle MRAMs, Spin-Torque Transfer (STT) MRAMs, and Thermal-Assisted Switching (TAS) MRAMs.

Generally speaking, STT-MRAMs are non-volatile memories that feature low voltage, high performance, scalability, remarkable endurance, and reliability compatible with other Back-End-Of-Line (BEOL) CMOS SRAMs [Mar21]. They also have an endless lifetime in reading and writing cycles, according to manufacturers [Gra11]. Chun et al. demonstrated the potential of STT-MRAMs as an alternative for high-density on-chip cache memories in [Chu+12]. Apalkov et al. [ADS16] presents an extensive review of the developments in MRAM technology over the past 20 years. A helpful work about the physics of STT-MRAMs was provided in [SZ02]. In [Agg+19] and [Nai+19], authors demonstrated a fully-functional 1-Gb standalone STT-MRAM on 28-nm CMOS and a manufacturable 22-nm FD-SOI 40-Mb embedded MRAM, respectively. Currently, aerospace, robotics, consumer electronics, and Internet-of-Things applications (IOTs) are interested in using STT-MRAM technology.

Radiation e ects on MRAMs

Various researches have been performed to study the radiation e ects on MTJ-based MRAMs. As yet, generally, results have indicated that MRAMs are quite robust against radiation e ects [Kat+18]. Although the MRAM memory cells are insensitive to radiation, some works such as [GP10; Nun+07] have demonstrated that the peripheral circuitry usually included in the chip to carry out I/O operations is susceptible to SELs and TID. In [NI07], SELs were observed at a LET as low as 7 MeVcm^2=mg, and a few read errors were observed with TID up to 60 krad(Si) in the MR2A16A device. Heidecker et al. tested MR0A08B manufactured by Everspin to a TID of 75 krad(Si); it was found that the device was resilient against SEUs [HAS10]. Also, results showed no latch-ups at an e ective LET of 84 MeVcm^2=mg.

Authors in [OBr+18] studied the SEE susceptibility of an AS008MA12A-C1SC, an 8-Mb STT-MRAM, under heavy ions. SEFIs with large numbers of bit ips happened at a LET of 1.84 MeV cm^2=mg and higher; however, they disappeared with a power cycle. Other research [Ing+19] studied the TID and heavy-ion responses of 55-nm non-volatile STT-MRAMs from Avalanche Technology. Results indicated that these devices were radiation tolerant. A 16-Mb MRAM device, UT8MR2M8, was tested under heavy ions accelerated to 15 MeV=amu [Haf+12]. No TID e ects (1 Mrad(Si)) and SELs (100 MeV cm^2=mg) were observed in this memory.

However, SEFIs were observed at a LET of 29.5 MeV$\cdot$cm^2/mg. Zhao et al. [Zha+19] investigated radiation effects of the 180-nm 4-Mbit MRAM (MR2A16AVYS35) under heavy ions. Hard Bit Errors (HBEs) were observed only when the energy was higher than 95.8 MeV.

Katti et al. [Kat+18] tested a 256-Mb STT-MRAM under heavy ions, and results proved no failures at energies as high as 84 MeV$\cdot$cm^2/mg. Kobayashi et al. [Dai+17] evaluated the influence of different kinds of heavy ions on a 10-nm CoFeB-MgO MTJ-based MRAM. Their findings demonstrated that recoverable bit flips appear at a threshold LET of about 15 MeV$\cdot$cm^2/mg. Xiao et al. [Zha+21] evaluated the displacement damage on modern pMJT-based STT-MRAMs against 3-MeV Ta ions with fluences ranging from 10^9 to 10^{14} ions/cm^2. No upset was observed at fluences lower than 10^{11} ions/cm^2; however, the structural damage at the CoFeB/MgO interface gradually degrades at higher fluences.

Other works have been devoted to studying the radiation effects of protons on MRAMs. For instance, in [Nun+07], the MR2A16A MRAM was tested under 200-MeV protons, resulting in being quite robust. Hughes et al. [Hug+12] irradiated STT film stacks and devices using 2-MeV and 220-MeV protons. Results did not reveal any changes in parameters of bit-state, retention, current-in-plane tunneling, or ferromagnetic resonance.

Finally, radiation effects of gamma rays and neutrons on MRAMs have also been studied in the literature. Thus, Ren et al. [Ren+12] investigated the gamma-ray and neutron radiation tolerance on MgO-based MTJs. The material was highly tolerant to gamma rays and epithermal neutrons at a fluence of 2.9×10^{15} n/cm^2. Tsiligiannis et al. [Tsi+13] also made static and dynamic tests on a 4-Mbit 180-nm commercial toggle MRAM using neutrons with energies of 25, 50, and 80 MeV and under a Californium-252 alpha source. Also, researchers in [Zha+19] studied radiation effects on a 180-nm 4-Mbit MRAM (MR2A16AVYS35), using gamma rays. The results showed no clear effects. The memory was soft-error resilient in static mode, and more sensitive when dynamic tests were made. Regarding radiation effects provoked by thermal neutrons on COTS MRAMs, to the best of the authors' knowledge, no results were found in the literature. However, pMTJs with sizes relevant for STT-MRAM applications have been found to be resilient to very high fluences of thermal neutron radiation [Mon+20].

3.2.6 Resistive Random-Access Memories (ReRAMs)

Features of ReRAMs

The primary theory of the memristor (a contraction for "memory resistor") device was introduced by professor L. Chua in 1971 [Chu71]. Theoretically, this study presented a fourth fundamental passive element as a new two-terminal circuit element called a memristor. It is illustrated by the relationship existing between the charge and the flux linkage. In 2008,

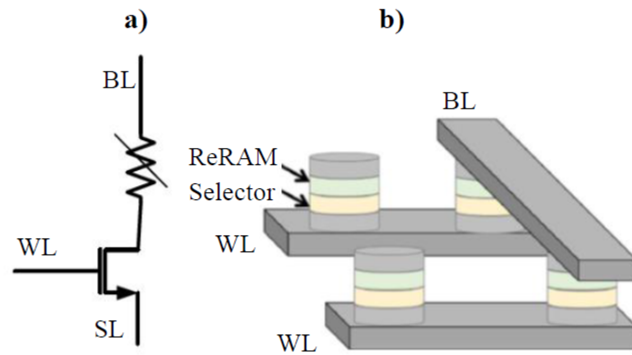

Figure 3.9: *a) Schematic of a 1-transistor-1-resistor (1T1R) configuration, b) description of a crosspoint architecture schematic, with the selector and the ReRAM cell.*

the first memristor device was fabricated. Strukov et al. created a TiO_2 layer, which was sandwiched between two platinum (Pt) electrodes [Str+08]. The proposed physical device employed resistance as a variable to express its state; this is why it was called an RRAM or ReRAM. Between 2005 and 2015 was the golden period of ReRAM investigation.

Generally speaking, a ReRAM cell is made of a metal oxide layer, most commonly titanium oxide (TiO_2), tantalum oxide (TaO_x), hafnium oxide (HfO_x) or tungsten oxide (WO_x) that is sandwiched by two metal electrodes [Yua13; Phi+12]. When the ReRAM cell is first manufactured, it is initially in the High Resistance State (HRS). Applying an external voltage pulse across the ReRAM cell allows a transition of the device from HRS (or OFF state) to a Low Resistance State (LRS) (or ON state) to represent the logical "0" and "1", respectively. The voltage is applied to the Bit Line (BL) in the "set" operation and connects the Source Line (SL) to the ground. In the "reset" operation, a voltage (VRESET) is applied to the SL and ties the BL to ground [Yua13; Zah+20] as depicted in Figure 3.9 ([GBK17]). ReRAMs are non-volatile memories since LRS and HRS keep their values even after removing the external voltage supply.

The advantages of ReRAMs are listed below [Abd18]:

- Small size.
- Low power consumption.
- Non-linear current-voltage (I-V) characteristics (ReRAMs are programmed in a period of tens of nanoseconds).
- Analog behavior is due to the device having many intermediate resistive states.

Lastly, ReRAMs are broadly employed in significant applications, such as crossbar RAM arrays, as well as low-power SRAM designs and sequential circuits [Abd18].

Radiation effects on ReRAMs

Some works have studied TID and SEEs on devices based on TiO_2, TaO_x, and HfO_2. Gonzalez et al. in [GBK17] provided a comprehensive review of radiation upsets on bipolar resistance-switching ReRAMs. This study indicates that these memories are naturally robust against different types of ionizing radiation since they do not directly interact with said radiation.

Bennett et al. [Ben+14] examined and modeled SEEs in 1T1R Hf/HfO_2-based ReRAM cells under heavy ions at different bias voltages. The results demonstrated that ReRAM cells are only sensitive in the high resistance state when a voltage higher than 0.65V was employed at the BL. Besides, it was found that individual ions are capable of changing the ReRAMs' resistance to provoke multiple events. Another research was presented by Alayan et al. [Ala+17], who irradiated HfO_2-based ReRAMs under heavy ions. Their findings show that these cells are resistant to SEEs when idle, but they were sensitive against radiation during a read operation. Further examinations in [Che+14] investigated the Panasonic MN101L, an 8-bit microcontroller with embedded ReRAM against heavy ions and a pulsed laser. SEFIs were observed in the microcontroller due to the structure of the ReRAM consisting in CMOS elements in their peripheral control circuits. Lyu et al. in [He+21] studied the MB85AS4MT (the same memory studied in this study), produced by Fujitsu, under heavy ions at a tandem accelerator and a cyclotron in an atmospheric environment. Results revealed that no SEUs nor SELs were observed in the memory under Xe ions (LET was 65 MeV·cm^2/mg). SEFIs happened in the peripheral circuitry of the device when the memory was irradiated with F-ions, Cl-ions, and Ge-ions at LETs of 4.4, 13.1, 3.73 MeV·cm^2/mg, respectively.

Authors in [Bi+19] performed tests on a 4-Mbit commercial ReRAM from Fujitsu, MB85AS4MT, to investigate TID effects by a Cobalt-60 source and SEEs provoked by heavy ions and a pulsed laser. Numerous SEFIs in this device were found under heavy ions, and a subsequent pulsed-laser scanning confirmed that events were located in its peripheral circuitry. Maestro-Izquierdo et al. also tested TiN/Ti/HfO_2/W ReRAMs in a cobalt-60 source [Mae+21]. Results evidenced that ReRAM cells are hardened against gamma radiation, which is consistent with other previous works.

More considerable research has been accomplished, such as TID studies on a TaO_x-based device under X-rays [Mar+12]; as well as gamma rays and 10-keV X-ray irradiation at IMEC on 55-nm HfO_2/Hf devices [Bi+13]. Similarly, more studies have assessed the effects of gamma irradiation on HfO_x-based memory cells [Fan+14] and 1-Mrad(Si) exposure on a CMOS-integrated HfO_x-based cell [Wee+14]. Generally, findings did not reveal any significant change in switching properties.

3.3 Communication protocols

In state-of-the-art SoCs, communication is generally used for transmitting data. It offers several advantages when compared to parallel ones, such as circuit simplicity, component pin usage, and higher speeds. The memories studied in this Ph.D. thesis employ different serial communication protocols, including I^2C, SPI, and Quad SPI [MSR15].

- I^2C: This protocol uses two wires, a Serial Clock Line (SCL) and a Serial Data Line (SDA). I^2C is a synchronous protocol, and multiple master and slave devices are connected to the same bus [Sem18]. The slave ones must have a unique address to identify themselves that is usually composed of a 7-bit signal followed by a Read/Write (R/W) bit. The current master device controls the I^2C bus while it drives the clock line and can write the bus or read from it. Slave devices access the data line when the clock signal is driven by the master. Data communication is half duplex since both processes (reads and writes) are carried over the SDA line. There are bus arbitration procedures in multi-master environments to prevent multiple devices from operating as bus-master at the same time. Each message produced by a master must start with a "start condition" and end with a "stop condition". Thus, a message is thus composed of the following elements:
  - Bus stop (or repeated start).
  - Device ID of the recipient of the message + R/W bit.
  - Data bytes + acknowledgement (as many as required by the device, this is device-dependent).
  - Stop condition (or repeated start = stop + start).
- SPI: The SPI protocol is a synchronous serial data standard that is used to communicate a microprocessor with other microprocessors or Integrated Circuits (ICs) such as memories. The SPI is a master/slave protocol based on four lines [ik09]:
  - Clock line (SCLK)
  - Master In, Slave Out (MISO)
  - Master Out, Slave In (MOSI)
  - Chip/Slave Select (CS/SS)

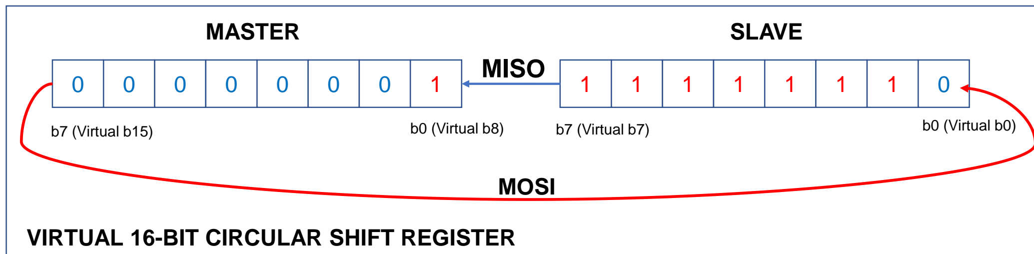

Figure 3.10: *Virtual 16-bit circular shift register of an SPI communication*

The master chooses each slave device by driving its Chip Select (CS) line low. SPI transmits data by using a serial shift register. When a slave is selected, the shift register operates as a virtual 16-bit circular shift register. Figure 3.10 depicts the circular behavior of an SPI transmission. Once a clock pulse is sent by the master, a shift happens.

Finally, a comparison between both protocols is illustrated in Table 3.1.

Table 3.1: *Comparison I^2C and SPI protocols*

I^2C	SPI
Multi-master and multi-slave.	Multi-slave and not a multi-master.
Half-duplex.	Full-duplex.
Feature of clock stretching.	Clock stretching is not supported in SPI.
Slower than SPI.	Faster than I^2C.
Consuming more power than SPI.	Using less power compared to I^2C.
Less susceptible to noise than SPI.	More susceptible to noise than I^2C.
Cheaper to implement than SPI.	Costly compared to I^2C.
Using a pull-up resistor.	No requirement of a pull-up resistor.
Ensuring sent data is received by the slave device.	Not verifying data is received or not.
Better for a long-distance.	Better for a short distance.

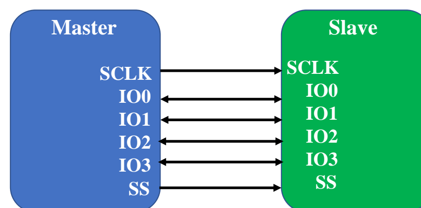

Figure 3.11: *Example of a Quad SPI setup with single slave*

- Quad SPI (QSPI): A quad I/O SPI has a 4-bit data bus interface, and hence it can improve throughput by four times with respect to SPI. With increased bandwidth supported by the multi I/O SPI devices, it can be applied to a much more comprehensive range of applications demanding higher performance [MSR15]. Figure 3.11 shows an example of a Quad SPI setup with a single slave.

Chapter 4

Experimental setup

This chapter will present the test setup of the FPGA and memories that were studied (Section 4.1), the test methods for carrying out the experiments (Section 4.2), the facilities used in this Ph.D. thesis (Section 4.3), and techniques of processing the data issued from the radiation-ground experiments (Section 4.4).

Table 4.1: *Tested devices*

<table>
<tr><th>Manufacturer</th><th>Device</th><th>Type of device</th><th>Technology process</th><th>Density</th></tr>
<tr><td rowspan="4">Infineon Technologies</td><td>CY14V101QS</td><td rowspan="2">nv-SRAM</td><td rowspan="2">bulk 130-nm + SONOS</td><td rowspan="2">1-Mbit</td></tr>
<tr><td>CY15B101J</td></tr>
<tr><td>CY15B102Q</td><td rowspan="2">FRAM</td><td rowspan="2">130-nm</td><td>2-Mbit</td></tr>
<tr><td>CY15B104Q</td><td>4-Mbit</td></tr>
<tr><td rowspan="2">Fujitsu</td><td>MB85AS4MT</td><td rowspan="2">ReRAM</td><td rowspan="2">180-nm</td><td>4-Mbit</td></tr>
<tr><td>MB85AS8MT</td><td>8-Mbit</td></tr>
<tr><td rowspan="2">Everspin</td><td>MR10Q010CSC</td><td rowspan="2">MRAM</td><td>180-nm</td><td>1-Mbit</td></tr>
<tr><td>MR25H40CDF</td><td>130-nm</td><td>4-Mbit</td></tr>
<tr><td>Xilinx</td><td>Artix-7 XC7A100T</td><td>FPGA</td><td>bulk 28-nm</td><td>28,61-Mbit</td></tr>
</table>

4.1 Selected devices and test setups

Table 4.1 shows the devices tested against radiation in this Ph.D. thesis. The following subsections will describe these devices in greater detail.

4.1.1 nv-SRAM (CY14V101QS)

This part is manufactured by Infineon Technologies and has a capacity of 1 Mbit. The memory is organized as two layers of 1 Mb each, one consisting of 130-nm CMOS SRAM and the other

one, nonvolatile SONOS Quantum Trap cells [1], as explained in Section 3.2.3. The memory is accessed through SPI and read/write operations are carried out at a clock frequency that can reach up to 108 MHz. The SRAM layer is manufactured in 130-nm bulk CMOS technology [Tec17]. This memory features bit interleaving, which has been unscrambled by using proprietary information provided by the manufacturer.

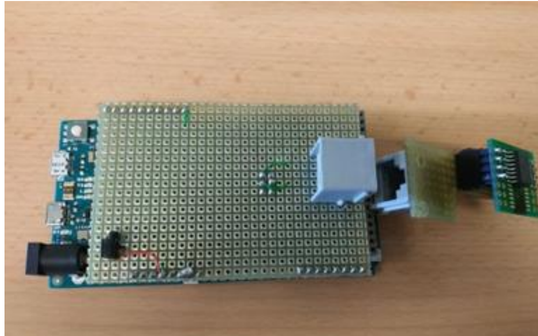

Figure 4.1: *Experimental setup for the CY14V101QS nv-SRAM.*

The test system, as shown in Figure 4.1, comprised an Arduino DUE, which runs the test software, and an extension board with the memory under test. An additional control computer was responsible for the data retrieval. The Arduino communicates with the control computer through a universal asynchronous receiver/transmitter (UART), whereas the ARM Cortex-M3 microcontroller of the Arduino communicates with the SRAM through SPI. In order to obtain reliable results, all the elements of the setup existing in the irradiation chamber were shielded with thick polyethylene plates except the DUT.

4.1.2 nv-SRAM (CY14B101J)

This device integrates a 1-Mbit nv-SRAM with a nonvolatile element in each memory cell and has a capacity of 128K×8 bits. As the CY14V101QS (described in Section 4.1.1), the embedded nonvolatile elements are also implemented with Quantum Trap technology. The memory is accessed through an I^2C interface, and read/write operations are accomplished at a clock frequency that can reach up from 100KHz up to 3.4MHz [Tec18].

The test system for this memory differs from the one used for the CY14V101QS memory, as shown in Figure 4.2. It was composed by an Arduino DUE, which executed the test software. A control computer was used for the data retrieval. The Arduino communicated with it by means of a UART. A shield Printed Circuit Board (PCB), connected on top of the Arduino, was designed to correctly route the I/O pins of the memory, as well as to provide a variable bias voltage to it. A daughterboard with 2 sockets was also developed for hosting the memories, and

[1] The embedded nonvolatile elements integrate the so-called "Quantum Trap" cells, providing reliable storage of data

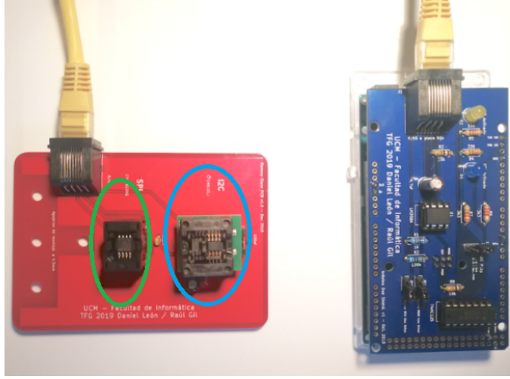

Figure 4.2: *Experimental setup for the for the CY14B101J nv-SRAM and for the CY15B102Q / CY15B104Q FRAMs. For the former, the socket to the right is used instead (blue circle). For the latter, the socket to the left is used (green circle).*

it was connected to the Arduino by means of a CAT6 twisted pair cable. One of the sockets is used to place the memories with the I^{2}C interface, and the other was used for the devices that are working with SPI.

4.1.3 FRAMs (CY15B102Q and CY15B104Q)

Two FRAMs were examined: the 2-Mbit CY15B102Q (256K×8 bits) and the 4-Mbit CY15B104Q (512K×8 bits). Both memories employ an advanced ferroelectric process in 130-nm bulk technology manufactured by Infineon Technologies [Cyp15]. Bitcells at the CY15B102Q are implemented with a 2T2C structure, whereas those of the CY15B104Q implement a 1T1C structure instead. Both devices are accessed through a high-speed SPI, and they present high reliability, low power consumption, as well as the following features:

- High endurance: 10^{13} reads/writes for the CY15B102Q, and 10^{14} reads/writes for the CY15B104Q.
- 121-year and 151-year data retention for the CY15B102Q and CY15B104Q, respectively.
- Maximum operating frequency up to 25 MHz and 40 MHz for the CY15B102Q and the CY15B104Q, respectively.

The test system used for these memories is the same as the one previously described in Figure 4.2. The only difference is that the SPI socket will be used for FRAM memories.

4.1.4 MRAMs (MR10Q010CSC and MR25H40CDF)

Two nonvolatile 180 and 130-nm toggle MRAMs (MR10Q010CSC and MR25H40CDF), manufactured by Everspin, were also studied in this Ph.D. thesis.

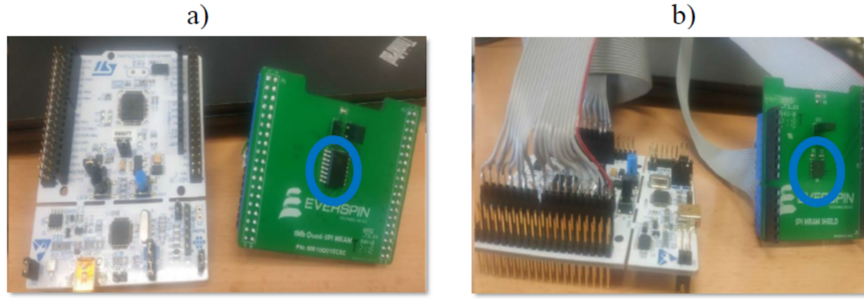

Figure 4.3: *Experimental setup for the MRAMs (colored circles indicate the location of memories) a) the MR10Q010CSC, and b) the MR25H40CDF.*

For testing the MR10Q010CSC, an MR10Q010-EVAL1 evaluation board (also provided by Everspin) was used (see Figure 4.3a). It has been designed to work with the NUCLEO-L476RG MCU board from ST Microelectronics [Eve16a]. The MR10Q010CSC has a capacity of 1 Mb (128K×8 bits), and it is accessed through Quad SPI.

Besides, a computer with Internet access and a Universal Serial Bus (USB) port (with standard A to mini B connectors) is needed to connect the evaluation board to the computer. An online workspace on the Mbed website [2] is necessary to upload the code to the memory.

For testing the MR25H40CDF, another evaluation board was also provided by Everspin (this time, the MR25H00-EVAL, see Figure 4.3b). It is compatible with the Arduino UNO pinout [Eve16b]. In this case, the NUCLEO-F411RE MCU board from ST Microelectronics was employed for using it. The rest of the setup description is the same as for the MR10Q010CSC. The most important features of these MRAMs, according to Everspin, are listed below [Eve18; Eve20]:

- Data retention greater than 20 years.
- Automatic data protection on power loss.
- Unlimited write endurance.
- Low-current sleep mode.

4.1.5 ReRAMs (MB85AS4MT and MB85AS8MT)

The ReRAMs under test were the 4-Mbit MB85AS4MT and 8-Mbit MB85AS8MT, manufactured by Fujitsu, which feature memory layouts of 512K×8 bits and 1M×8 bits, respectively. The most significant features of these memories are described below:

- High data endurance: 1.2×10^6 times/byte.

[2] http://developer.mbed.org/

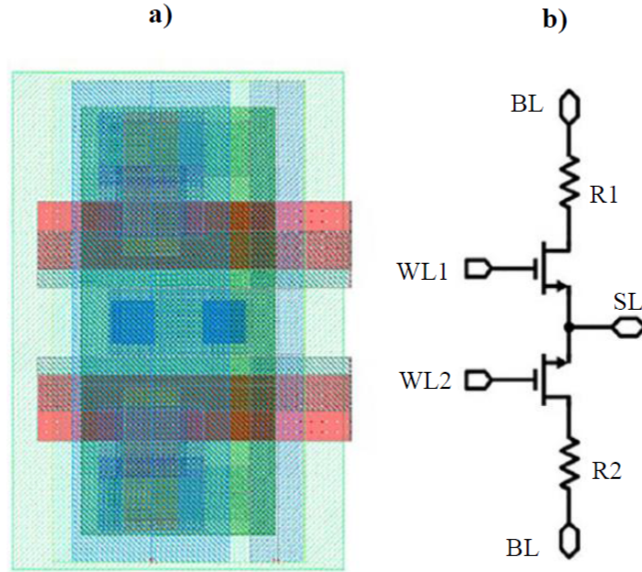

Figure 4.4: *a) Layout and b) schematic of the memory cells of the MB85AS4MT that was evaluated under radiation [Bi+19].*

- They work by SPI communication protocol.
- Data retention stands for 10 years (+85° C).
- Operating power supply voltage ranges from 1.65 V to 3.6 V.
- The maximum frequency is 5 MHz for the MB85AS4MT and 10 MHz for the MB85AS8MT.

The MB85AS4MT device features TaOx-based cells, which consist in a two-transistor, two-resistor (2T2R) structure, with a common source as depicted in Figure 4.4. The test system is the same as used for the nv-SRAMs and FRAMs (Figure 4.2), as ReRAMs are placed in the SPI socket.

4.1.6 Artix-7 XC7A100T FPGA

An Artix-7 XC7A100T FPGA embedded into a Nexys-4 DDR board was also studied in this thesis. The device contains 15,850 logic slices, each with four 6-input Look-Up Tables (LUTs), 8 FFs, and 4,860 Kbits of fast BRAM, from which 540 Kb to execute ECC and six clock management tiles.

4.2 Test methods

Different test methodologies were carried out on the DUTs to assess their sensitivity to upsets. In this thesis, static and dynamic tests were carried out, which are described below.

1. Static tests: They are accomplished by initializing a specific pattern on the DUT's memory cells before exposing them to radiation. During irradiation, the device is powered but dropped in an idle mode; and after turning off the beam, the DUT's memory cells are read and compared with expected values. The whole memory array is written with either "all 0", "all 1", or "logical checkerboard."

   It is worth mentioning that, for memories containing volatile and non-volatile parts (i.e., the CY14V101QS and the CY15B101J), a different technique was used for testing the non-volatile part. In this case, during irradiation, the device was turned off and turned on after powering off the beam. The rest of the process was the same as described above.

2. Dynamic tests: In these tests, several consecutive read operations are carried out on the whole memory while the device is under irradiation. The idea is that specific algorithms cause conditions to increase the sensitivity of the device against SEEs. Dynamic tests were performed as described below [Tsi+14a; Dil+04]:

   - Dynamic Stress (March DS):

     $$\uparrow(r1,w0,r0,r0,r0,r0,r0);$$
     $$\uparrow(r0,w1,r1,r1,r1,r1,r1);$$
     $$\uparrow(r1,w0,r0,r0,r0,r0,r0);$$
     $$\downarrow(r0,w1,r1,r1,r1,r1,r1);$$
     $$\downarrow(r1,w0,r0,r0,r0,r0,r0);$$
     $$\uparrow(r0,w1,r1,r1,r1,r1,r1)$$

   - March C:

     $$\uparrow(w0);\uparrow(r0,w1);\ \uparrow(r1,w0);$$
     $$\downarrow(r0,w1);\ \downarrow(r1,w0);\ \uparrow(r0)$$

March algorithms are constituted by several elements. Each element (shown in the "(...)" bracket pair) and its operations are applied to the entire memory space, and only then the algorithm advances to the next cycle. Operations can be read (indicated as 'rX') or write (indicated as 'wX'). X can be 0 or 1, indicating the information that is written or expected to be read. Each element is applied in an ascending (↑) or descending (↓) order on all memory addresses. It is worth mentioning that, in March DS, a 'w1' operation is needed before starting the irradiation of the DUT.

Table 4.2: *Rounds of irradiation carried out in different facilities*

Facility	DUTs	Date
GENEPI2 (14.2-MeV neutrons)	nv-SRAM (CY14V101QS) FPGA (Artix-7 XC7A100T)	November 2017 and May 2018
CNA cyclotron (15.3-MeV protons)	FRAMs (CY15B102Q/CY15B104Q) nv-SRAMs (CY14V101QS/CY14V101J)	February 2019
CNA Tandem lab (1-MeV protons)	ReRAM 4-Mbit (MB85AS4MT) FRAMs (CY15B102Q/CY15B104Q)	June 2021
TENIS (25-meV thermal neutrons)	FPGA (Artix-7 XC7A100T) FRAMs (CY15B102Q/CY15B104Q) nv-SRAMs (CY14V101QS/CY14V101J) ReRAMs (MB85AS4MT/MB85AS8MT) MRAMs (MR10Q010CSC/MR25H40CDF)	March and September 2021
PIAF (14.8-MeV neutrons)	nv-SRAM (CY14V101J) FRAMs (CY15B102Q/CY15B104Q) ReRAMs (MB85AS4MT/MB85AS8MT) MRAMs (MR10Q010CSC/MR25H40CDF)	November 2021

4.3 Test facilities

This section provides details of the different radiation facilities used to perform tests and measure the SEE sensitivity of the devices that are discussed in this Ph.D. thesis. Table 4.2 describes in detail all the campaigns that were made. The subsections below will refer to the facilities in the first column of this table.

4.3.1 GENEPI2 facility at the LPSC

Two tests, made in November 2017 and May 2018, were run at the GENEPI2 neutron source (Figure 4.5)., which is operated at the LPSC (Laboratoire de Physique Subatomique et de Cosmologie) in Grenoble (France) [Vil+14; Vil+16]. This accelerator is under operation on the GENESIS platform (GEnerator of NEutrons for Science and IrradiationS). GENEPI2 is an electrostatic accelerator producing neutrons by impinging a deuteron beam onto a fixed target. With a Tritium (T) target, neutrons are produced via the nuclear fusion reaction ${}_1^2D +_1^3 T \rightarrow_0^1 n +_2^4 He$ with an average energy of 14.2 MeV. An ion source, operating at the electronic cyclotronic resonance, produces an intense and continuous deuterium (D) ion beam. A series of electrodes shape the beam, which is accelerated to 220 keV through an electrostatic column. After magnetic selection by a dipolar electromagnet, deuterons are guided through a 5

meter long transport line, including focusing and steering elements. The beam line terminates with the target made of a tritium compound. From the production target, neutrons are emitted in all directions. For the radiation tests, the devices under test are set facing directly the tritium target, at a small distance determined according to the required neutron flux. The neutron production is monitored continuously throughout experiments to determine the dose for each irradiation (accuracy better than 15%).

Figure 4.5: *GENEPI2 neutron source.*

4.3.2 Cyclotron at the CNA

A proton irradiation campaign took place in February 2019 at the Centro Nacional de Aceleradores (CNA), Sevilla (Spain). The experiments were performed using the external beamline installed in the 18/9 IBA compact cyclotron laboratory. The devices were placed at 50 cm from the exit nozzle with a 100 μm aluminum foil as a window; so that the final energy of protons at the surface was 15.3 MeV, whose estimated spread stood on the order of 400 keV. The final energy of the incident beam was obtained using the energy loss data calculated with the SRIM2013 code [ZZB10].

The proton flux monitoring was performed by measuring the beam current into an electrically isolated graphite collimator (1 cm of diameter) behind the exit window. A medium flux value was computed in the base of the pulses registered by the counter. Finally, the fluence at the DUT was calculated depending on the exposure time for each run.

Despite the low proton energy, the different device technologies were sensitive enough without delidding them. Furthermore, previous tests conducted by the CNA group with similar devices indicate that the covering (epoxy or similar) thickness on the order of 900-μm as maximum allows working with incident proton energies on the order of 15 MeV to study SEEs in technologies below 130-nm [Rez+20; Rez+22]. FRAMs and nv-SRAM memories during the irradiation campaign at CNA are displayed in Figure 4.6.

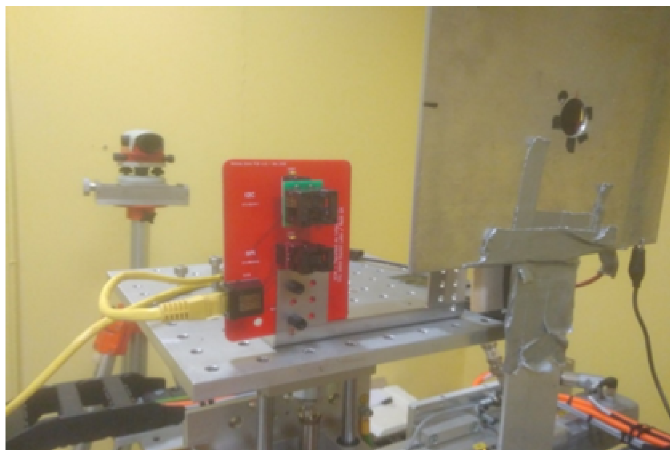

Figure 4.6: *Setup for the irradiation of the nv-SRAM and FRAMs at the CNA.*

4.3.3 Tandem laboratory at the CNA

The irradiation beamline of the 3-MV Tandem Pelletron installed at the CNA [Mor+18] was used to perform an irradiation campaign in June 2021. The campaign was performed with protons at an energy of 1.02 MeV ±1%, obtained in base to the last calibration of the tandem accelerator (October 2020, internal document). The irradiation was performed at room temperature, and the pressure into the chamber was in the range of 1×10^{-6} mbar. The proton energy at this facility can be configured to a value ranging from 1 to 6 MeV. In this case, it was set to 1 MeV.

The DUTs were fitted in the specific sample holder designed and manufactured to be used in the vacuum chamber of the Tandem CNA laboratory. First, the particle beam is focused on the scintillator placed in the sample holder to obtain a homogeneous spot with a size of 1 cm^2. Afterward, scanning with a magnetic system increases the full irradiation area. The total fluence is calculated based on the value of the particle density integrated into the complete area. During the focalization process of the beam, only the scintillator was exposed; the samples remained masked behind the slits and one extra aluminum foil, which stops the beam. Complete scanning of 15 cm × 15 cm was established in this case. The current intensity was measured "in vivo" on the conductive slits and full sample holder, using a Brookhaven 1000C current integrator in the 0.5-nA over 20-nA sensitivity scale.

4.3.4 TENIS facility at the ILL

Two radiation-ground campaigns were performed at the new Thermal and Epithermal Neutron Irradiation Station (TENIS) hosted by the Institut Laue-Langevin (ILL) in March and September 2021. TENIS replaced D50 as a facility where thermal neutron experiments were executed at the Platform for Advanced Characterisation of Grenoble (PAC-G) [Weu+18; Bea+15].

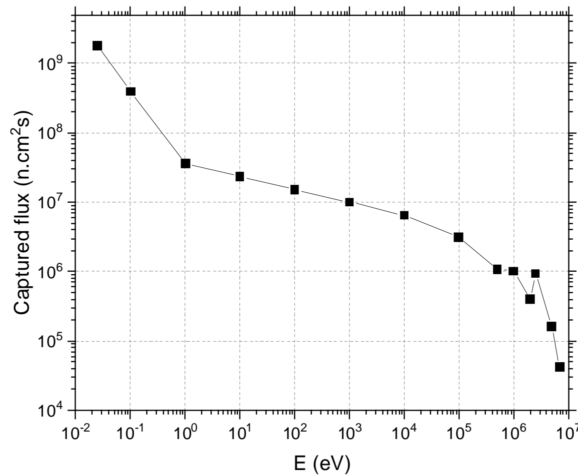

Figure 4.7: *Monte Carlo N-Particle (MCNP) calculated neutron energy spectrum on the TENIS beamline at the ILL high flux reactor.*

TENIS has a fission-like neutron energy spectrum with a main component of thermal neutrons. Figure 4.7 directs the Monte-Carlo N-Particle (MCNP) calculated neutron energy spectrum TENIS beamline at the ILL with a high flux reactor.

At the beam exit, a captured flux of 2.86×10^9 n/cm^2/s at nominal reactor power (58 MW) was measured using gold foil activation. The sample position was 49.4-cm away, leading to an estimated captured flux of 2.1×10^9 and 2.4×10^9 n/cm^2/s, in two campaigns, March (reactor power 43 MW) and September 2021 (reactor power 54 MW), respectively. Figure 4.8 shows a view of the FPGA under irradiation under thermal neutrons at the ILL.

Figure 4.8: *Setup for the irradiation of the FPGA at the ILL.*

Table 4.3: *Informational data on the monoenergetic neutron field used at the PIAF*

Reaction	Target	E_n (MeV)	ΔE_n (keV)	Φ_{sc}/Φ_{dir} ($\times 10^{-3}$)
$^3H(d,n)^4He$	Ti(T) 1 mg/cm^2	14.8	435	(2.8 ± 0.7)%

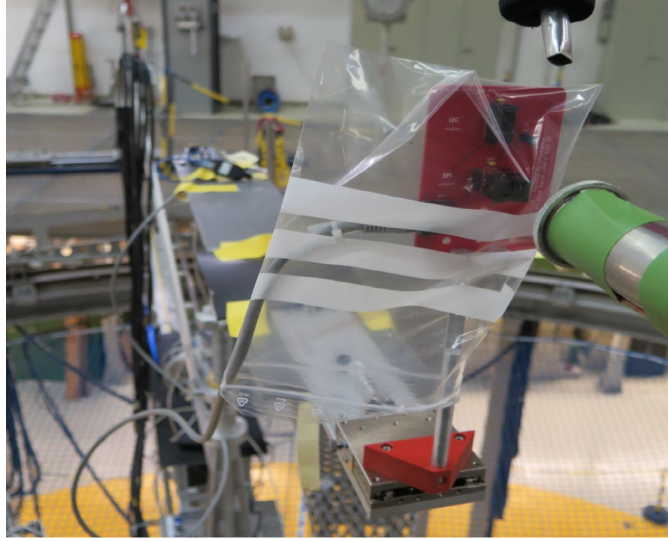

Figure 4.9: *Setup for the irradiation of the memory chips at the PIAF.*

4.3.5 PTB Ion Accelerator Facility (PIAF)

More tests were performed under a monoenergetic 14.8-MeV neutron beam at the PIAF, in November 2021.

- Irradiation conditions: The monoenergetic neutron fields were produced according to the general recommendations of the ISO standards [ISO01; ISO02; ISO98]. More details on the production and characteristics of the neutron fields are given in Table 4.3. The mean energy, E_n, and the Full Width at Half Maximum (FWHM), ΔE_n, of the direct neutron distribution are nominal values.

  Tests were performed in open geometry in the low-scatter measurement hall ($24 \times 30 \times 14 m^3$) of the PIAF, at an ambient temperature of (21.5±1.0)°C. Different PCBs were used to mount the memory chips, which were replaced every time the DUT had to be changed. These were mounted free in the air for each measurement. The distance between the surface of the memory chip and the neutron production target backing was 5.0 ± 0.1 cm. The Printed Circuit Boards (PCBs), including the memory chips, were covered with a thin plastic bag to avoid contamination, as shown in Figure 4.9.

- Determination of the neutron fluence: The total neutron fluence Φ is the sum of the

fluence Φ_{dir} of the direct neutrons in the target and the fluence Φ_{sc} of neutrons scattered in the target assembly. The value of Φ_{dir} was determined using a De Pangher long counter (details of the measurement and analysis procedures are described in [Nol18]), whereas the value of Φ_{sc} was calculated using the Monte Carlo code TARGET [Sch05]. The ratio Φ_{sc}/Φ_{dir} is listed in Table 4.3.

4.4 Data processing

This section presents the methods used to extract SBUs and multiple events, as well as to estimate false multiple events as a result of the accumulation of simpler ones.

4.4.1 Extracting SBUs and MCUs from a large set of results

Memories with old technologies were manufactured by placing the bits belonging to a word in physically adjacent cells, which caused the possibility of MBUs occurring. Therefore, standard ECCs were not able to recover them. The manufacturers solved it with bit interleaving, which consists in placing bits from the same word physically far from each other. Figure 4.10 shows an interleaving model. Thus, this technique prevents single particle effects on several bits of the same word. Unlike MBUs, simple ECC methods can recover MCUs. Unfortunately, the information regarding how said interleaving is made is usually unknown to researchers. Therefore, if a large number of events is observed in a radiation-ground experiment, it is a huge challenge to identify MCUs among the set of events that were observed.

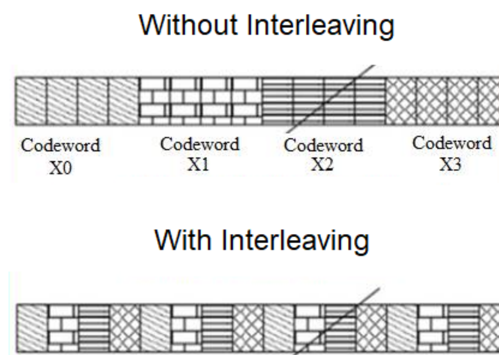

Figure 4.10: *An interleaving model.*

There are two techniques to categorize bitflips into SBUs and MCUs in radiation experiments: a) knowing the memory's physical layout or b) investigating statistical anomalies existing in the

set of bitflips observed with respect to a theoretical scenario where only SBUs can occur. In the first case, the manufacturer must provide proprietary information about the layout to create a function relating the logical address of the flipped cell with the physical position on an XY plane. Thus, two flipped cells separated by a distance lower than a threshold value, such as Manhattan Distance (D) technique [Cra17], will be considered originating in a single particle impact. This technique has been used by many authors for analyzing experimental results issued from radiation-ground experiments [Cle+17; Bos+15; Bos+16]. The second choice consists in combining logical addresses in pairs (e.g., XORing [FP07] or subtracting [Wir+14; Han+11]) to detect the values that appear more often than expected and, hence, show the existence of probable MCUs. Anomalously repeated values are used to merge addresses in pairs and, this way, discover related bitflips [Cle+16; Fra+17]. The main benefit of this technique is that researchers do not need any proprietary information about the memory layout. Thus, gathering enough experimental data lets the finding of anomalously repeated XOR'ed or subtracted values in order to group bitflips into SBUs and MCUs.

In order to analyze the data that have been issued from the experiments made in this thesis, both techniques have been used. The former was used whenever the manufacturer provided confidential data about the internal implementation of the interleaving, but for the rest of the cases, the statistical approach was used. This statistical approach was implemented in a user-friendly tool called LELAPE [Cle+16; Fra+17]. LELAPE is the Spanish acronym for "Listas de Eventos para Localizar Anomalías Preparando Estadísticas," which in English means LAELAPS ("Lists of All Events for Locating Anomalies by Preparing Statistics"). As a result, this tool checks sets of random logical addresses of bitflips and finds those that belong to the same multiple events. LELAPE has been used in this Ph.D. thesis to analyze the experimental data issued from radiation-ground tests on memories.

4.4.2 Estimating the number of "false" multiple events by accumulation of simpler ones

In radiation tests on SRAMs or FPGAs, if two or more independent bitflips occurred in a memory accidentally happen in adjacent cells, they can be misled with multiple events. As the number of bitflips increases, it also raises the probability of two independent SBUs close to each other, incorrectly categorized as multiple events. Tausch, in 2009 [Tau09], used the "birthday statistics" model to make a simple formula presenting the probability of false pairs of SBUs with 2-bit MCUs and demonstrated the assumptions with results on apparent MBUs in an irradiated FPGA. Since its publication, this model has been widely used by many authors to refine the precision of experimental multiple-event cross-sections [Ton+17; Wir+14; She+10;

Table 4.4: *List of parameters of the memory and radiation-ground experiment that was carried out*

Parameter	Meaning	Note
L_N	Memory size in bits	
N	Number of bits to codify L_N	$2^{N-1} < L_\mathrm{N} \leq 2^N$
W	Word width in bits	
L_A	Number of word addresses	$L_\mathrm{A} = L_\mathrm{N}/W$
N_SB	Number of SBUs	
N_BF	Number of total bitflips	

SLF10; SLJ12; Mal+17].

Based on this idea, the GHADIR research team presented an improved version of the formula proposed by Tausch [Tau09] to estimate the number of false 2-bit MBUs, and additional equations to estimate the number of false 2-bit and 3-bit MCUs [Fra+20; Fra+19], existing in a dataset issued from a radiation-ground experiment. Thus, the expected number of such false multiple events can be specified by providing the parameters from the memory and the experiment that was carried out, as shown in Table 4.4. Also, this technique is accurate for irradiation campaigns on SRAM-based FPGAs. These equations were used in this Ph.D. thesis to refine the results and are explained below.

False 2 and 3-bit MBUs

According to [Fra+19], the expected number of false 2 and 3-bit MBUs occurred by accumulation of SBUs can be estimated by using Eqs. 4.1 and 4.2:

$$N_{\mathrm{F_2bit_MBU}} = \frac{1}{2} \cdot \frac{W-1}{W} \cdot \frac{N_{BF} \cdot (N_{BF}-1)}{L_\mathrm{A}} \cdot \left(1 - \frac{N_{BF}-2}{L_\mathrm{A}}\right) \tag{4.1}$$

$$N_{\mathrm{F_3bit_MBU}} = \frac{1}{6} \cdot \frac{(W-1)\cdot(W-2)}{W^2} \cdot \frac{N_{BF} \cdot (N_{BF}-1) \cdot (N_{BF}-2)}{L_\mathrm{A}^2} \cdot \left(1 - \frac{N_{BF}-3}{L_\mathrm{A}}\right) \tag{4.2}$$

False 2-bit MCUs

According to [Fra+20], the expected number of false 2-bit MCUs occurred by accumulation of SBUs can be estimated by using Eq. 4.3:

$$N_{\mathrm{F_2bit_MCU}} = \frac{1}{L_\mathrm{X}} \cdot N_P \cdot S_1 \tag{4.3}$$

where:

$$S_1 = 2 \cdot D \cdot (D+1) \tag{4.4}$$

$$N_{\mathrm{P}} = \binom{N_{\mathrm{BF}}}{2} = \frac{1}{2} \cdot N_{\mathrm{BF}} \cdot (N_{\mathrm{BF}} - 1) \tag{4.5}$$

D is the threshold "Manhattan Distance" value used to categorize 2 events as belonging to the same multiple events. S_1 is the number of bitcells around a given flipped bitcell c_1 for which, if another cell, c_2, is also flipped, both c_1 and c_2 will be considered as part of the same MCU, if MD is used as criteria to group SBUs into the same multiple event [Fra+20]. In this reference, this is referred to as the "cell influence area" of c_1. L_{X} can be L_{N} or L_{A}, depending on cell or word addresses to determine the abnormal values.

False 3-bit MCUs

According to [Fra+20], the expected number of false 3-bit MCUs occurred by accumulation of SBUs can be estimated by using Eq. 4.6:

$$N_{\mathrm{F_3bit_MCU}} = N_{\mathrm{T}} \cdot \frac{1}{L_X^2} \cdot S_1 \cdot (S_1 - 1) \cdot M \tag{4.6}$$

where S1 was defined above and N_{T} is:

$$N_{\mathrm{T}} = \binom{N_{\mathrm{SB}}}{3} = \frac{1}{6} \cdot N_{\mathrm{SB}} \cdot (N_{\mathrm{SB}} - 1) \cdot (N_{\mathrm{SB}} - 2) \tag{4.7}$$

M can range from 1 to 3 according to the influence area of three flipped cells. If the influence areas of those cells overlap, the possible combinations decrease. In the optimistic mode, M=1, the smallest influence area occurs, and the largest for the pessimistic happens in M=3. It should be mentioned that in this thesis, all results were analyzed by considering M=1. For instance, Figure 4.11 displays an example of the influence areas of three flipped cells when D=2.

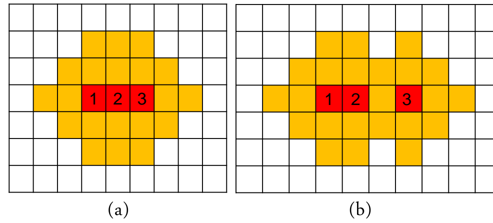

Figure 4.11: *Dependence of the influence area of three flipped cells. In this example, D=2. In (a), flipped bits are adjacent, covering a total surface of 20 cells. In (b), it is assumed an SBU with a close 2-bit MCU happened that covers 23 cells. Red cells show the flipped cells, and orange cells are the influence areas.*

Chapter 5

Test results and discoveries

This chapter presents the test results and the discoveries made throughout this Ph.D. thesis on devices, as reported in Table 4.1 and at the facilities briefed in Table 4.2 with different particles. Most of these points have been discussed in the publications issued from this Ph.D. thesis [Fra+20; Fab+20; Kor+20; Kor+22; Fab+21; Fab+22]. The significant parameters for analyzing the results include particle type (neutrons or protons) and energy, flux, the incidence angle of particles against the surface and the DUT, and test type (static or dynamic).

5.1 Infineon nv-SRAM (CY14V101QS): Experimental results and discussion

This section provides the SEE susceptibility of the nv-SRAM (CY14V101QS) of Table 4.1 with the campaigns presented in Table 4.2.

5.1.1 CY14V101QS: Experimental results under 14.2-MeV neutrons

Static tests were carried out on this memory. It was irradiated with two different incident angles (normal and grazing), and two directions were tested for each. These are depicted in Figure 5.1: horizontal (H) and vertical (V) for grazing angles; and the front and back of the memory for normal incidence.

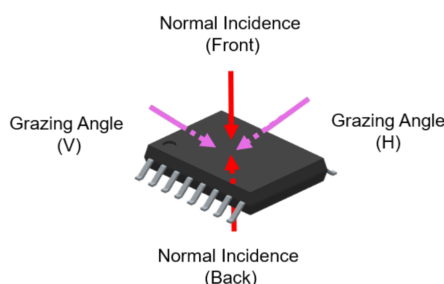

Figure 5.1: *Beam incident angles that were tested for the CY14V101QS memory.*

Table 5.1 shows the rounds of irradiation that were carried out, grouped into 16 different types of experiments (4 patterns x 2 incident angles x 2 directions). Rounds from 1 to 10 minutes were made, at fluxes that ranged from 1.04×10^7 to 9.70×10^7 $n \cdot cm^{-2} \cdot s^{-1}$. Each round of reading had its particular flux, distance, and exposure time. For the grazing angles, the distance was calculated to the center of the chip. These were different because the extension board was not symmetric; hence these numbers were forced and not chosen. Roughly, it can be observed that the number of affected addresses is similar in all the rounds of irradiation that had similar fluence. They also seem to scale accordingly with said fluence.

Table 5.1: *Rounds of irradiation performed on static experiments carried out for the CY14V101QS memory under 14.2- MeV neutrons*

N^o	Angle	Distance test (cm)	Pattern	Fluence ($\times 10^{10}$) (n/cm^2)	Number of affected addresses
1	Normal incidence (Front)	1.9	0x55	2.34	902
2		1.9	0x55	2.34	914
3		1.9	0x55	4.65	1810
4		1.9	0xFF	2.33	938
5		1.9	0xFF	2.34	899
6		1.9	0x00	2.32	904
7		1.9	0x00	2.32	860
8		1.9	0xAA	2.33	949
9		1.9	0xAA	2.32	955
10	Grazing angle (H)	2.6	0x55	1.24	588
11		2.6	0xFF	1.24	649
12		2.6	0xAA	1.23	574
13		2.6	0x00	1.25	626
14	Grazing angle (V)	3.2	0x55	0.818	338
15		3.2	0xFF	0.818	378
16		3.2	0xAA	0.818	335
17		3.2	0x00	0.826	339
18	Normal incidence (Back)	5.2	0x55	0.62	177
19		5.2	0x55	0.78	221
20		5.2	0xAA	0.776	226
21		5.2	0xFF	0.777	239
22		5.2	0x00	0.778	241

It should be mentioned that the errors discussed will correspond to the bulk CMOS layer of the nvSRAM. No errors were observed on the SONOS Quantum Trap layer (see Subsection 3.2.3 from Chapter 3 for more details) after receiving a total fluence of $3.53 \cdot 10^{11}$ n/cm^2.

CY14V101QS: SBUs and MCUs

As discussed in Subsection 4.4.1, SBUs and MCUs must be extracted from the set of detected SEUs to correctly analyze the SEU sensitivities depending on the multiplicity of the events. This was done by using unscrambling proprietary information provided by Infineon Technologies, which allowed translating the logical addresses into physical ones. This made it possible to find the physical XY cell placement of the errors in the SRAM. Once the placement was found, the MD technique [Cra17] was used; in this case, the D value was 2. In addition, according to Table 5.1, in some rounds of reading, the number of recorded bitflips was high; hence the probability of multiple events being the result of 2 simple ones was not negligible. For this reason, the equations presented by the authors in [Fra+20] and discussed in Subsection 4.4.2 were used to correct the numbers of MCUs that were primarily found.

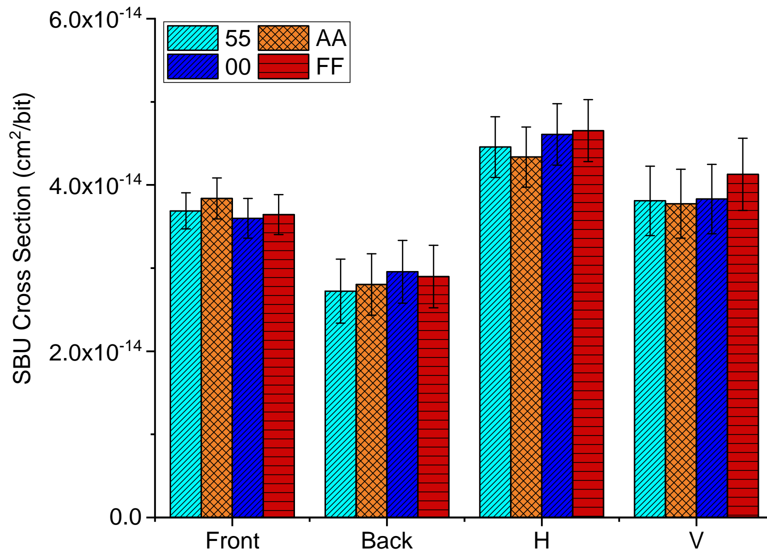

Figure 5.2: *Experimental SBU cross-sections obtained at different incident angles and patterns for the CY14V101QS memory under 14.2- MeV neutrons.*

Figure 5.2 displays the SBU cross-sections for different patterns and angles, the error margins of which have been calculated with 95% confidence, as explained in [Aut+14; Vel+14]. It is observed that the SBU sensitivity increases at grazing angles and that the H direction showed to be more prone against SBUs for all the patterns. It is also remarkable that, for a normal incidence, the irradiation from the back yielded fewer errors (therefore, a lower sensitivity) than from the front. The physical mechanisms leading to this phenomenon will be deeply discussed in Section 5.1.5.

Next, Figure 5.3 shows the experimental 2-bit MCU cross-sections. In this case, fewer events were observed. This figure shows a similar trend to Figure 5.2. On the one hand, the higher error rates observed at grazing angles (H and V) are consistent with the experimental results

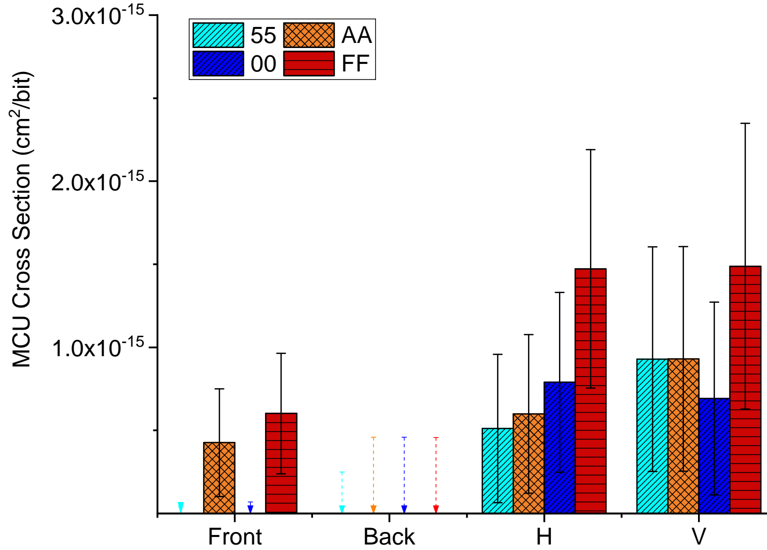

Figure 5.3: *Experimental 2-bit MCU cross-sections obtained at different incident angles and patterns for the CY14V101QS memory under 14.2-MeV neutrons. Arrows indicate the uppermost possible values for cross-section in this memory if no events were observed.*

presented by Harada *et al.* [Har+12], Hirokawa *et al.* [Hir+15], and Kato *et al.* [Kat+19]; it is also pointed out that the sensitivity for 2-bit MCUs for 14.2-MeV neutrons increases at grazing angles. On the other hand, again, in this figure, it is observed that the number of events increases when irradiating from the front of the SRAM compared to receiving the radiation from the back. It should be mentioned that very few MCUs were observed at normal incidence (Front & Back). However, these abundances were considerably higher for grazing ones (H & V).

Finally, the null abundance of MCUs in the "Back" experiment was surprising. In fact, the ratios between "SBU Front"/"MCU Front" and "SBU Back"/"MCU Back" are very different since "MCU back" is much lower than expected. The large confidence margins make it difficult to reach further conclusions, particularly regarding the dependence on the pattern (constant or *checkerboard*).

CY14V101QS: MBUs

Due to a large number of detected bitflips and the relatively small size of the memory (only 1 Mb), the chance of observing pairs of nearby but independent SBUs and confusing them with multiple events is not negligible. Since the DUT implemented bit interleaving, MBUs are theoretically impossible to happen in this memory. However, several 2-bit MBUs were observed during the experiments, presumably due to the accumulation of 2 SBUs in the same word. Thus, the expected number of false 2-bit MBUs was calculated by Eq. 4.1.

Figure 5.4 demonstrates the number of experimental 2-bit MBUs (dots and confidence margins) in comparison with the predictions issued by Eq. 4.1 (dashed line). Dots refer to the

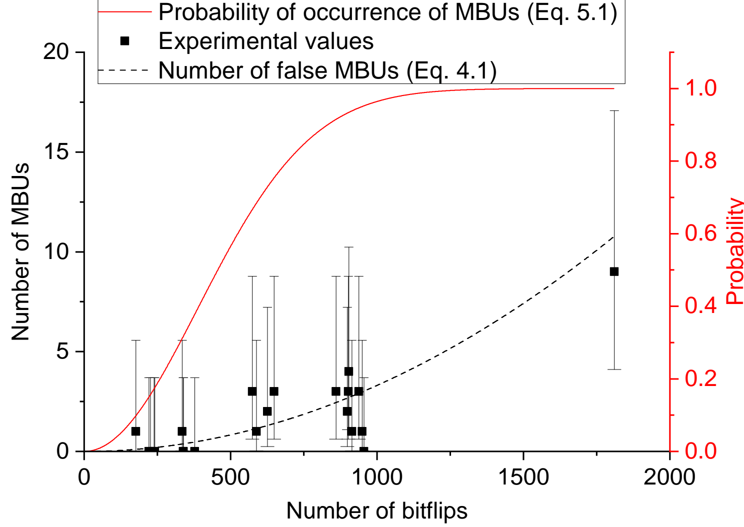

Figure 5.4: *Experimental and estimated number of 2-bit MBUs (dots and (4.1) - dashed line). The continuous line indicates the probability of occurrence of 2-bit MBUs according to (5.1).*

different rounds that were made (Table 5.1). The prediction reasonably matches all the observed experimental occurrences, concluding that the experimental MBUs were, indeed, false ones. The figure also includes the probability of occurrence of such multiple events in the continuous line, which tends to 1 as the number of bitflips increases. This probability was taken from (17) in [Tau09] and it can be modeled as follows:

$$\text{PROB}_k(L_N, N_{BF})_{\text{2bit_MBU}} \approx 1 - exp(-\frac{N_{BF} \cdot (N_{BF} - 1) \cdot (2k - 1)}{2L_N}) \tag{5.1}$$

where k is a value postulated by the researcher to be set to $\frac{W}{2}$. The other parameters were described in Table 4.4. It should be noted that both lines (continuous and dashed) refer to different vertical scales (right and left, respectively).

5.1.2 CY14V101QS: Experimental results under 15.3-MeV protons

This section presents test results on CY14V101QS under 15.3-MeV protons, as shown in Table 5.2. The volatile part of the memory was radiated in rounds from 1 to 6 minutes, and static tests were conducted on the non-volatile part ranging from 5 to 15 minutes. The DUT was tested with different patterns, including 0x00, 0xFF, 0x55, and 0xAA. Also, dynamic tests were made, under algorithms March DS and C, with fluences of 5.50 and 3.20 $\times 10^{11}$ p/cm^2, respectively.

Figure 5.5 indicates the SBU cross-sections for different patterns, showing that errors are in the same order of magnitude. The highest cross-section is observed at pattern 0xAA; however, no dependence was observed in different patterns.

Table 5.2: *Rounds of irradiation carried out for the CY14V101QS memory under 15.3-MeV protons*

Nº	Test type	Pattern	Fluence ($\times 10^{11}$) (p/cm^2)	Number of bitflips
1	Static	0x55	0.80	105 (V part)
2		0xFF	0.78	101 (V part)
3		0x00	0.93	132 (V part)
4		0xAA	1.00	166 (V part)
5		0x55	0.80	0 (NV part)
6		0x55	3.70	0 (NV part)
7		0xAA	62.00	0 (NV part)
8	Dynamic	March DS	5.50	771
9		March C	3.20	431

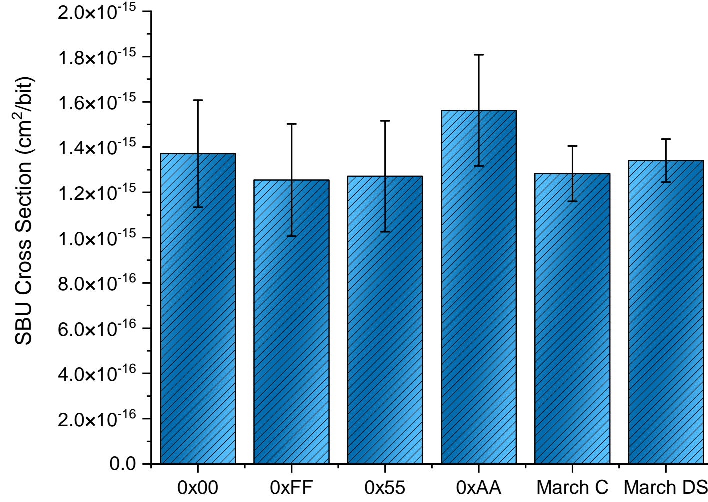

Figure 5.5: *Experimental SBU cross-sections of the CY14V101QS memory under 15.3-MeV protons.*

According to the manufacturer, the NV-part of the CY14V101QS memory is immune to errors. This was experimentally verified in Rounds 5 to 7 in Table 5.2; since no SEE was found in a total fluence of 66.5×10^{11} p/cm^2.

Regarding dynamic test results, the SBU sensitivity of the memory is in the same order of magnitude as in the static ones (Figure 5.5).

Among static tests, only one MCU was observed at pattern 0xAA; the other detected ones were false in static and dynamic experiments. Besides, no MBUs were observed, except 7 MBUs in March DS; regarding Eq. 4.1, the number of false ones was 1.96.

5.1.3 CY14V101QS: Experimental results under thermal neutrons

Static and dynamic tests were made under 25-meV thermal neutrons (Table 5.3). It was radiated in rounds from 1 to 5 minutes for each pattern with a total fluence of 46.08×10^{11} n/cm^2.

The device received 12.20 and 15.40 n/cm^2 fluences in March C and March DS, respectively. Approximately, the number of affected addresses was similar in all the rounds of irradiation that had similar fluence.

Table 5.3: *Rounds of irradiation carried out for the CY14V101QS memory (volatile part) under thermal neutrons*

N^o	Test type	Pattern	Fluence ($\times10^{11}$) (n/cm^2)	Number of bitflips
1	Static	0x55	1.44	176
2		0x55	2.88	378
3		0x55	7.20	876
4		0xAA	1.44	189
5		0xAA	2.88	351
6		0xAA	7.20	949
7		0x00	1.44	180
8		0x00	2.88	340
9		0x00	7.20	879
10		0xFF	1.44	176
11		0xFF	2.88	374
12		0xFF	7.20	1285
13	Dynamic	March C	12.20	1405
14		March DS	15.40	1870

The highest SBU cross-sections were observed with pattern 0xFF, as shown in Figure 5.6. The sensitivity was the lowest when the irradiation on the memory was performed using the pattern 0x00. All detected MCUs were false ones, so no MCU is reported among these tests. Two dynamic experiments were applied to the memory. Figure 5.6 shows that the highest sensitivity was observed in March DS. The same as static ones, no MCUs were observed again in dynamic tests.

Finally, 16 2-bit MBUs in the CY14V101QS under thermal neutrons were observed, which, according to Eq. 4.1, were false ones.

5.1.4 CY14V101QS: Comparison of taken results under 14.2-MeV neutrons, 15.3-MeV protons, and 25-meV thermal neutrons

This section compares all the static experiments that were made on the CY14V101QS. Figure 5.7 illustrates the devices' SBU cross-sections, obtained during static tests, as a function of the data pattern. A difference of one order of magnitude was found between 14.2-MeV neutrons and other particles' SBU cross-sections (protons and thermal neutrons). The response of the

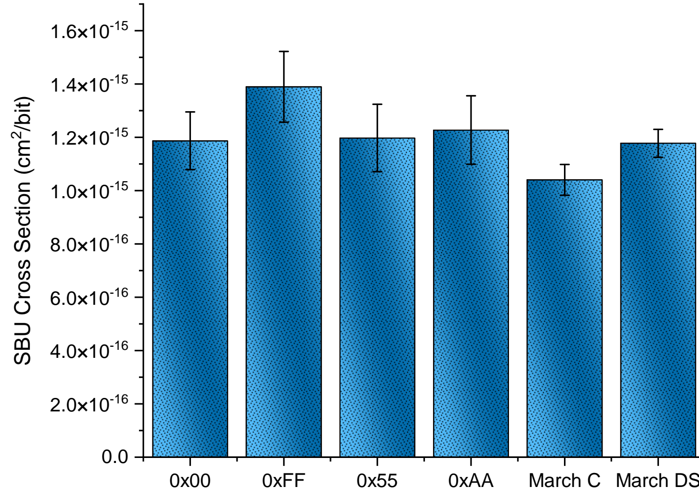

Figure 5.6: *Experimental SBU cross-sections of the CY14V101QS memory under thermal neutrons.*

device to thermal neutron and proton irradiations share similar characteristics.

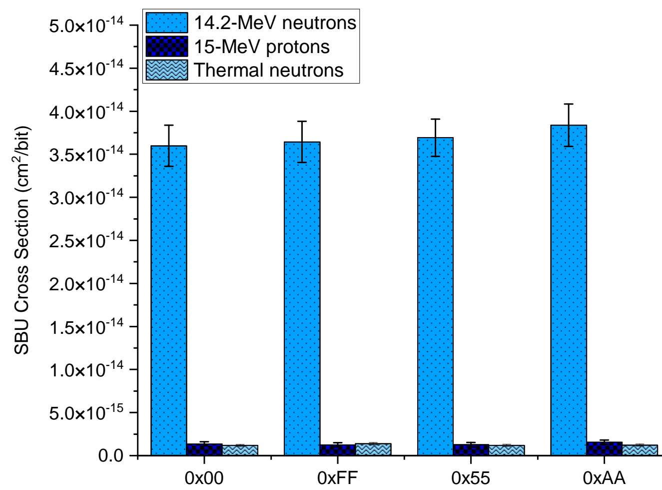

Figure 5.7: *Comparison of static SBU cross-sections of the CY14V101QS memory under 14.2-MeV and thermal neutrons, and protons.*

Several reasons can demonstrate why proton and neutron cross-sections have almost one order of magnitude in difference with similar energies. An investigation in [HG17] showed that at 30 MeV and above, the SEU cross section of protons is supposed to equal the neutrons' one. However, the cross-section for protons is lower than for neutrons of lower energies (below 30 MeV). The reasons are explained below:

1. There is a higher cross-section for inelastic neutron reactions in silicon than for proton ones.

2. More energy is deposited in inelastic neutron events than in proton ones.
3. There is a lower energy threshold in neutron SEUs than in the proton ones.
4. Due to a bump in the neutron SEU cross-section at 14 MeV, the equivalent LET dramatically rises for neutrons with energy close to 14 MeV.

Also, authors in [Rez+20] performed simulations using GEANT4 to investigate the reason for the difference in the proton and neutron cross-sections. They showed that, in a practical view, the difference in cross-sections could be assigned to nuclear reaction properties and the scattering/albedo neutrons caused by polyethylene shielding and concrete chamber walls.

5.1.5 CY14V101QS: Discussion of experimental results

CY14V101QS: SEU Sensitivity Assessment under 14.2-MeV Neutrons with MUSCA-SEP3

MUSCA-SEP3 is a Monte Carlo prediction tool that works with databases. This tool has been developed by researchers of the "Office National d'Études et de Recherches Aérospatiales" (ONERA), with whom there has been a collaboration to carry out this Ph.D. thesis. It simulates the radiation effects of different kinds of particles (protons, neutrons, heavy ions) on memories implemented with diverse semiconductor manufacturing technologies (bulk CMOS, SOI, Fin-FET, etc.), taking into account the miniaturization of the technological node [Hub+09a; Hub+13; GA15]. This tool has as input an XY floorplan of memory cells without taking into account any other on-chip architectural module, such as I/O buffers, row/column decoders, sense amplifiers, and so on. It provides a complete simulation environment that models the interaction of the radioactive particles with the matter, which allows performing estimations of the SEU sensitivity from the overall system down to the semiconductor level. MUSCA-SEP3 receives as inputs a device description, the semiconductor active zones, and the critical charge of the bit cells without the need for any particular experimental data [Hub+09a].

For the case of modeling an SRAM with MUSCA-SEP3, the elementary cell is firstly described, so the rules of translation are applied to all the memory. For modeling the elementary cell, several volumes represent physically sensitive drains, i.e., their sizes and positions. To illustrate the methodology of modeling, the studied SRAM (planar bulk technology), the active zones (drains and sources), and the Shallow-Trench Isolation (STI) topology were designated. This technique uses a General Design Specification (GDS) extractor to get these details from GDSII files. Reverse engineering leads to a detailed knowledge of elementary cell topology. Furthermore, this reverse analysis obtains the crucial physical parameters of the device, such

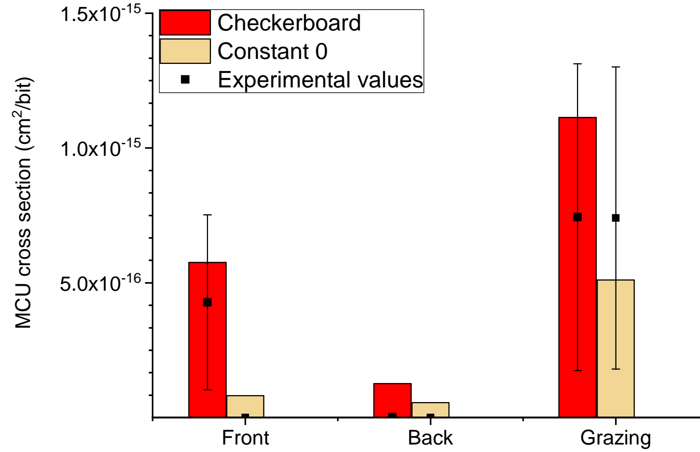

Figure 5.8: *Comparison of 2-bit MCU cross-sections (14.2-MeV neutrons) issued from MUSCA-SEP3 vs. experimental results of the CY14V101QS memory for different incidence angles and patterns.*

as NMOS and PMOS drains implantation and the metallization and the passivation layers [Art+11].

Simulations issued from this tool were compared with the experimental ones obtained under 14.2-MeV neutrons. Figure 5.8 shows such a comparison for 2-bit MCUs. Since the experimental results were not conclusive about the correlation between the pattern and the device SEU sensitivity, the figure only displays averaged results regarding both *checkerboard* and the "Constant 0" patterns ("Constant 1" is not shown for simplicity). Columns display predictions, whereas dots do likewise with experimental results (with 95% confidence margins). Two conclusions can be drawn:

- Predictions show a good concordance with the experimental results, including a lower sensitivity in neutron tests made from the back of the device.
- Predictions depict a slight dependence on the pattern (the sensitivity seems lower for the "Constant 0" pattern). As discussed above, this point could not be confirmed by looking at the experimental results.

CY14V101QS: MUSCA-SEP3 Analytical Study of Angular Effects

This subsection aims at further understanding the nuclear mechanisms leading to the difference between SBU and MCU cross-sections observed experimentally and in MUSCA-SEP3 simulations regarding the different angles of incidence tested in the experiments.

For 14.2-MeV neutrons, the impact in semiconductor devices is predominantly caused by nuclear neutron scattering processes. Recoil atoms, commonly referred to as "primary knock-on atoms" (PKAs), are produced through neutron-nucleus interactions, and they traverse the device

materials, including passivation, metallization, and the active semiconductor. Secondary ions are characterized by their atomic numbers, mass numbers, energies, and directions.

From the strict point of view of nuclear interaction, back-side or front-side irradiations imply the same secondary ion productions with very similar characteristics. These, in turn, create electron-hole pairs in the active silicon that participate in the transport and charge collection mechanisms. However, the device's metallization and passivation layers are asymmetrically distributed concerning the active silicon substrate (i.e., they exist on the front side but not on the back side). In contrast, the active silicon is symmetrically distributed to itself. Thus, angular properties may be suspected of having a significant impact on the SEU occurrence, in particular, for 14.2-MeV neutrons.

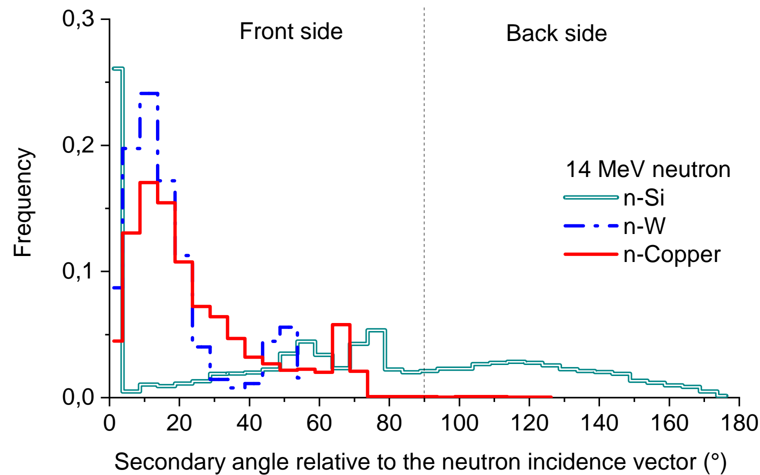

Figure 5.9: *Emission angle frequency of secondary ions induced by a 14.2-MeV neutron interaction with Silicon, Tungsten and Copper ion nuclei. The incidence (or direction) vector of neutrons in this simulation is normal with respect to the device's surface.*

To get a deeper insight into this, the characteristics of secondary particles, including elastic and non-elastic reactions in Silicon (Si), Tungsten (W), and Copper (Cu), have been investigated using GEANT4 simulations [Esp+04]. In silicon, secondary ions can range from H to P with several isotopes. This research considered the order of 10^4 interactions for these three species. Simulations provide the secondary ions count, atomic and mass numbers, energies, and directions. Figure 5.9 presents the emission angle frequency for the three species, which is measured with respect to the neutron direction vector (featuring normal incidence for the device's surface). The figure only shows the abundance of secondary ions whose energy is high enough to participate in the SEE generation process (a minimum threshold value of 0.1 MeV was considered for this purpose). Angle values ranging 0° to 90° correspond to secondary ions emitted in the direction of the incident vector. In contrast, angles greater than 90° imply secondary ions emitted in the opposite direction. Results presented in the figure show that, for 14.2-MeV neutron interactions, secondary ions are mainly emitted in the direction of the neutron incident vector. This is

especially true for n-W and n-Cu interactions, which reinforces the idea that the secondary ions emitted by these reactions explain the differences between SEE sensitivities in front neutron incidence vs. back.

Therefore, the front-side irradiation is characterized by the contribution to the SEU cross-sections of secondary ions produced in the active silicon and the passivation/metallization layers. However, in the case of the back-side irradiation, secondary ions produced in the passivation/metallization layers participate sparsely in the generation of electron-hole pairs in the active silicon. In fact, only 0.48% and 33.5% of secondaries are emitted backward from n-Cu and n-Si reactions, respectively. This explains the significant difference observed (both experimentally and through simulations) between the SEU sensitivities of both kinds of tests.

In the case of lateral irradiation, the interpretation is more complex. When a neutron traverses the active zones of the device from the front or the back, the effective thickness that participates in the SEU occurrence via the nuclear processes is in the order of 10 to 20 μm. However, in the case of lateral incidence, the sensitive areas correspond to the whole SRAM array.

In Figure 5.9, an analysis of secondary ions induced by 14.2-MeV neutron interactions showed that they are mainly emitted in the direction of the neutron incidence angle. In the case of front/back incidence, the occurrence of MCUs is due to the proximity of the carrier deposition on adjacent cells and/or the carrier diffusion mechanism. However, in the case of lateral incidence, the path of the particle may impact a larger number of cells, which strongly depends on the coupled secondary ion range and carrier density. Thus, Figure 5.10 presents the distribution of the secondary ion range for which the LET value is greater than $0.1\text{MeV}\cdot\text{cm}^2/\text{mg}$ (i.e. $\sim 1\text{fC}/\mu\text{m}$ corresponding to the order of magnitude of the upset threshold). Results are presented for heavy ions ($Z > 11$) and alpha particles. Concerning the latter, range values are on the order of a few tens of micrometers (note the logarithmic scale), which confirms that the particle's track can match, or be very similar to, the thickness of the plane of the SRAM array. Apparently, this is only possible in the case of a lateral incidence. For heavy secondary ions, the range value can be greater than 1 μm, with a significant carrier generation in several adjacent cells. In any case, this figure shows that the lateral incidence is more favorable to the occurrence of multiple events.

CY14V101QS: Assessment of SEU Sensitivity in Environments with Isotropic Particles

This subsection investigates the influence of angular properties on the SEU sensitivity. The previous subsection has shown that the MCU cross-sections issued by MUSCA-SEP3 are accurate compared to the experimental ones, considering the front, back, and lateral incidence. Thus,

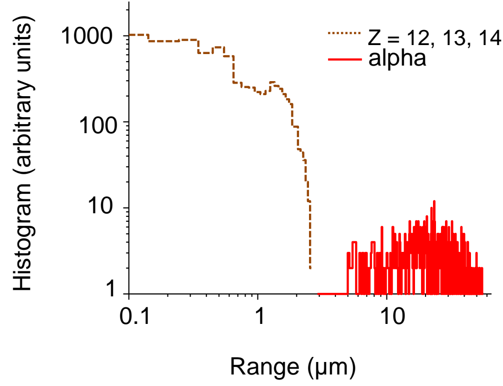

Figure 5.10: *Distribution of secondary ion range (Z > 11) and alpha particles, for which the LET value is greater than* $0.1\ \mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$.

simulations can be applied for other incidences, using a spherical description based on the θ and ϕ angles, as depicted in the spherical coordinate system of Figure 5.11(a). Vector $\overrightarrow{\rho}$ defines the direction and sense of incidence of the radiation beam, whereas θ is the angle concerning the Z axis, and ϕ is the angle of the projection of $\overrightarrow{\rho}$ on the HV plane concerning the H axis. Note that the H and V axes are consistent with the simplified description of the directions given in Figure 5.1. Figure 5.11(b) depicts the position of the passivation/metallization layers over the sensitive volume of silicon. It should be said that $\theta = 0$ makes $\overrightarrow{\rho}$ point to the back of the board, and $\theta = \pi$ corresponds to the front of the board.

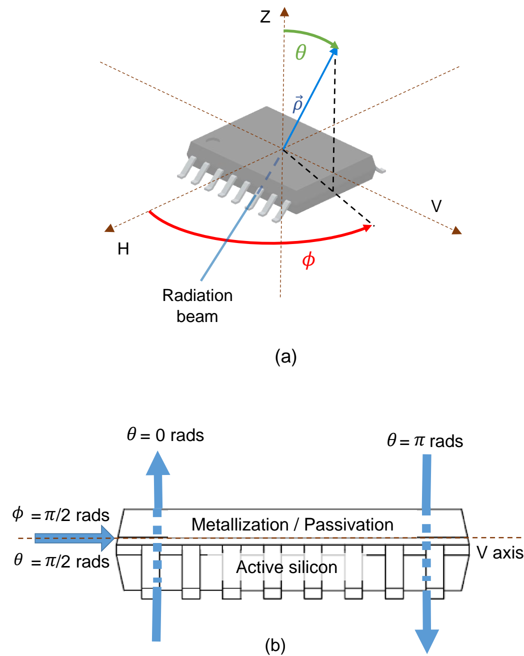

Figure 5.11: *a) Spherical coordinate system and b) passivation / metallization layers.* θ *and* ϕ *are the tilt angles of the incident particles with respect to the Z and H axis, respectively.*

Table 5.4 and Figure 5.12 present the MCU cross-sections for 14.2-MeV neutrons for a

130-nm bulk CMOS technology as a function of θ and ϕ, with an angular resolution of $\pi/4$ and $\pi/8$, respectively by means of MUSCA-SEP3. For simplicity, θ ranges from 0 to π and ϕ ranges from 0 to $\pi/2$. Therefore, only a quarter of the possible angles of θ and ϕ have been simulated, corresponding to the sector facing the reader in Figure 5.11(a). In this case, it is interesting to note that the worst configuration was obtained for $\theta = \pi/2$ and $\phi = \pi/4$, i.e., an oblique grazing direction (see Figure 5.12 in between H and V) that maximizes the SEE sensitivity (both off-state transistors simultaneously impacted by the charge deposition). In fact, this maximum value (62.3×10^{-17}cm^2/bit) and the minimum one (5.61×10^{-17}cm^2/bit) differ by one order of magnitude.

Table 5.4: *2-bit MCU cross-sections (cm^2/bit), obtained with MUSCA-SEP3, as a function of θ and ϕ (see Figure 5.11(b), with an angular resolution of $\frac{\pi}{4}$ and $\frac{\pi}{8}$, respectively. In light-gray cells, the front, back and grazing incidences discussed in Subsection 5.1.1. The dark-gray cell is the highest value*

		ϕ (rads)				
		0	$\frac{\pi}{8}$	$\frac{\pi}{4}$	$\frac{3\cdot\pi}{8}$	$\frac{\pi}{2}$
θ (rads)	0	5.61	5.61	5.61	5.61	5.61
	$\frac{\pi}{4}$	7.20	7.93	9.83	8.36	7.90
	$\frac{\pi}{2}$	38.30	45.70	62.30	56.80	51.10
	$\frac{3\cdot\pi}{4}$	10.50	11.50	14.30	12.20	11.50
	π	8.16	8.16	8.16	8.16	8.16
		$\times10^{-17}$cm^2/bit				

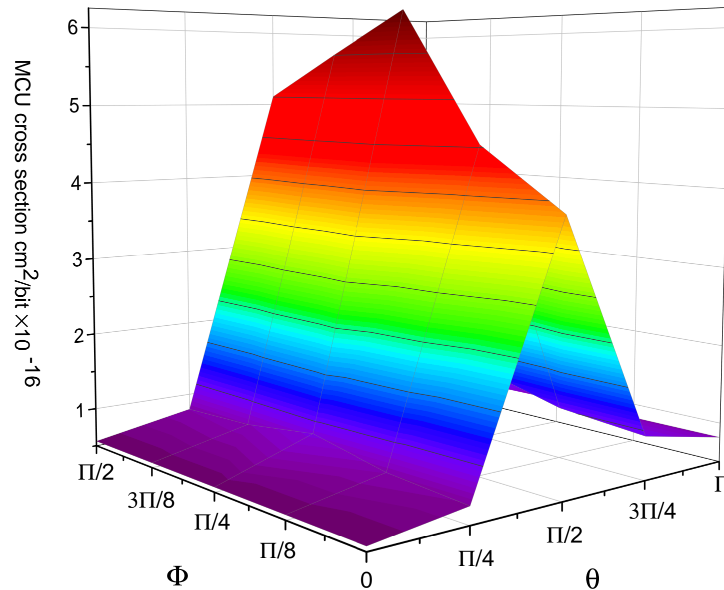

Figure 5.12: *2-bit MCU cross-sections (cm^2/bit), obtained with MUSCA-SEP3, of the tested technology of the CY14V101QS (130-nm bulk CMOS), as a function of θ and ϕ angles of incidence. Graphical representation of the data of Table 5.4.*

It also has to be noted that the grazing incidences discussed in the previous section are amongst the highest sensitivities simulated in this study, albeit none of them is the absolute

highest one. They correspond to the cells ($\theta = \pi/2$, $\phi = 0$) and ($\theta = \pi/2$, $\phi = \pi/2$). These and the front and back incidences have been highlighted in light-gray color in the table for clarity. Also, note that when keeping θ constant to $\pi/2$ (grazing direction always parallel to the HV plane), changing ϕ leads to an asymmetrical variation of the MCU sensitivity, which is higher towards the V direction ($\theta = \phi = \pi/2$).

Thus, for instance, for 2-bit MCUs, the device sensitivity can be calculated considering two hypotheses:

- Front normal incidence of the neutrons with an MCU cross-section of $5.61 \times 10^{-17}\text{cm}^2/\text{bit}$. This is a clear underestimation when considering the results of Table 5.4 and Figure 5.12.
- Isotropic incidence of the neutrons. This case implies integrating the product of neutron fluence and 2-bit MCU cross-section over the solid angle. In this case, considering that 1) these results can be extrapolated to the rest of the possible incident angles ($\theta = \{\pi \cdots 2\pi\}$ and $\phi = \{\pi/2 \cdots 2\pi\}$); 2) all the possible incident angles have the same probability, and 3) keeping the angular resolution of Table 5.4, the estimated sensitivity would be around $1.70{\times}10^{-16}\text{cm}^2/\text{bit}$, which more than doubles the one that would be considered in an anisotropic environment where only normal incidence is taken into account.

Of course, this approach is valid for other technologies (Fin-FET, SoI, etc.) and miniaturization nodes. Additionally, this study remains valid for non-interleaved architectures (such as old FPGAs), where part of the MCUs will be MBUs provoked by a single particle. These conclusions can be considered a first step toward analyzing other memories operating in harsh environments.

5.2 Infineon nv-SRAM (CY14B101J): Experimental results and discussion

This section discusses the SEE sensitivity of the second nv-SRAM (CY14B101J) of Table 4.1 with the campaigns carried out in Table 4.2.

5.2.1 CY14B101J: Experimental results under 15.3-MeV protons

The experiments (Table 5.5) were produced with an average proton energy of 15.3 MeV at fluxes that ranged from $3.10{\times}10^8$ to $7.30{\times}10^9$ p/s/cm^2. Static tests in voltages of 3.3V and 2.7V were carried out on the memory. Also, two dynamic methods were performed at a fluence of $6.50{\times}10^{11}$ and $7.20{\times}10^{11}$ p/cm^2.

Table 5.5: *Rounds of irradiation carried out for the CY14B101J memory under 15.3-MeV protons*

N^o	Test type	Pattern	Voltage (V)	Fluence ($\times 10^{11}$) (n/cm^2)	Number of bitflips
1	Static	0x55	3.3	0.83	225
2		0xFF	3.3	0.84	182
3		0x00	3.3	0.82	196
4		0xAA	3.3	0.83	210
5		0x55	2.7	0.84	217
6		0xFF	2.7	0.83	228
7		0x00	2.7	0.85	199
8		0xAA	2.7	0.83	219
9		0x55	3.3	87.00	1 (NV part)
10	Dynamic	March C	3.3	6.50	1634
11		March DS	3.3	7.20	2001

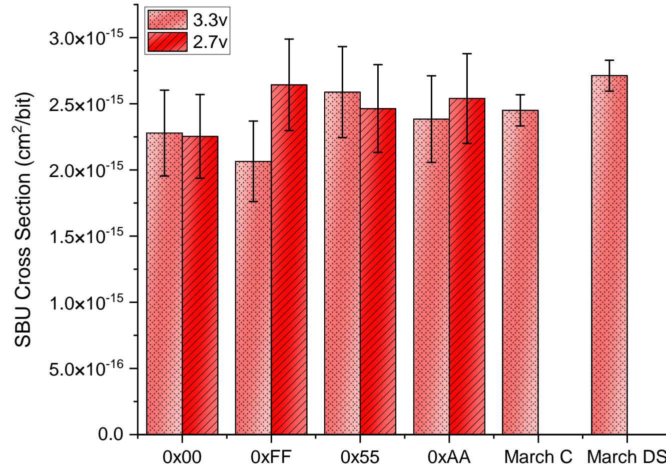

Figure 5.13: *Experimental SBU cross-sections of the CY14B101J memory under 15.3-MeV protons.*

Figure 5.13 shows the SBU cross-sections in static and dynamic modes for two bias voltages, 3.3V and 2.7V. As the figure shows, no remarkable difference was observed among different voltages and patterns for the static tests. Comparing the results of all static and dynamic tests, it appears that the cross-section value is higher for the March DS. One interesting result is observed when one bitflip was detected in the 65634th address in the SONOS Quantum Trap layer after receiving a total fluence of 87.00$\times 10^{11}$ p/cm^2.

2 and 3-bit MCUs were observed, but after applying Eqs. (4.3) and (4.6), it could be concluded that they were false ones. At last, 5 2-bit MBUs occurred in the CY14B101J under 15.3-MeV protons, which, according to Eq. 4.1 were false ones too.

5.2.2 CY14B101J: Experimental results under thermal neutrons

Static and dynamic experiments on CB14101J were conducted under 25-meV thermal neutrons at a fixed flux of 2.4×10^9 n/s/cm^2. The main characteristics of the tests are summarized in Table 5.6. The static experiments correspond to Rounds 1 to 8 in the table, which report fluences of 1.44×10^{11} and 2.88×10^{11} n/cm^2 (1 and 2 minutes, respectively) for each pattern.

Table 5.6: *Rounds of irradiation carried out for the CY14B101J memory (volatile part) under thermal neutrons*

N^o	Test type	Pattern	Fluence ($\times 10^{11}$) (n/cm^2)	Number of bitflips
1	Static	0x00	1.44	211
2		0x00	2.88	425
3		0xFF	1.44	201
4		0xFF	2.88	402
5		0x55	1.44	119
6		0x55	2.88	372
7		0xAA	1.44	202
8		0xAA	2.88	390
9	Dynamic	March C	28.80	3514
10		March DS	64.80	7863

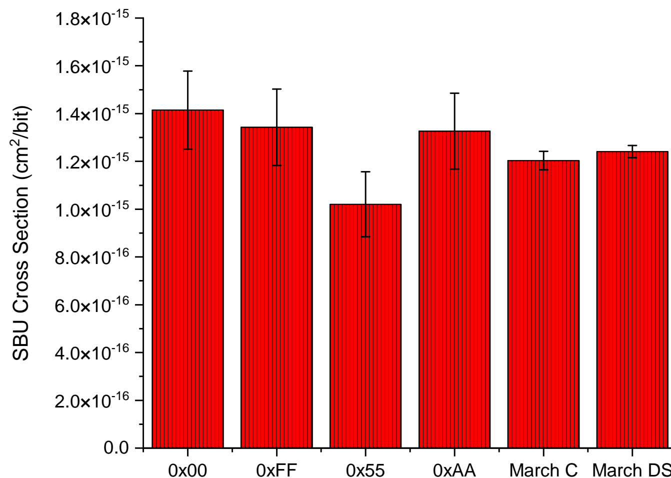

Figure 5.14: *Experimental SBU cross-sections of the CY14B101J memory under thermal neutrons.*

Figure 5.14 presents the devices's SBU cross-section during static and dynamic campaigns. The sensitivity was higher during the static tests at patterns 0x00, 0xFF, and 0xAA than in the dynamic modes. By increasing the beam time from 1 to 2 minutes, it can be seen that the number of bitflips gets doubled or even more. As the figure shows, the lowest cross-section belongs to pattern 0x55, although the difference is not significant. Both dynamic tests yielded almost the same sensitivity.

Concerning multiple events, no MCUs were recorded in all patterns at those fluence levels. 50 MBUs during static and dynamic modes were detected, which turned out to be false, after checking by using Eq. 4.1.

5.2.3 CY14B101J: Experimental results under 14.8-MeV neutrons

Three static campaigns and two dynamic tests were conducted at a fixed flux of 5.5×10^6 n $\cdot$ cm$^{-2}\cdot$ s^{-1} against 14.8-MeV neutrons, as provided in Table 5.7. The particle fluence ranged from 3.3×10^9 to 14.9×10^9 n/cm^2. Fast neutrons induced around a few hundred upsets for each test.

Table 5.7: *Rounds of irradiation carried out for the CY14B101J memory (volatile part) under 14.8-MeV neutrons*

N^o	Test type	Pattern	Fluence ($\times10^9$) (n/cm^2)	Number of bitflips
1	Static	0x55	3.30	237
2		0x55	4.95	348
3		0xAA	4.95	365
4		0x00	4.95	392
5		0xFF	4.95	383
6	Dynamic	March C	6.67	439
7		March DS	14.90	975

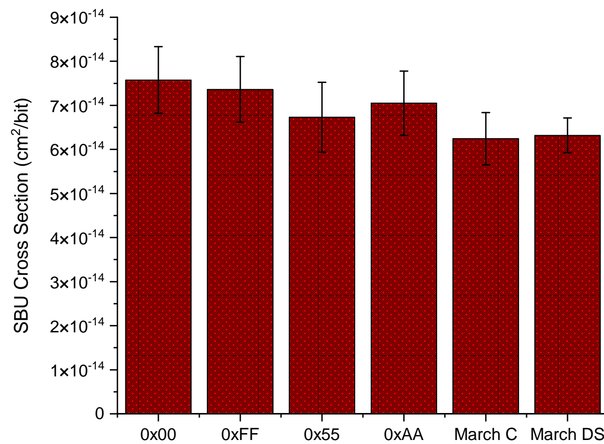

Figure 5.15: *Experimental SBU cross-sections of the CY14B101J memory under 14.8-MeV neutrons.*

The experimental static and dynamic SBU cross-sections of CY14B101J have been displayed in Figure 5.15. No dependence on the SBU cross-sections was detected in different patterns. Among all experiments, no MCUs or MBUs happened.

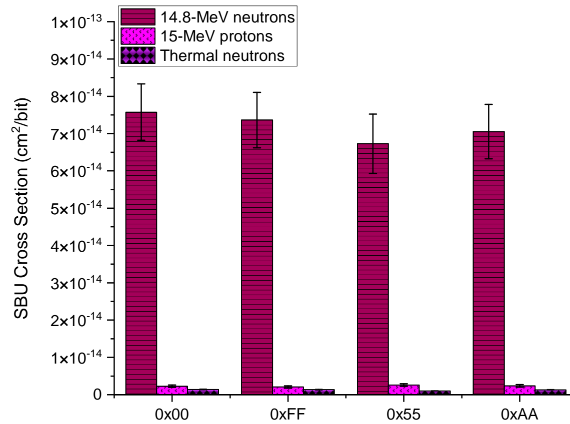

Figure 5.16: *All static experimental SBU cross-sections of the CY14B101J memory under 14.8-MeV and thermal neutrons and 15.3-MeV protons.*

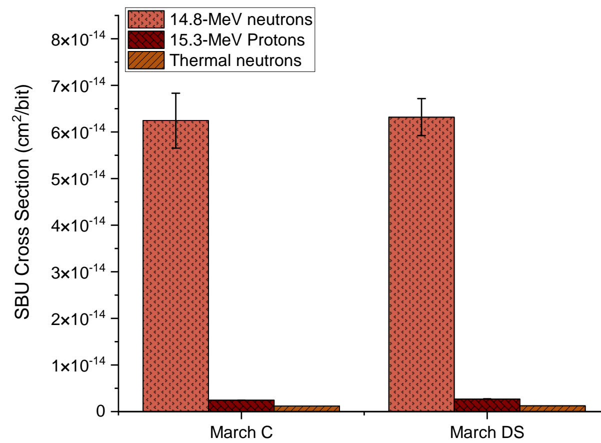

Figure 5.17: *All dynamic experimental SBU cross-sections of the CY14B101J memory under 14.8-MeV and thermal neutrons and 15.3-MeV protons.*

5.2.4 CY14B101J: Discussion of experimental results

The comparison of experimental static and dynamic SBU cross-sections of CY14B101J under proton, fast and thermal neutron irradiations are discussed in this section. The response of the device tested in static tests is compared in Figure 5.16. The sensitivity of the DUT was much higher during neutron irradiation with one order magnitude difference compared to thermal neutrons and protons. These results are similar to the events observed for the CY14V101QS as discussed in Subsection 5.1.5.

Regarding dynamic campaigns, similar to the static ones, the memory experienced the highest cross-section under 14.8-MeV neutrons; as it is about one order of magnitude higher compared to obtained ones against protons and thermal neutrons, as shown in Figure 5.17.

5.2.5 Comparison of taken results of the CY14V101QS and CY14B101J memories with each other

This section compares the results of both nv-SRAMs (CY14V101QS and CY14B101J) under protons, 14.2/ 14.8-MeV and thermal neutrons in static and dynamic modes. Figure 5.18 presents that in all static and dynamic rounds. The sensitivity of the CY14B101J is higher than that of the CY14V101QS; however, the SBU cross-section values are in the same order of magnitude. The same results are observed in Figure 5.19 against 14.2/ 14.8-MeV neutrons. However, when looking at Figure 5.20, one can observe that both memories exhibited the same SEE sensitivity under thermal neutrons. In any case, considering these 3 figures altogether, it can be noticed that the I^2C circuitry (i.e., the one used by the CY14B101J) is more susceptible to radiation effects than the SPI one (used by the CY14V101QS).

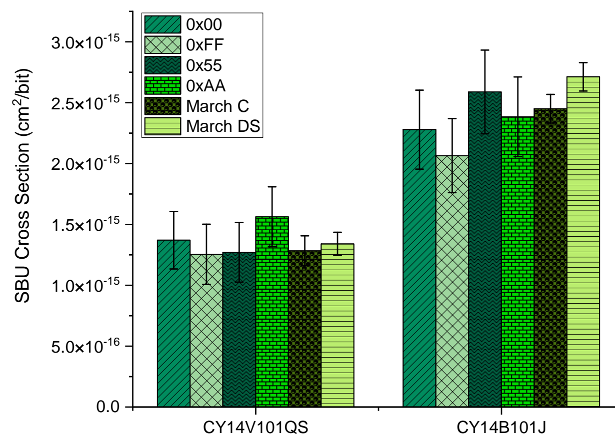

Figure 5.18: *Comparison of obtained results of CY14V101QS and CY14B101J under 15.3-MeV protons.*

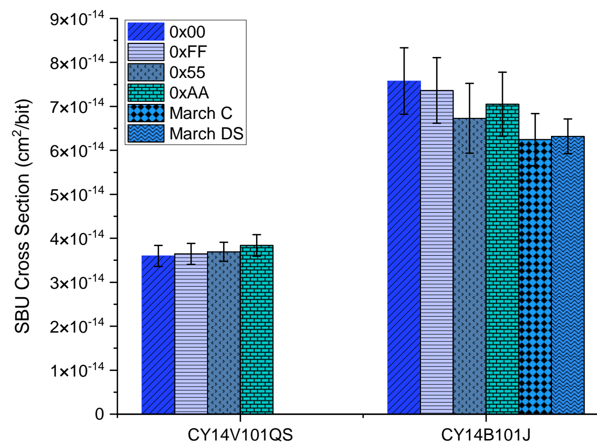

Figure 5.19: *Comparison of obtained results of the CY14V101QS and CY14B101J memories under 14.2/ 14.8-MeV neutrons.*

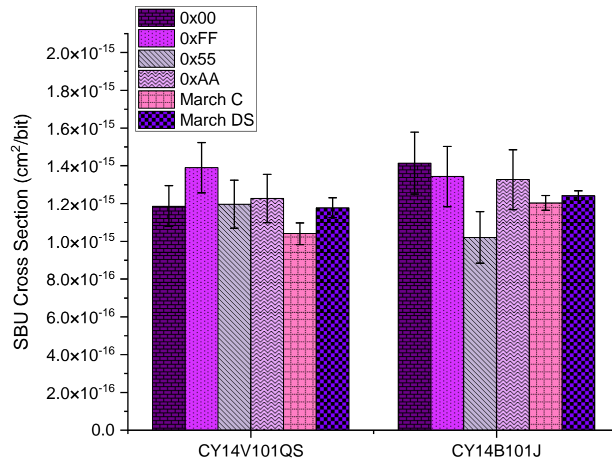

Figure 5.20: *Comparison of obtained results of the CY14V101QS and CY14B101J memories under thermal neutrons.*

5.3 Infineon FRAMs (CY15B102Q and CY15B104Q): Experimental results and discussion

This section discusses the SEE susceptibility of the FRAMs of Table 4.1 under 15.3-MeV and 1-MeV protons, thermal neutrons, and 14.8-MeV neutrons. Contrarily to the experiments presented in Sections 5.1 and 5.2, in this case, SEFIs and destructive SEEs were observed. These errors had in common that 1) either they affected an enormous amount of data addresses and the read contents were random when performing several consecutive readings, or 2) the regular operation of the memory was halted. If a reset in the power supply recovered the contents or operation of the memory, it was considered a SEFI; otherwise, the error was permanent and counted as a destructive SEE. Also, the setup platform did not have any system to monitor the current consumption of the memories under test, hence the type of destructive SEE (Single Event Burnout or SEB, Single Event Latchup or SEL, Single Event Gate Rupture or SEGR, as typically classified in the literature [Sex03]) could not be determined.

In other occasions, some events initially identified as SBUs or MCUs with little multiplicity (and with non-random erroneous contents) disappeared after performing a power cycle on the memory. These were considered as "unstable" events, following the terminology of Wei et al. [Wei+19], who also observed these events on COTS FRAMs under neutrons.

5.3.1 CY15B102Q and CY15B104Q: Experimental results under 15.3-MeV protons

12 rounds on the CY15B102Q FRAM were done. The results for each test are detailed in Table 5.8. Rounds from 5 to 20 minutes were carried out in static mode and one 31-minute round in dynamic mode, at fluxes ranging from 0.24×10^9 to 8.9×10^9 p/s/cm^2.

Table 5.8: *Rounds of irradiation carried out for the FRAMs (2-Mbit CY15B102Q and 4-Mbit CY15B104Q) under 15.3-MeV protons*

N^o	Sample	Test type	Pattern	Fluence ($\times 10^{11}$) (n/cm^2)	Observed event
1	FRAM (2-Mbit)	Static	`0x55`	0.85	×
2			`0x55`	7.50	2 unstable errors-in-row + 1 unstable SBU
3			`0xFF`	7.30	6 unstable SBUs + 3 SBUs
4			`0xAA`	7.40	4 unstable errors-in-row + 1 unstable SBU + 2 SBUs
5			`0xAA`	81.00	destructive SEE
6			`0x00`	6.70	×
7			`0x00`	13.00	×
8			`0x00`	93.00	destructive SEE
9			`0x55`	24.00	SEFI
10			`0x00`	5.90	SEFI
11			`0x00`	2.90	×
12		Dynamic	March C	4.40	×
13	FRAM (4-Mbit)	Static	`0x55`	3.30	×
14		Dynamic	March C	9.20	4 SBUs
15		Static	`0x55`	6.20	destructive SEE
16			`0x55`	3.90	×
17			`0x55`	6.10	×

In the first round, no bitflips were observed, but several events were detected in Rounds 2-4 when tripling the flux with respect to the first round. Isolated SBUs, "unstable" SBUs and "errors-in-row" were observed, as indicated in the table. The latter is a particular kind of multiple events that affected consecutive bits in the same row (physically speaking), following the same terminology as Ju et al. [Ju+22], which is another related work on COTS FRAMs.

Figure 5.21 shows the bitmap display panel for the bitflips observed in some of these rounds, obtained with a graphical tool provided by the manufacturer. Each bitflip is shown as 2 colored squares since the FRAM cells of this memory are 2T-2C and each square indicates a single capacitor being affected by a bitflip. Errors are displayed as colored square blocks in the location corresponding to the bit's actual physical die location. The color of a flipped bit is consistent with the I/O line for that bit; which means each bit in a word has a unique color. Non-flipped bits are represented in the white sections, and portions of the die with no active bits (divisions between sections, segments, etc.) are shown in gray color.

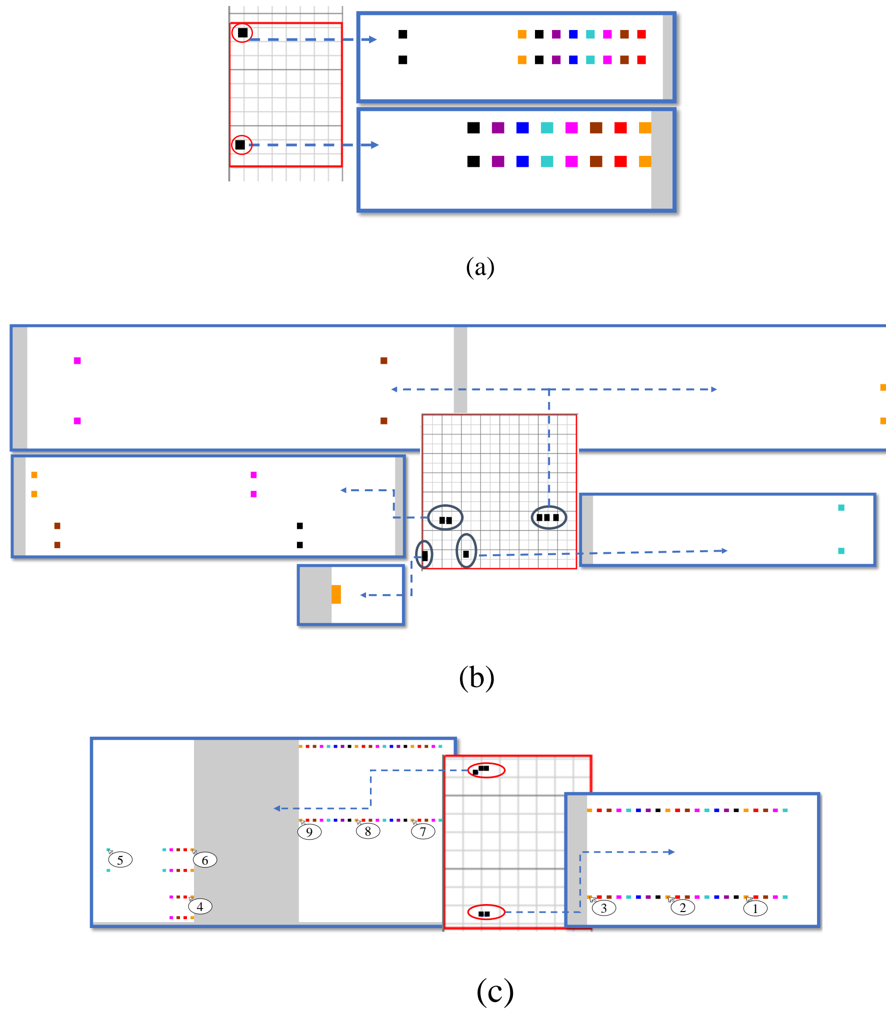

Figure 5.21: *a) 2 errors-in-row and 1 SBU (all unstable), adding 17 bitflips, were observed on the CY15B102Q FRAM under 15.3-MeV protons (Round 2 in Table 5.8) b) 9 isolated SBUs (6 of which were unstable) were observed on the same memory (Round 3 in Table 5.8) c) 4 errors-in-raw (unstable) and 3 isolated SBUs, adding 52 bitflips, were observed on the CY15B102Q FRAM under 15.3-MeV protons (Round 4 in Table 5.8). 2 errors-in-raw affected consecutive addresses, whose starting locations are also indicated in the figure.*

The highest particle fluences and fluxes belonged to Rounds 5 and 8, which caused permanent damage to the memories (a destructive SEE occurred on those occasions), and the tested devices had to be replaced. In Round 9, all addresses were visibly stuck at "0," but no such stuck bits were found after a power cycle; so that was considered as a SEFI. Another SEFI, this time affecting 40,000 addresses with random contents was also observed in Round 10. Finally, the CY15B102Q received a fluence of $4.40{\times}10^{11}$ p/cm^2 in a dynamic experiment (Round 12), where no SEEs were observed.

Five more rounds were carried out on the CY15B104Q FRAM (Rounds 13-17 of Table 5.8). Fluxes ranged from $0.22{\times}10^9$ to $0.51{\times}10^9$ p/s/cm^2 with exposure times varying from 20 to 30 minutes. Rounds 14 and 15 yielded the most important findings. In Round 14 (where a

Table 5.9: *Rounds of irradiation carried out for the FRAMs (2-Mbit CY15B102Q and 4-Mbit CY15B104Q) under 1-MeV protons*

N^o	Sample	Test type	Pattern	Fluence ($\times 10^{10}$) (p/cm^2)	Observed events
1	FRAM (2-Mbit)	Static	`0x55`	4.99	×
2			`0x55`	16.60	SEFI
3			`0x55`	0.83	×
4			`0x00`	0.83	×
5			`0xAA`	2.50	×
6			`0x55`	1.30	×
7			`0xAA`	1.30	×
8			`0xAA`	4.00	×
9			`0xAA`	3.30	×
10			`0x55`	8.30	×
11			`0xAA`	4.00	×
12			`0xAA`	10.00	SEFI
13		Dynamic	March C	15.00	destructive SEE
14			March C	13.00	×
15			March C	25.00	destructive SEE
16			March C	24.00	destructive SEE
17	FRAM (4-Mbit)	Static	`0x55`	2.20	×
18			`0x55`	3.40	×
19			`0xAA`	6.80	×
20			`0x55`	4.10	×
21			`0x55`	8.30	×
22			`0xAA`	4.90	×
23			`0xFF`	8.60	destructive SEE
24		Dynamic	March C	21.00	×
25				28.40	destructive SEE

March-C dynamic test was applied), 4 isolated bitflips were observed, without any evidence of multiple events. A destructive SEE occurred in Round 15 once the device was irradiated with a fluence of 6.20×10^{11} p/cm^2. No SEEs were observed in Rounds 13, 16 and 17.

5.3.2 CY15B102Q and CY15B104Q: Experimental results under 1-MeV protons

In this case, the FRAMs were delidded prior to the irradiation tests. 25 rounds were performed throughout the campaign, including static and dynamic modes as shown in Table 5.9.

At first, the CY15B102Q experienced a fluence of 4.99×10^{10} p/cm^2, and no SEE occurred. Thus, the fluence was increased to 16.6×10^{10} p/cm^2 increased in the next round, but a SEFI occurred. In Rounds 3 to 11, the fluence was lower compared to Round 2, and no errors were observed. In Round 12, the fluence was increased to 10.00×10^{10} p/cm^2, which again caused a SEFI to the memory (as in Round 2). Finally, Rounds 13 to 16 were dynamic tests on the

Table 5.10: *Rounds of irradiation carried out for the FRAMs (2-Mbit CY15B102Q and 4-Mbit CY15B104Q) under thermal neutrons*

N^o	Sample	Test type	Pattern	Fluence ($\times 10^{11}$) (n/cm^2)	Observed events
1	FRAM (2-Mbit)	Static	`0x55`	6.30	$\times$
2			`0xAA`	2.52	$\times$
3			`0xAA`	6.30	$\times$
4			`0x55`	6.30	$\times$
5			`0xFF`	14.40	$\times$
6		Dynamic	March C	20.00	$\times$
7			March DS	28.80	$\times$
8	FRAM (4-Mbit)	Static	`0x55`	6.30	$\times$
9			`0xAA`	6.30	$\times$
10			`0xAA`	7.20	$\times$
11		Dynamic	March C	40.10	$\times$
12			March DS	31.00	2 SBUs
13			March DS	58.80	3 SBUs

CY15B102Q. Among these, only in Round 14 no errors were observed, and in the rest (with fluences ranging from 15.00×10^{10} to 24.00×10^{10} p/cm^2), the memory was permanently damaged again.

Rounds 17 to 25 in Table 5.9 show the tests performed on the CY15B104Q. For the static tests of Rounds 17-23, no errors were observed except for Round 23, where the fluence was the highest one among these (8.60×10^{10} p/cm^2), which provoked permanent damage on the memory. For the dynamic test of Round 24, surprisingly, no errors were observed at a fluence of 21.00×10^{10} p/cm^2, but a slight increase in the fluence (Round 25) permanently damaged the memory again.

5.3.3 CY15B102Q and CY15B104Q: Experimental results under thermal neutrons

In this case, 13 rounds were performed, which are displayed in Table 5.10. No errors were observed in static modes, but for the dynamic ones, 2 and 3 SBUs affected consecutive addresses in the the CY15B104Q, in Rounds 12 and 13, respectively. Figure 5.22 shows the SBUs detected in these rounds.

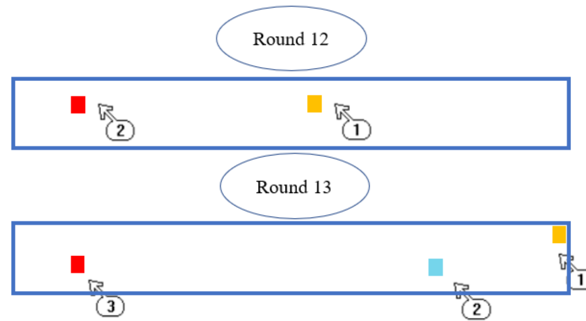

Figure 5.22: *SBUs that were observed on the CY15B104Q FRAM under thermal neutrons (Rounds 12 and 13 in Table 5.10).*

5.3.4 CY15B102Q and CY15B104Q: Experimental results under 14.8-MeV neutrons

Finally, 6 more rounds (3 static tests and 3 dynamic ones) were performed on the FRAMs under 14.8-MeV neutrons. Results are presented in Table 5.11. In Round 1, 2 10-bit errors-in-raw + 2 SBUs were observed, affecting consecutive addresses, as shown in Figure 5.23. The same tool used for Figure 5.21 was used here again to obtain the XY representation of the observed bitflips.

Finally, one more isolated SBU was observed in the same memory when carrying out a dynamic March-C test (Round 3 in Table 5.11).

Table 5.11: *Rounds of irradiation carried out for the FRAMs (2-Mbit CY15B102Q and 4-Mbit CY15B104Q) under 14.8-MeV neutrons*

N^o	Sample	Test type	Pattern	Fluence ($\times 10^{10}$) (n/cm^2)	Observed events
1	FRAM (2-Mbit)	Static	0x55	2.50	2 errors-in-row + 2 SBUs
2			0xAA	2.50	×
3		Dynamic	March C	2.40	1 SBU
4			March DS	2.44	×
5	FRAM (4-Mbit)	Static	0x55	2.25	×
6		Dynamic	March C	2.21	×

5.3.5 CY15B102Q and CY15B104Q: Discussion of experimental results

The tested FRAMs proved to be very resilient against errors provoked by radiation, both under 1-MeV/15.3-MeV protons and thermal/14.8-MeV neutrons. Yet, the following types of errors were found on the FRAMs:

- Unstable SBUs and errors-in-row.

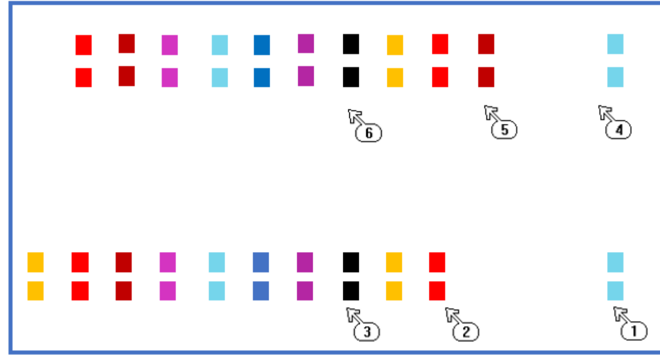

Figure 5.23: *2 errors-in-raw + 2 SBUs, adding 22 bitflips, were observed on the CY15B102Q FRAM under 14.8-MeV neutrons (Round 1 in Table 5.11).*

- SBUs.
- SEFIs.
- Destructive SEEs.

Such unstable errors on FRAMs were also reported by Wei et al. [Wei+19], this time on the FM28V100 FRAM manufactured by Infineon Technologies and under 6.1-MeV heavy ions. In that work, the authors believed that these errors might be due to errors in the decoder circuit. These errors were only observed under 15.3-MeV protons and on the 2T-2C CY15B102Q FRAM.

Errors-in-row were consistent with the ones observed by Ju et al. [Ju+22] on the FM22L16 FRAM (also manufactured by Infineon Technologies), who demonstrated that they originated in N-well resistors in the peripheral circuits, through tests conducted with laser.

SEFIs were observed quite often on the CY15B102Q, for 1-MeV and 15.3-MeV protons. It is suspected that this was due to errors in the combinatorial logic used to implement I/O operations, which propagate to the rest of the device and provoke communication issues. These SEFIs were similar to the ones detected in other works, such as [SG+02; Zha+15]. In [SG+02], Scheick et al. examined the FM1806 and FM1808 devices under heavy ions, and found SEFIs due to errors in the devices' peripheral circuitry. In [Zha+15], Zhang et al. found, through laser tests in a similar device (the FM18W08 FRAM) a SEFI-sensitive area exactly in the physical location of the device's peripheral circuit.

Apart from the fact that the CY15B102Q is manufactured with 2T-2C cells and the CY15B104Q with 1T-1C cells, it was not possible to obtain further information from the manufacturer about the physical implementation of both FRAMs. However, results suggest that the latter is more robust against radiation effects, by the look of Tables 5.8 and 5.9, since no SEFIs were observed on the CY15B104Q. The very few SBUs that were spotted (in concordance with other related works on FRAMs under heavy ions [Nun+07]) do not allow extracting further

conclusions.

Additionally, both memories proved to be sensitive against high proton fluxes. The CY15B102Q suffered permanent damage under 1-MeV 15-25 $\times 10^{10}$ p/cm^2. For 15.3-MeV, higher fluences (81-93 $\times 10^{10}$ p/cm^2) were needed to provoke the same effect, which is consistent with the well-known fact that low-energy protons contribute more significantly to the total SER than higher-energy ones [Dod+15]. Also, in comparison with the work of Jia et al. [Wei+19], who examined the parallel FM28V100 FRAM, it is noteworthy to state that heavy ions never provoked permanent damage on that device. It can be attributed the permanent damage observed on the CY15B102Q and CY15B104Q (see Tables 5.8 and 5.9) to some kind of latchup occurred in the combinatorial logic of the devices, which is more complex for serial devices, and traditionally not as radiation-hardened by design as memory cells.

Finally, to our knowledge, the radiation effects of neutrons and thermal neutrons have not been studied on these memories so far. Results shown in Tables 5.10 and 5.11 suggest that these devices are quite robust against neutrons if we compare results with protons. The few amounts of such errors do not allow extracting conclusions when comparing the CY15B102Q and the CY15B104Q; or the static and dynamic tests.

5.4 Fujitsu ReRAMs (MB85AS4MT and MB85AS8MT): Experimental results and discussion

This section discusses the SEE susceptibility of the ReRAMs of Table 4.1 under low-energy protons, thermal and 14.8-MeV neutrons.

5.4.1 MB85AS4MT and MB85AS8MT: Experimental results under 1-MeV protons

The MB85AS4MT ReRAM was examined against low-energy protons. Results are depicted in Table 5.12. In Rounds 1-3, no errors were observed, but when increasing the fluence to 13.80$\times 10^{10}$ p/cm^2, all memory addresses were permanently stuck-at-0, so it had to be replaced with a new one. This new device, in Rounds 5-7, did not experience any error, but at a higher fluence (18.00$\times 10^{10}$ p/cm^2) again it became unusable (this time, a destructive SEE was observed). The last one that was tested (Rounds 9-11) experienced another permanent stuck-at-0 (Round 11) at high fluence.

Table 5.12: *Rounds of irradiation carried out for the MB85AS4MT ReRAM under 1-MeV protons*

N^o	Fluence ($\times 10^{10}$) (p/cm^2)	Observed events
1	0.84	×
2	3.42	×
3	11.40	×
4	13.80	Permanent stuck-at-0
5	3.60	×
6	6.00	×
7	12.00	×
8	18.00	destructive SEE
9	6.00	×
10	12.00	×
11	18.00	Permanent stuck-at-0

5.4.2 MB85AS4MT and MB85AS8MT: Experimental results under thermal neutrons

This time, both the MB85AS4MT (4 Mbits of capacity) and MB85AS8MT (8 Mbits of capacity) were exposed to thermal neutrons. Tables 5.13 and 5.14 show the rounds of irradiation for both devices. Neutron fluxes were either 2.1×10^9 or 2.4×10^9 n/cm$^2/s$ (because they were carried out at different times in the same facility), but in any case, the table shows the total neutron fluences for each one of the rounds. Also, different bias voltages were tested in order to evaluate the possible effect of Dynamic Voltage Scaling (DVS) on the memory, which is known to have negative effects on the reliability of SRAMs [Cle+18; Rez+20; Rez+22].

As Table 5.13 indicates, many SEFIs involving communication loss with the memory were observed at the static tests on the MB85AS4MT, which were possible to recover after a power cycle on the memory. A recoverable stuck-at-0 was also observed in Round 10. Tests at bias voltages lower than the nominal one (i.e., <3.30 V), seem to point to a higher susceptibility of this memory against radiation effects (especially SEFIs).

Dynamic tests (Rounds 25-28 in Table 5.13) were also carried out at different bias voltages. In all of them, SEFIs were observed, consisting in a total malfunction of the dynamic stress test that was carried out (March C or March DS). In all cases, a power cycle solved the problem.

Finally, Table 5.14 shows the rounds of irradiation made on the MB85AS8MT ReRAM under thermal neutrons. Static and dynamic tests, as well as rounds made at different bias voltages, were carried out. Contrarily to the tests shown in Table 5.13, the MB85AS8MT showed total immunity against thermal neutrons. However, SEFIs were observed in the 4 dynamic tests made on this memory (Rounds 12-15). SEFIs in both devices in dynamic tests indicate that the surrounding I/O logic must not be very different in both cases.

Table 5.13: *Rounds of irradiation carried out for the MB85AS4MT ReRAM under thermal neutrons*

Nº	Test type	Pattern	Voltage (V)	Fluence ($\times 10^{11}$) (n/cm^2)	Observed events
1	Static	`0x55`	3.30	6.30	SEFI
2		`0x55`	3.30	2.52	×
3		`0xFF`	3.30	6.30	SEFI
4		`0xFF`	3.30	12.60	SEFI
5		`0xFF`	3.30	25.20	SEFI
6		`0xFF`	3.20	12.60	×
7		`0xFF`	3.09	12.60	×
8		`0xFF`	2.99	6.30	SEFI
9		`0xFF`	2.88	6.30	×
10		`0xFF`	2.78	6.30	Stuck-at-0
11		`0x55`	2.78	6.30	SEFI
12		`0xFF`	2.68	6.30	SEFI
13		`0xFF`	3.30	6.30	×
14		`0xFF`	3.20	6.30	×
15		`0xFF`	3.09	6.30	×
16		`0xFF`	2.99	6.30	SEFI
17		`0xFF`	2.89	6.30	SEFI
18		`0xFF`	2.78	6.30	SEFI
19		`0xFF`	2.68	6.30	SEFI
20		`0xFF`	2.56	6.30	SEFI
21		`0xFF`	2.47	6.30	×
22		`0xFF`	2.37	6.30	SEFI
23		`0xFF`	2.26	6.30	SEFI
24		`0xFF`	2.16	6.30	SEFI
25	Dynamic	March C	3.30	37.20	SEFI
26		March C	2.47	16.20	SEFI
27		March C	2.26	49.60	SEFI
28		March DS	3.30	86.40	SEFI

5.4.3 MB85AS4MT and MB85AS8MT: Experimental results under 14.8-MeV neutrons

Both ReRAMs were also examined under 14.8-MeV neutrons. The experiments that were carried out are summarized in Table 5.15. Similarly, as with thermal neutrons, no errors were observed in any of these memories in the static tests, but for 2 out of the 3 dynamic ones, SEFIs occurred.

5.4.4 MB85AS4MT and MB85AS8MT: Discussion of experimental results

The most common kind of error observed in the tested ReRAMs was SEFIs. In this case, no isolated SBUs were detected, and permanent damage was only provoked under 1-MeV protons

Table 5.14: *Rounds of irradiation carried out for the MB85AS8MT ReRAM under thermal neutrons*

N^o	Test type	Pattern	Voltage (V)	Fluence ($\times 10^{11}$) (n/cm^2)	Observed events
1	Static	0x55	3.30	6.30	×
2		0xFF	3.30	6.30	×
3		0xFF	3.20	6.47	×
4		0xFF	3.09	6.30	×
5		0xFF	2.99	6.30	×
6		0xFF	2.89	6.30	×
7		0xFF	2.78	6.30	×
8		0xFF	2.68	6.30	×
9		0xFF	2.56	6.30	×
10		0xFF	2.47	6.30	×
11		0xFF	2.37	6.30	×
12	Dynamic	March C	3.30	22.60	SEFI
13		March C	2.37	38.40	SEFI
14		March C	2.99	14.40	SEFI
15		March DS	3.30	18.70	SEFI

Table 5.15: *Rounds of irradiation carried out for the ReRAMs (4-Mbit MB85AS4MT and 8-Mbit MB85AS8MT) under 14.8-MeV neutrons*

N^o	Sample	Test type	Pattern	Fluence ($\times 10^{10}$) (n/cm^2)	Observed events
1	ReRAM (4-Mbit)	Static	0x55	0.68	×
2			0xFF	1.36	×
3		Dynamic	March C	1.23	×
4			March DS	2.04	SEFI
5	ReRAM (8-Mbit)	Static	0xFF	1.02	×
6		Dynamic	March C	1.25	SEFI

at a very high fluence (>13.80 $\times 10^{10}$ p/cm^2).

SEFIs were also observed in other related works on ReRAMs, such as Chen et al. [Che+14], who tested the Panasonic MN101L microcontroller under heavy ions. They attributed such errors to the peripheral circuits, not the memory array. Lyu et al. and Bi et al. also tested the MB85AS4MT ReRAM with a pulsed laser, showing extremely high robustness of memory cells, but its peripheral IO interface circuit (built with CMOS technology) was susceptible to SEFIs [He+21; Bi+13]. A team of NASA [OBr+13] also used a pulsed laser to test a 180-nm CMOS ReRAM. Again, the resistive memory array was robust against SEUs, but the sense amplifiers was an important source of SEFIs. Finally, Bi et al. [Bi+19] observed SEFIs of the MB85AS4MT ReRAM under heavy ions, which was confirmed and exclusively located in the peripheral circuits via a pulsed laser scan.

The MB85AS4MT and MB85AS8MT ReRAMs underwent permanent damage considerably less frequently than the FRAMs that were discussed in Section 5.3. Other related works such as

Lyu et al. [He+21], also showed that the MB85AS4MT was not sensitive against such permanent damage, this time under heavy ions.

A comparison between the MB85AS4MT and the MB85AS8MT (Tables 5.13 and 5.14, static tests) clearly indicates that the latter is much more resilient against SEFIs affecting the normal operation of the devices. This is true for thermal neutrons, however for 14.8-MeV ones, their response looks to be quite similar (Table 5.15).

Finally, both memories were considerably more sensitive against errors when working in dynamic mode, as the FRAMs evaluated in the previous section did. This is consistent with the work of Bi et al. [Bi+19], who also evaluated the MB85AS4MT under TID synergistic effects. To our knowledge, no other works have evaluated radiation effects' impact on the dynamic operation of ReRAMs.

5.5 Everspin MRAMs (MR10Q010CSC and MR25H40CDF): Experimental results and discussion

The MRAMs in Table 4.1 were tested under thermal and 14.8-MeV neutrons. Results are discussed in detail in the following subsections.

5.5.1 MR10Q010CSC and MR25H40CDF: Experimental results under thermal neutrons

9 and 7 rounds of irradiation were carried out on the MR25H40CDF and MR10Q010CSC, respectively, under thermal neutrons, as indicated in Table 5.16.

The MR25H40CDF did not experience any failure for the 8 static + 1 dynamic tests that were made under neutron fluences up to 12.6×10^{11} n/cm^2 (for static tests) and 28.32×10^{11} n/cm^2 (for the dynamic one). The MR10Q010CSC was also quite robust in the static tests, but SEFIs were detected in 2 out of the 3 dynamic tests that were carried out.

5.5.2 MR10Q010CSC and MR25H40CDF: Experimental results under 14.8-MeV neutrons

3 more tests (1 static + 2 dynamic ones) were done on both MRAMs, as Table 5.17 indicates. All these rounds yielded no errors. In general, both MRAMs demonstrated to be quite robust against fast neutrons.

Table 5.16: *Rounds of irradiation carried out for the MRAMs (4-Mbit MR25H40CDF and 1-Mbit MR10Q010CSC) under thermal neutrons*

N^o	Sample	Test type	Pattern	Fluence ($\times 10^{11}$) (n/cm^2)	Observed events
1	MRAM (4-Mbit)	Static	`0xFF`	6.3	×
2			`0xAA`	6.3	×
3			`0x00`	12.6	×
4			`0x55`	6.3	×
5			`0x55`	7.2	×
6			`0x00`	7.2	×
7			`0xFF`	7.2	×
8			`0xAA`	7.2	×
9		Dynamic	March DS	28.3	×
10	MRAM (1-Mbit)	Static	`0x55`	7.2	×
11			`0x00`	7.2	×
12			`0xAA`	7.2	×
13			`0xFF`	7.2	×
14		Dynamic	March C	12.5	SEFI
15			March DS	19.8	SEFI
16			March DS	57.8	×

Table 5.17: *Rounds of irradiation carried out for the MRAMs (4-Mbit MR25H40CDF and 1-Mbit MR10Q010CSC) under 14.8-MeV neutrons*

N^o	Sample	Test type	Pattern	Fluence ($\times 10^{10}$) (n/cm^2)	Observed events
1	MRAM (4-Mbit)	Static	`0x55`	2.75	×
2		Dynamic	March C	1.24	×
3			March C	1.30	×
4	MRAM (1-Mbit)	Static	`0xFF`	2.75	×
5		Dynamic	March C	0.99	×
6			March DS	0.99	×

5.5.3 MR10Q010CSC and MR25H40CDF: Discussion on experimental results

Other related works on the UT8MR2M8, MR0A08B, MR2A16A, and AS008MA12A-C1SC MRAMs [Nun+07; Ing+19; Haf+12; OBr+13; Hei14] proved them to be as resilient against heavy ions, protons, neutrons and alpha particles as the MR25H00 and MR10Q010 devices discussed in this Ph.D. thesis. Following the same trend as with FRAMs and ReRAMs, MRAMs were sensitive against SEFIs in dynamic tests. Tsiligiannis et al. [Tsi+13] also observed such SEFIs on the 4-Mbit toggle MRAM, and Nuns et al. [Nun+07] showed that the MR2A16A device was susceptible to SELs against heavy ions, but no SEUs were seen under 200-MeV protons. As in the case of FRAMs and ReRAMs, a possible explanation could be the CMOS peripheral circuitry being used in reads and writes in the MTJ cells, which is susceptible against

Table 5.18: *An overview of the detected SEEs on FRAMs, ReRAMs, and MRAMs. For simplicity, the table summarizes radiation effects observed in any of the following particle sources: 1-MeV and 15.3-MeV protons, as well as thermal and 14.8-MeV neutrons*

N^o	Sample	Observed events						
		SBUs	SEFIs	Destructive SEEs	Stuck-at-0's	Permanent stuck-at-0's	Unstable SBUs	Unstable errors-in-row
1	FRAM (2-Mbit)	Yes	Yes	Yes	×	×	Yes	Yes
2	FRAM (4-Mbit)	Yes	×	Yes	×	×	×	×
3	ReRAM (4-Mbit)	×	Yes	Yes	Yes	Yes	×	×
4	ReRAM (8-Mbit)	×	Yes	×	×	×	×	×
5	MRAM (4-Mbit)	×	×	×	×	×	×	×
6	MRAM (1-Mbit)	×	Yes	×	×	×	×	×

radiation [Zha+14]. The manufacturer totally confirmed these assumptions about the observed events in the MRAM devices. Finally, other related works [Haf+12; Tsi+13; Bol13; Ji+19b; HJG17] also demonstrated that toggle MRAMs, especially in static mode, were immune against SELs, SEUs, or MBUs.

Finally, Table 5.18 summarizes all the radiation effects observed on the FRAMs, ReRAMs and MRAMs discussed in Sections 5.3, 5.4, and 5.5. As can be seen in the table, the CY15B102Q FRAM underwent up to 5 types of SEEs, whereas the MR25H40CDF did not undergo any type of radiation effect.

5.6 Artix-7 XC7A100T FPGA: Experimental results and discussions

This section provides the sensitivity of the Artix-7 XC7A100T FPGA of Table 4.1 under 14.2-MeV neutrons and 25-meV thermal neutrons. Besides, the extraction methods of information retrieval from the FPGA will be presented.

5.6.1 Artix-7 XC7A100T FPGA: Stages to run each test

This section describes the methodology that was used to extract the information from the configuration memory of the FPGA (CRAM) and, thus, to check the SEEs that occurred after exposing this device against radiation. For this purpose, a modified version of OpenOCD software [Ope22] was used to implement the *GCapture* instruction and the *readback* operation

[J C21] to communicate with the FPGA. These modifications allow us to read back the whole FPGA's configuration memory and even frame by frame[1]. By performing a *GCapture* operation before the *readback* procedure, it was possible to read the actual state of the FFs of the FPGA architecture. The following stages were used for each test:

1. The target design is first loaded. This bitstream will be later referred to as "golden" since it contains information that has not been corrupted by radiation. This design was a large shift counter using 126,800 FFs, which is 63% of the total FFs of the FPGA. No more than this amount of FFs could be used in the design since the Xilinx Vivado tool could not synthesize and implement it otherwise. In the HDL code itself, 50% of these FFs were initialized to 1's and the rest to 0's.

2. To initialize each byte of the BRAM with a 0x55 pattern. This was done manually, again by modifying the HDL code itself of the design.

3. To irradiate the device in different times.

4. To perform a *readback* of the whole CRAM and save it in the control computer in a binary file.

5. To get the actual status of the FFs in the design. For this purpose, a *GCapture* command followed by another *readback* of the CRAM is executed. The *GCapture* copies the bits from the FFs of the FPGA architecture into some specific bits of the CRAM. Subsequently, it was possible to locate these specific bits by using the .ll file generated during synthesis.

6. Finally, the two files that were obtained in Steps 4 and 5 are compared with the "golden" CRAM values. On the one hand, the differences between the first *readback* (Step 4) and the "golden" give the bitflips that occurred in the CRAM. On the other hand, the differences between some specific bits from the second *readback* (which are extracted with the .ll file as explained in Step 5) and those of the "golden" show the bitflips occurred in the architectural FFs of the FPGA.

5.6.2 Artix-7 XC7A100T FPGA: Extraction of the bitflips

When carrying out the first *readback* (Step 4, in Subsection 5.6.1), the whole contents of the CRAM of the FPGA are retrieved, which can be saved in a binary file. Hence, by comparing this file with the "golden" bitstream (Step 1, in Subsection 5.6.1), one can obtain the bitflips that occurred in the FPGA's CRAM.

[1]A frame is the smallest reconfiguration block of Xilinx FPGAs

Then, when a *GCapture+readback* are carried out (Step 5, Subsection 5.6.1), another binary file can be generated, this time containing, in some specific locations, the values of the FFs of the FPGA's architecture at the moment of carrying out the *GCapture* (i.e., after radiation). The specific locations of the values of the FFs can be retrieved by using a *logic location* (.ll) file, which is generated by Vivado through the synthesis and implementation of the design.

Said .ll file is a flat text file containing one line per physical latch or BRAM bit existing in the FPGA architecture that is used in the design. Each of these lines provides the following information:

1. The bit offset of the current latch/BRAM bit with respect to the beginning of the data payload of the FPGA's programming file (i.e., .bit file) that is written on its CRAM.
2. The frame number (F) + bit offset with respect to F, which is used to access the content of that same latch/BRAM bit in the FPGA architecture.
3. The name of the involved latch/BRAM bit, which is the same as the name given by the HDL programmer for that bit of information.

By using the information in items 1) and 3) from the previous list, it is possible to extract the data stored in all latches from the whole information that is retrieved through this second *readback*. This information is then compared with the initial values that were written on the FFs in Step 2 in Subsection 5.6.1 to check if there were bitflips on them.

5.6.3 Artix-7 XC7A100T FPGA: Extraction of SBUs and MCUs

As explained in Section 4.4 from Chapter 4, in most cases researchers are unaware of the physical structure of memory or FPGAs; thus, for extracting MCUs and SBUs from the whole set of SEEs occurred on the FPGA, the LELAPE tool (Section 4.4) was used again to classify said types of events. In the case of the results obtained with the FPGA, it was observed an irregular abundance of pairs of addresses varying in 1, 2, 3230-3234, and 6462-6466.

Values 3230-3234 can be obtained as $(32\times101) \pm \{0, 1, 2\}$; and 6461-6466, as $(2\times32\times101) \pm \{0, 1, 2, 3\}$. This is related to the fact that, in Artix-7 XC7A100T Xilinx FPGAs, a frame has 101 32-bit words [Xil18]. Thus, the large-scale events suggest MCUs affecting physically close bits but belonging to different frames. For illustrative purposes, Figure 5.24 shows a scheme of the inferred physical structure of Xilinx Artix-7 FPGAs, as the researchers are unaware of the actual one. The 101 words existing in the same frame are organized vertically in the same column, so the same bit of a word in the following (or precedent) frame is 3232 bits away and 6464 bits away if considering 2 frames apart. Therefore, if bits n, n+3232, and n+6464 were

simultaneously affected by a particle, values 3232 and 6464 would be yielded if subtracting the addresses bound to those bits. Similar reasoning can be given for the rest of the values in the ranges of values 3230-3234 and 6461-6466.

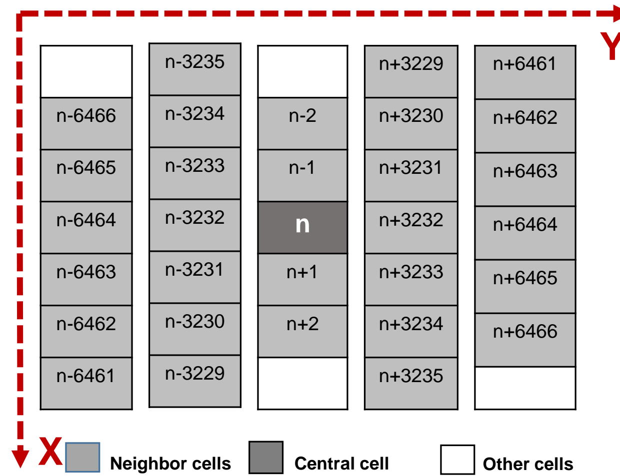

Figure 5.24: *Location of a cell with address n in the bitstream and the addresses of some of its neighbors in the Artix-7 XC7A100T FPGA.*

5.6.4 Artix-7 XC7A100T FPGA: Experimental results under 14.2-MeV neutrons

The experiments were performed in two campaigns under 14.2-MeV neutrons at the GENEPI2 facility, as reported in Table 4.2. During the irradiation, a Raspberry Pi 3 was connected to the board through the USB and GPIO (General Purpose Input Output), as depicted in Figure 5.25.

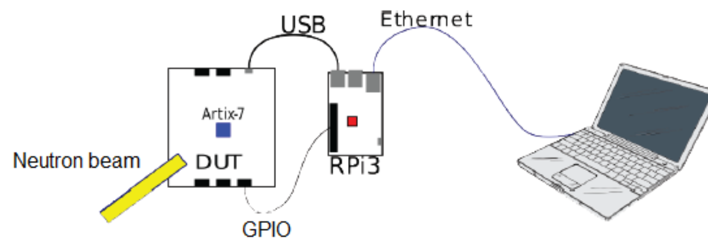

Figure 5.25: *Artix-7 XC7A100T FPGA and control system.*

Artix-7 XC7A100T FPGA: Rounds of irradiation under 14.2-MeV neutrons

Table 5.19 displays the neutron fluence received by the FPGA in the different campaigns and the total number of bitflips followed in each type of resource of the FPGA. The number of bitflips was higher in the second campaign, which might be explained by beam flux uncertainty, aging [Kas+14], or DD [Gad+12].

Table 5.19: *Irradiation rounds and number of bitflips observed for the Artix-7 XC7A100T FPGA, under 14.2-MeV neutrons*

			BitFlips	
N^o	Campaign	Fluence ($\times 10^{11}$) (n/cm^2)	CRAM	FFs
1	November 2017	0.43	56	0
2		0.48	176	0
3		1.89	278	2
4		1.26	186	1
5		2.82	383	2
6	May 2018	0.63	140	2
7		0.64	128	1
8		0.64	131	1
9		1.85	370	0
10		3.37	681	3
	Total	14.01	2429	12

Table 5.20: *Characteristics of MBUs detected of the CRAM in the Artix-7 XC7A100T FPGA*

		Experimental MBUs			False MBUs		
N^o	N$_{BF}$	2-bit	3-bit	>3-bit	2-bit (Eq. 4.1)	3-bit (Eq. 4.2)	Prob. (Eq. 5.1)
1	56	2	0	0	0.002	4.0×10^{-8}	0.2%
2	76	9	0	0	0.003	1.0×10^{-7}	0.3%
3	278	18	3	0	0.047	5.1×10^{-6}	4.6%
4	186	16	0	0	0.021	1.5×10^{-6}	2.1%
5	383	8	4	0	0.089	1.3×10^{-5}	8.5%
6	140	16	1	0	0.012	6.4×10^{-7}	1.2%
7	128	6	0	0	0.010	4.9×10^{-7}	1.0%
8	131	10	2	0	0.010	5.2×10^{-7}	1.0%
9	370	7	0	1	0.083	1.2×10^{-5}	8.0%
10	681	17	8	4	0.282	7.5×10^{-5}	24.5%

Artix-7 XC7A100T FPGA: MBUs observed under 14.2-MeV neutrons

As displayed in Table 5.19, most errors were detected in the CRAM and rarely in the FFs. Most likely due to the presence of ECC, no bitflips on the BRAM were found. Table 5.20 shows the number of MBUs of different multiplicities observed in the CRAM of the FPGA, as well as the number of "false" MBUs expected in each experiment (assuming a word width of 32 bits), following the predictions of Eqs. 4.1 and 4.2, presented in Section 4.4. The probability of observing one or false MBUs was also estimated by using Eq. 5.1.

Artix-7 XC7A100T FPGA: SBUs and MCUs observed under 14.2-MeV neutrons

The number of observed events of different sizes are displayed in Table 5.21. Next, Figure 5.26 illustrates the averaged values of the cross-sections of the CRAM against different types of

MCUs, categorized by their multiplicity.

Table 5.21: *Number of MCUs observed on the Artix-7 XC7A100T FPGA, which were extracted by using the statistical approach discussed in Section 5.6.3.*

	Event multiplicity							
Test	1	2	3	4	5	6	7	8
1	35	9	1	0	0	0	0	0
2	31	13	1	4	0	0	0	0
3	142	45	1	8	1	1	0	0
4	108	30	2	3	0	0	0	0
5	230	63	1	3	0	2	0	0
6	57	22	5	6	0	0	0	0
7	74	20	2	2	0	0	0	0
8	63	20	1	5	1	0	0	0
9	231	62	1	3	0	0	0	0
10	390	105	9	4	0	5	0	1
Total	1361	389	24	38	2	8	0	1

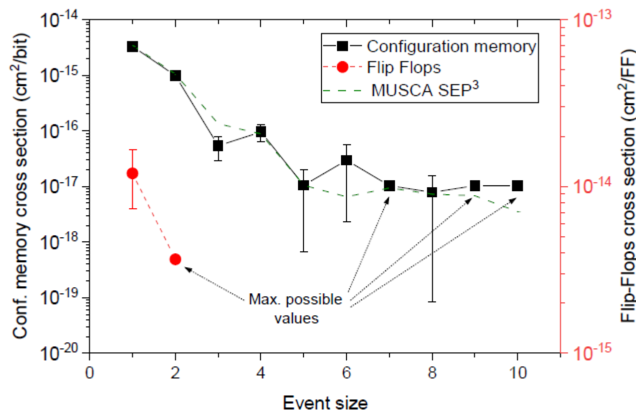

Figure 5.26: *Cross-sections for 14.2-MeV neutrons according to the event multiplicity. Note that lines are related to the different vertical axis. Displayed values are the weighted average of the values of all the tests shown in Table 5.21. Note that there are 4 dots that are related to unobserved events in which we can only provide the maximum possible value. The dashed line indicates, the cross-sections issued from MUSCA-SEP3.*

As the figure shows, the SBU and 2-bit MCU cross-sections are on the same order of magnitude. It is worth mentioning that the cross-sections for larger events lower with the multiplicity. Finally, the SBU cross-sections for FFs is higher than the CRAM ones. No multiple events were observed in the FFs, since they are very sparse to each other in the architecture of this FPGA. Also, the figure displays the predictions obtained from the tool MUSCA-SEP3 [Hub+09a]. One can notice that the tool accurately anticipates the cross-sections for all multiplicities.

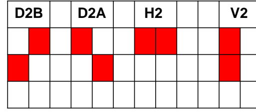

Figure 5.27: *Observed shapes for 2-bit MCUs under 14.2-MeV neutrons in the Artix-7 XC7A100T FPGA.*

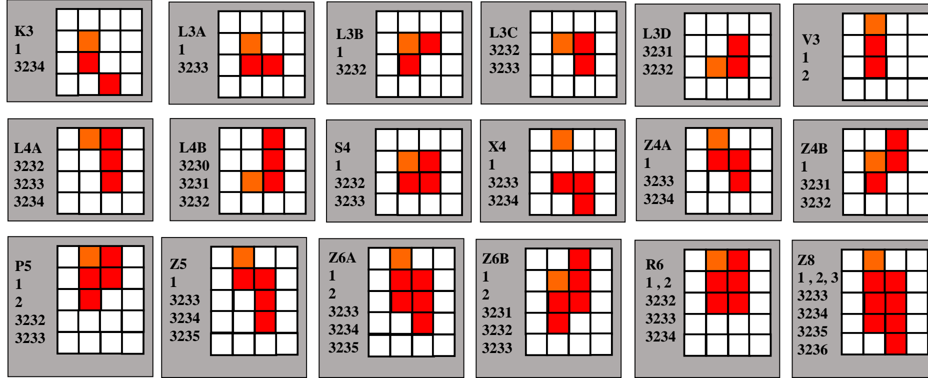

Figure 5.28: *Observed shapes for 3-8 bit MCUs and their signature in the bitstream under 14.2-MeV neutrons in the Artix-7 XC7A100T FPGA.*

Artix-7 XC7A100T FPGA: Hypothetical shape of MCUs under 14.2-MeV neutrons

Studying the shape of multiple events is possible by associating the index in the bitstream of cells in multiple events with the probable position in the XY plane. Figures 5.27 and 5.28 show the observed shapes of 2 and 3 to 8-bit MCUs, respectively. Each event has a name on it ("K3," "L3A," etc) and some numbers (which can be seen as the event's signature), pointing to the distances between the reference cell and each one of the others. As figures reveal, multiple events occur vertically most along the wordlines. In fact, the events involving just one or two adjacent columns were detected, but up to 5 rows were affected in Z8, as reported in Figure 5.28. In largest events, the directionality is common; which clearly suggests that the worlines are physically organized in groups of 2 nearby columns, as suggested in [Kat+19] and [Lia+19]. This suggests the existence of some sort of physical barrier that separates pairs of columns and avoids the propagation of the events along the X-axis. On the other hand, SBUs were equally distributed, indicating no preference for even or odd columns. Shapes displayed in Figures 5.27 and 5.28 are similar to those reported by authors in [Du+19] after irradiating a 28-nm Xilinx Kintex-7 SRAM-based FPGA under ultrahigh energy heavy-ions. Finally, events spanning over 3 or more different columns didn not occur, which is coherent with the barrier mentioned above.

5.6.5 Artix-7 XC7A100T FPGA: Experimental results under thermal neutrons

Tests on this FPGA were carried out in March 2021 under thermal neutrons at the ILL, as presented in Table 4.2. A control computer was connected to the DUT through a USB-to-JTAG connection to run the tests as displayed in Figure 5.29 a). The FPGA was irradiated with 6 incident angles. These are depicted in Figure 5.29 b): Normal front and back incidences, grazing angles in two directions (East-West (EW) and North-South (NS)), 45°, and 135°.

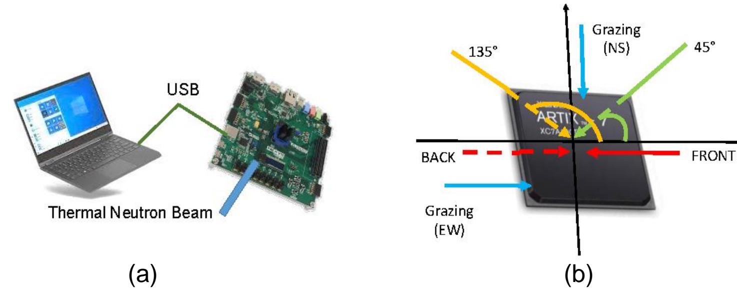

Figure 5.29: *The Artix-7 XC7A100T FPGA under thermal neutrons a) Experimental setup. b) Beam incident angles that were tested.*

Artix-7 XC7A100T FPGA: Rounds of irradiation under thermal neutrons

Table 5.22 shows 17 rounds of irradiation that are categorized into 6 types depending on the incident angle. The number of observed bitflips in CRAM and FFs is approximately proportional to the particle fluence. Most bitflips appeared in the CRAM and a few in the FFs. No bitflips were observed in the BRAM. In these tests, many bitflips, several thousands in some cases, were observed, although the exposure times were short (5 minutes maximum).

Table 5.22: *Rounds of irradiation carried out for the Artix-7 XC7A100T FPGA under thermal neutrons*

N^o	Beam angle	Fluence ($\times 10^{11}$) (n/cm^2)	CRAM	FFs
1	Normal incidence (Front)	1.26	7360	25
2		2.52	14275	47
3		6.30	29829	98
4	Normal incidence (Back)	1.26	5040	14
5		2.52	10077	32
6		6.30	25356	97
7	45°	0.92	5439	27
8		1.84	11181	46
9		4.60	26888	83
10	135°	0.87	4791	16
11		1.74	9565	29
12	90°-EW	1.26	900	3
13		2.52	2089	11
14		6.30	8178	22
15	90°-NS	1.26	1395	2
16		2.52	2652	8
17		6.30	6598	20

Artix-7 XC7A100T FPGA: MBUs observed under thermal neutrons

Table 5.23 reports the observed MBUs according to their multiplicity and the estimated false ones, which were estimated by using Eqs. 4.1 and 4.2 (Subsection 4.4.2). It can be concluded that not all the MBUs observed experimentally are false ones. As an example, in Round 1, 314 2-bit MBUs were seen; 32.78 of which are considered to be false ones.

Table 5.23: *Characteristics of MBUs observed in the CRAM of the Artix-7 XC7A100T FPGA under thermal neutrons*

	Experimental MBUs			False MBUs	
N^o	2-bit	3-bit	$>$ 3-bit	2-bit	3-bit
1	314	57	20	32.78	0.069
2	674	124	55	123.32	0.47
3	1,706	292	122	538.48	3.94
4	230	41	14	15.38	0.021
5	465	69	29	61.45	0.17
6	1338	235	96	389.09	2.53
7	257	37	20	17.90	0.027
8	515	226	32	76.00	0.21
9	1459	235	79	437.53	3.04
10	227	35	3	13.89	0.019
11	494	57	36	55.36	0.14
12	26	5	3	0.49	0.000 14
13	73	8	10	2.64	0.0017
14	369	59	19	40.56	0.094
15	47	12	0	1.18	0.0005
16	135	27	10	4.25	0.003
17	296	61	20	26.34	0.048

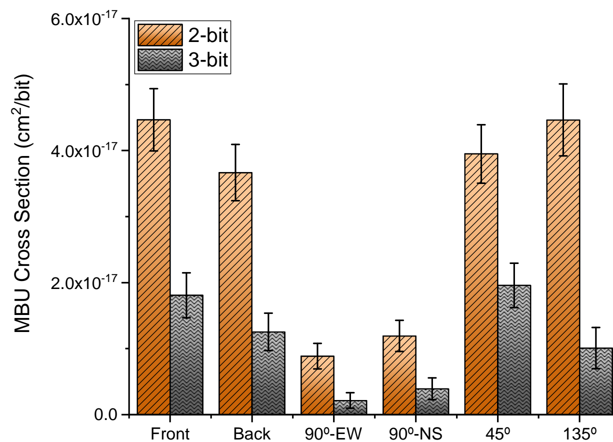

Figure 5.30: *2- and 3-bit MBU per-bit cross-sections obtained at different incident angles in the CRAM of the Artix-7 XC7A100T FPGA under thermal neutrons.*

Once these false multiple events were filtered, the per-bit cross-section plots of 2 and 3-bit MBUs at different incident angles in the CRAM are presented in Figure 5.30. Error margins

with 95% confidence are also included in the figure, as explained in [Aut+14]. The relevant finding in Figure 5.30 is that there are notable differences in the MBU cross-section depending on the incidence angle. Thus, the highest 2-bit MBU cross-sections are obtained for the front direction and 135°, the lowest one being for 90°. The 3-bit MBUs follow a similar trend, with the possible exception of the 45° and 135° cases. This might be due to the low number of such events not being high enough to extract statistically strong conclusions.

Artix-7 XC7A100T FPGA: SBUs and MCUs observed under thermal neutrons

MCUs with multiplicities ranging from 2 to 128 were identified in each test. Table 5.24 shows the MCUs observed in each case. MCUs of different multiplicities were observed in all directions, with the exception of the largest events. Events with higher multiplicities occurred much less frequently, and it was particularly surprising that MCUs in the form of clusters of 128 and 384 bits (=128×3) bits were also detected. It is suspected that these were SEFIs related to errors that emerged in the FPGA's clock distribution elements or input/output buffers (IOBUFs).

Table 5.24: *Characteristics of MCUs observed in the CRAM in the Artix-7 XC7A100T FPGA under thermal neutrons*

	Directions					
Size	Front	Back	45°	135°	90°-EW	90°-NS
2	✓	✓	✓	✓	✓	✓
3	✓	✓	✓	✓	✓	✓
4	✓	✓	✓	✓	✓	✓
5	✓	✓	✓	✓	✓	✓
6	✓	✓	✓	✓	✓	✓
7	✓	✓	✓	✓	✓	✓
8	✓	✓	✓	✓	✓	✓
9	✓	✓	✓	✓	✓	×
10	✓	✓	✓	✓	✓	×
11	✓	✓	✓	×	✓	✓
12	✓	✓	✓	×	×	×
128	✓	✓	✓	✓	✓	✓
384	×	×	✓	×	×	×

Figure 5.31 shows the 2 and 3-bit MCU cross-sections of all the 6 possible types of experiments (classified by incident angle and direction), once the MCUs were deduced from the set of observed SEUs and the false ones were estimated and filtered out from the set of MCUs that were initially identified. By the look of the figure, it can be concluded that the device had the highest MCU sensitivity at 45°, 135°, and the front direction; and the lowest at grazing angles. The back direction is in between them. This is in agreement with the results regarding MBUs presented in Figure 5.30, but at the same time, it contradicts the results that were obtained with 14.2-MeV neutrons for the [Kor+20] 130-nm nv-SRAM discussed in Section 5.1.1 (Figure 5.3), where the

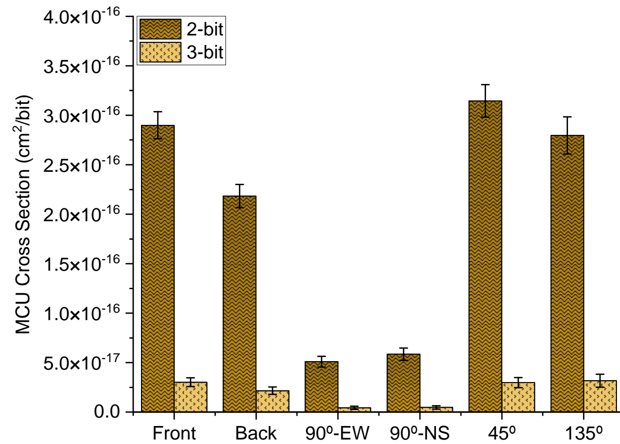

Figure 5.31: *2- and 3-bit MCU cross-sections obtained at different incident angles in the CRAM of the Artix-7 XC7A100T FPGA under thermal neutrons.*

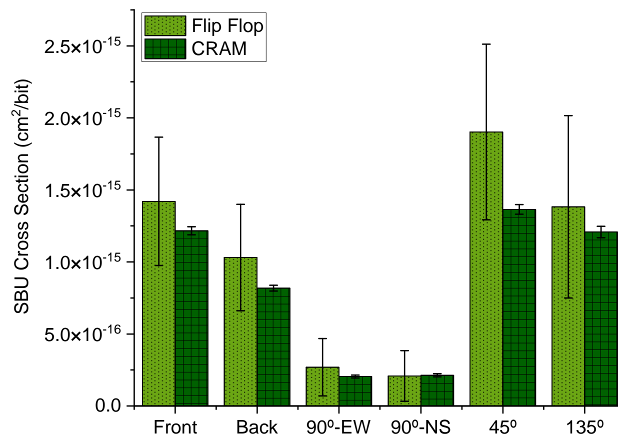

Figure 5.32: *SBU cross-sections obtained at different incident angles for the FFs and the CRAM of the Artix-7 XC7A100T FPGA under thermal neutrons.*

highest MCU sensitivity was measured at grazing angles. The differences in the SEE sensitivity between thermal and fast neutrons for this FPGA is further discussed in Section 5.6.7.

Figure 5.32 shows the sensitivity of the FFs of this FPGA under thermal neutrons. The figure only shows the SBU cross-section since FFs are not logically arranged into larger words because they are sparse in the FPGA architecture. In addition, it shows the comparison of the SBU cross-sections of CRAM cells with that of FFs. On the one hand, the sensitivity trend belonging to the incidence angle is similar to those detected in Figures 5.30 and 5.31 (highest for 45°, 135°, and the front direction, lowest for grazing angles, and in between these, the back direction). Also, the sensitivity of FFs was higher than that of the CRAM cells, albeit they are in the same order of magnitude.

Artix-7 XC7A100T FPGA: Shape of MCUs under thermal neutrons

The shapes of the MCUs observed in the Artix-7 XC7A100T FPGA under thermal neutrons were also studied. The types of 2-bit MCUs are shown in Figure 5.33. The shapes include a horizontal one (H2), two vertical ones (V2 and V2B), two diagonal ones (D2A and D2B), and two types of events in a chess-like knight-jump move (KJA and KJB). Figure 5.34 displays the abundance of these for the same 6 types of tests used in Figures 5.30, 5.31, and 5.32. The most abundant type of 2-bit MCU in all the cases was the D2A, followed by D2B and H2. Verticals and the knight-jump ones occurred very few times.

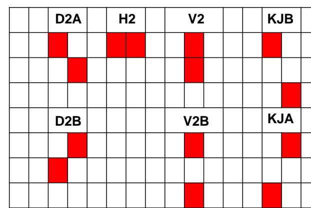

Figure 5.33: *Possible shapes of the 2-bit MCUs observed in the Artix-7 XC7A100T FPGA under thermal neutrons.*

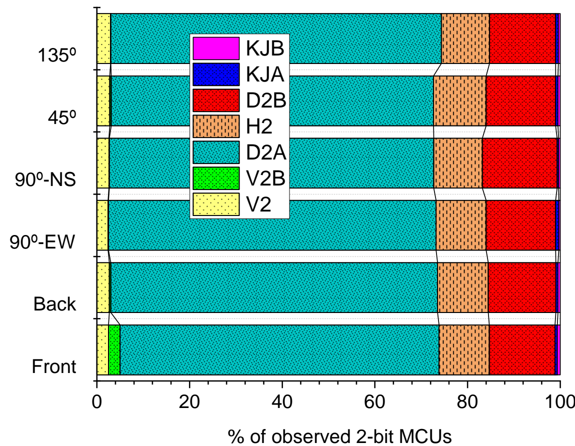

Figure 5.34: *Abundance and classification of the 2-bit MCUs observed in the Artix-7 XC7A100T FPGA under thermal neutrons, according to their shapes (Figure 5.33).*

The shapes of the 3-bit MCUs observed on this FPGA were also studied. 43 different types of such multiple events were detected, as displayed in Figure 5.35. Considering the variety of such possible multiple events, it is suspected some of the identified MCUs might stand false events resulting from the interaction of 2-bit events (usually, D2A, the most abundant) with an isolated SBU. Each event has a name on it ("XAB," "XBE," etc) and a couple of numbers, indicating distances between bitflips 1&2 and 1&3 of the 3-bit MCU, in a similar way as it was made in Figure 5.28. As previously explained in Section 5.6.3, distances in vertical increase by 1; and in horizontal by 3232 (i.e., 101x32), which is related to the addressing of the CRAM in

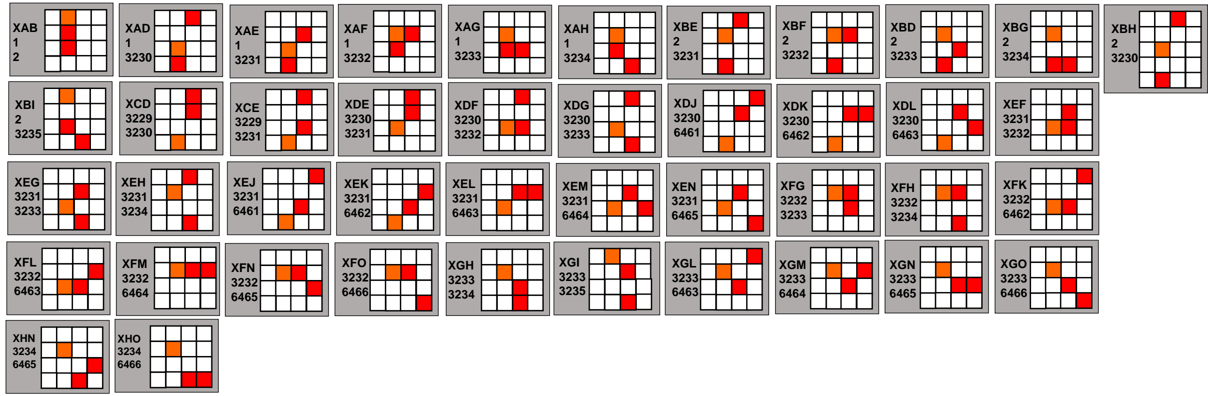

Figure 5.35: *Shapes of the 3-bit MCUs and their signatures in the bitstream observed in the Artix-7 XC7A100T FPGA under thermal neutrons.*

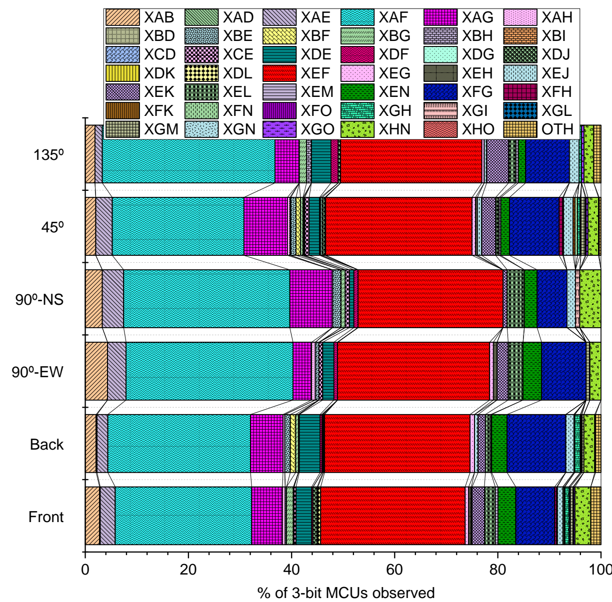

Figure 5.36: *Abundance and classification of the 3-bit MCUs observed in the Artix-7 XC7A100T FPGA under thermal neutrons, according to their shapes (Figure 5.35).*

this FPGA. Next, Figure 5.36 depicts the percentages of seen events of each type. The most observed types of 3-bit MCUs are XAF and XEF, followed by XFG. These 3 types of events are actually the result of rotating the same pattern by 90° with respect to each other, which is linked to the fact that the incident angle of particles with respect to the device's surface was different for each experiment.

As it as previously reported in Table 5.24, MCUs of larger multiplicities were also observed on this FPGA under thermal neutrons. Figure 5.37 displays the most frequently observed shapes for each multiplicity, from 4-bit through 12-bit. For each multiplicity, shapes are displayed from more to less often, from left to right, and they are named XIA, XIB, and XIC. In general, it can be observed that these multiple events are mostly organized in columns, which, again, is consistent with the addressing mode of the Artix-7 FPGA. The abundance of such events

depending on their shapes is depicted in Figure 5.38. In addition, Figure 5.37 illustrates the shapes of the events with multiplicities 128 and 384. As indicated in the figure, all these events exhibited an unexpected horizontal shape, which points to the existence of some sort of SEFI.

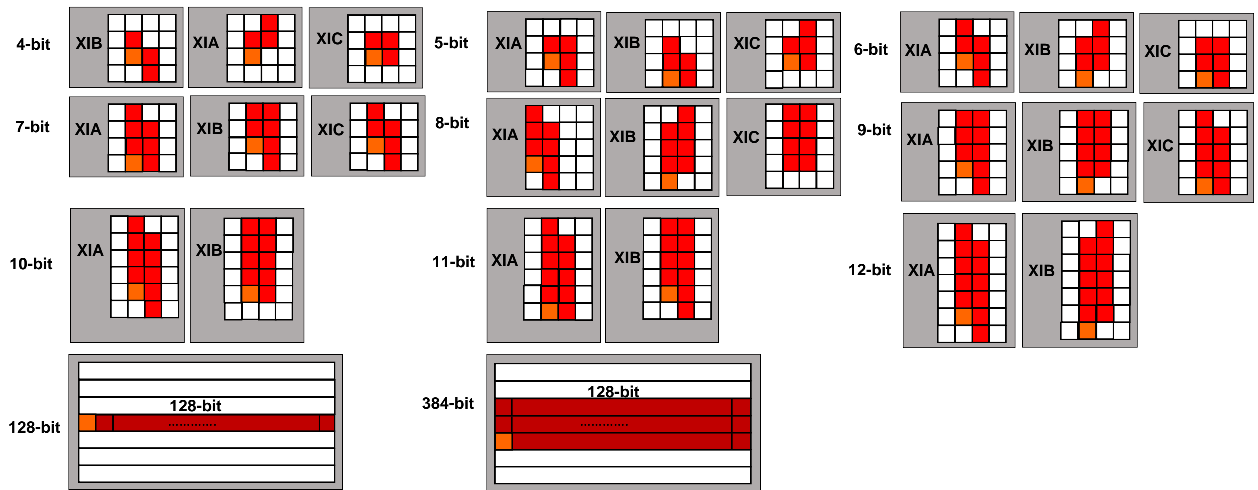

Figure 5.37: *Shapes of 4-bit to 12-bit, 128-bit and 384-bit MCUs observed on the Artix-7 XC7A100T FPGA under thermal neutrons.*

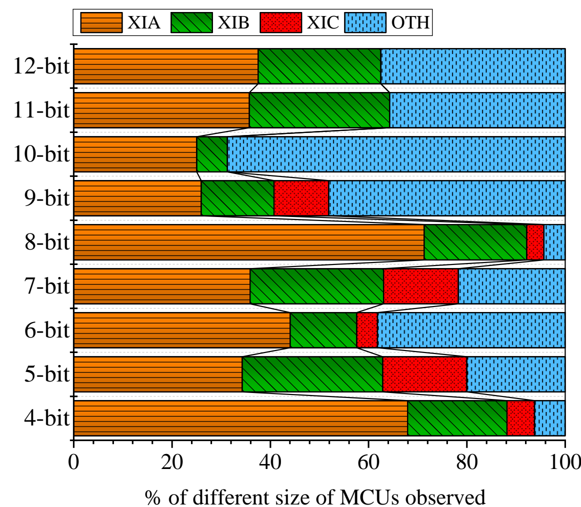

Figure 5.38: *Abundance and classification of the observed 4 to 12-bit MCUs observed in the Artix-7 XC7A100T FPGA under thermal neutrons, according to their shapes (Figure 5.37).*

5.6.6 Artix-7 XC7A100T FPGA: Comparison between of experimental results under thermal neutrons with MUSCA-SEP3 predictions

As mentioned earlier, thermal neutron-induced SEUs have been reported since the 1980s for devices containing ^{10}B in borophosphosilicate glass (BPSG) layers. Foundries stopped using BPSG from the 180-nm technological node and below; nevertheless, thermal neutron-induced SEUs have continued to be reported for modern technologies. Boron doping in p-type silicon,

using diborane (B_2H_6) and boron trifluoride (BFl_3) in interconnect processing has been recognized as another source of ^{10}B contributing to thermal neutron-induced SEEs. The ^{10}B can increase SEE susceptibility because it has an unusually high nuclear cross-section of 3845 barns (where 1 barn = 10^{-24} cm^2 for thermal neutrons), while thermal neutron cross-sections with ^{11}B and Si are only 5.3 and 2.2 barns, respectively. The isotopic abundance of natural boron is 20% ^{10}B and 80% ^{11}B. The risk of introducing ^{10}B is the high cross-section for ^{10}B thermal neutron capture and subsequent production of secondary particles that can cause SEEs. The ^{10}B cross-section for thermal neutrons is dominated by the (n,α) reaction inducing emission of an alpha particle and a Lithium-ion with energies of 1.47 MeV and 0.84 MeV, respectively.

Simulations of the impact of the thermal neutrons in the 28-nm bulk technology were performed using MUSCA-SEP3 [Hub+09b]. For this purpose, the (n_{th},α) nuclear reaction was simulated, whose energetic and angular properties have been described previously. Firstly, p-type sources and drains were supposed to contain a boron concentration of 10^{20} cm^{-3}. Secondly, the wells were characterized by a boron concentration of 10^{19} cm^{-3} and the tungsten plug (defined as a layer), by a concentration of 10^{16} cm^{-3}. A 12 $\times$ 12 SRAM array was considered for each simulation, and incident neutrons were uniformly distributed across the surface and the direction considered. The elementary SRAM cell surface was supposed to be equal to 0.135 μm^2 (i.e. 0.57 μm $\times$ 0.24 μm). SBU and MCU-type event analyses can be extracted from simulations.

Figure 5.39 presents the 2 and 3-bit MCU cross-sections of the front, 90°, and 45° incident angles with respect to the chip surface. Results cannot be compared quantitatively with the experimental results because the SRAM cell description and the critical charge are based on assumptions. Nevertheless, trends are very close to experimental results. The highest MCU sensitivity was obtained at 45° and the front direction, while the lowest was for 90°.

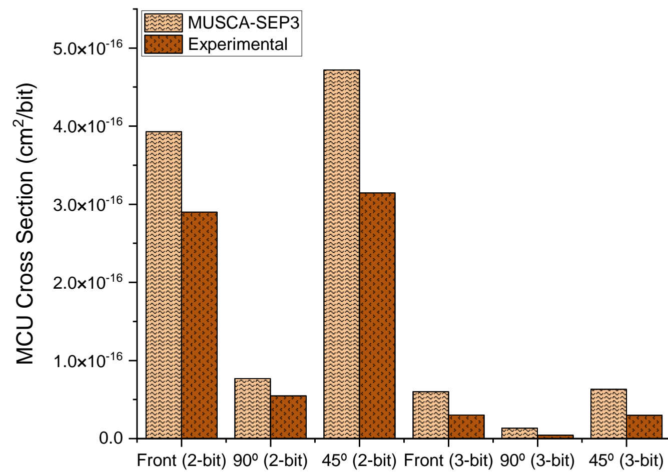

Figure 5.39: *Comparison of 2 and 3-bit MCU cross-sections issued from MUSCA-SEP3 vs. experimental results for different incidence angles under thermal neutrons on the Artix-7 XC7A100T FPGA.*

5.6.7 Artix-7 XC7A100T FPGA: Comparison between thermal and 14.2-MeV neutrons

A comparison between the radiation effects observed on the CRAM of the Artix-7 XC7A100T FPGA under thermal and 14.2-MeV neutrons was made. At first, only normal incidence and front direction of the neutron beam were considered in this comparison. Figure 5.40 compares the cross-sections for both types of neutrons according to the multiplicity of the events. It can be noted that thermal neutrons yielded MCUs with higher multiplicities than fast 14.2-MeV ones. On the other hand, it can be seen that 14.2-MeV neutrons provoke events more easily than thermal ones, especially for multiplicities ranging from 1 to 3. For larger multiplicities, the cross-section values are very similar for both irradiation sources.

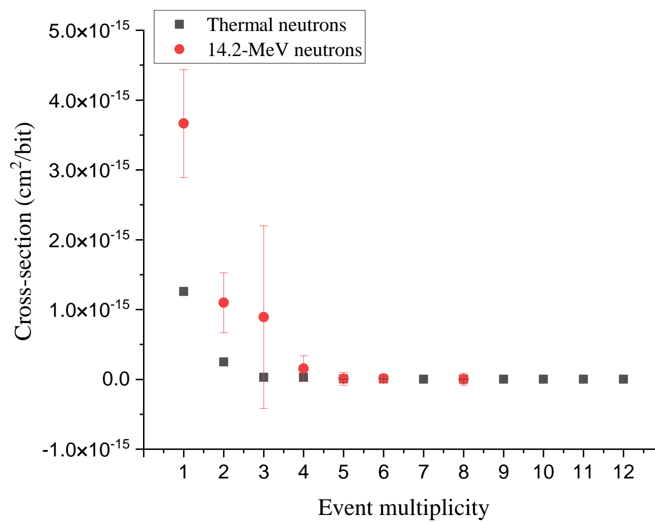

Figure 5.40: *Comparison of cross-sections of thermal neutrons and 14.2-MeV neutrons according to the multiplicity of the events observed in the Xilinx Artix-7 XC7A100T FPGA.*

Comparative results also show a considerable difference in FF cross-sections for both irradiation sources. These were 2.12×10^{-13} (cm^2/bit) and 6.75×10^{-15} (cm^2/bit), for thermal neutrons and 14.2-MeV ones, respectively.

Chapter 6

Conclusions and future work

This chapter is devoted to summarizing obtained results in this Ph.D. thesis and hints for future work.

6.1 Summary of the thesis

This Ph.D. thesis has presented the main findings of a five-year investigation into the SEE sensitivity of the following COTS devices: CY14V101QS and CY15B101J nv-SRAMs (working with SPI and I^2C protocols, respectively), a 28-nm bulk Artix-7 XC7A100T Xilinx FPGA, CY15B102Q and CY15B104Q FRAMs, MR10Q010CSC and MR25H40CDF MRAMs (working with Quad SPI and SPI protocols, respectively), and MB85AS4MT and MB85AS8MT ReRAMs under 1-MeV and 15.3-MeV protons, thermal and 14.8/14.2-MeV neutrons. Also, the influence of incident angle has been studied for CY14V101QS and the Artix-7 Xilinx FPGA under 14.2/14.8-MeV neutrons and thermal neutrons, respectively.

First, the SEU sensitivity of the CY14V101QS nv-SRAM was studied when it was hit by 14.2-MeV neutrons. It was irradiated with two different beam incident angles (normal and grazing), and two directions were tested for each; including horizontal (H) and vertical (V) for grazing angles, and the front and back of the memory for normal incidence. SBU sensitivity increased at grazing angles. It was notable that the irradiation from the back induced fewer errors than from the front. The observed MCUs showed a similar trend to SBU cross-sections, with fewer occurrences of bitflips. Then, the predictive platform MUSCA-SEP3 was used to predict cross-sections taking angular effects into account. The simulations were cross-checked with experimental results, showing good concordance between them. Furthermore, this tool was used to provide more insight into the physical reasons that explain this phenomenon, namely the directions and penetration range of secondary ions produced in the nuclear reactions and the asymmetry of the metallization/passivation layers of the device concerning its active silicon.

In a subsequent radiation-ground campaign, the same memory was irradiated under 15.3-MeV

protons. The results indicated the pattern written on the memory (0xFF, 0x55, 0xAA, and 0xFF) had little impact on the device's SEE sensitivity. No MCUs and MBUs were seen. This device was also tested under thermal neutrons in static and dynamic tests in another campaign. It was found that SEEs were more likely to occur in the latter type of tests. Finally, a comparison was carried out between the experimental results taken under 14.2-MeV neutrons, 15.3-MeV protons, and thermal neutrons. A difference of one order of magnitude was found between 14.2-MeV neutrons and other particles' SBU cross-sections (protons and thermal neutrons). Several reasons can explain why proton and neutron cross-sections have almost one order of magnitude in difference with similar energies. On the one hand, is a higher cross-section for inelastic neutron reactions in silicon than for proton ones. Also, more energy is deposited in inelastic neutron events compared to proton ones. Another reason points out a lower energy threshold exists in neutron SEUs than in proton ones [HG17; Rez+20].

In following campaigns, another nv-SRAM (the CY15B101J) was exposed to 14.8-MeV and thermal neutrons, and 15.3-MeV protons. This memory was more sensitive when carrying out dynamic experiments under protons. A bitflip in the non-volatile layer of the memory was also detected after receiving a total fluence of 87.00×10^{11} p/cm^2. In other experiments, the sensitivity was the highest during the static tests at patterns 0x00, 0xFF, and 0xAA than in the dynamic modes against thermal neutrons. Three static campaigns and two dynamic tests were conducted under 14.8-MeV neutrons. The highest SBU cross-section was observed at 0x00 pattern among static and dynamic tests. Comparing the results obtained by 14.8-MeV and thermal neutrons, and 15.3-MeV protons, it was noticed that the SEE sensitivity of this memory was one order of magnitude higher under neutrons than under protons, which again can be explained by the existence of a lower energy threshold in neutrons than in the proton ones. Also, inelastic neutron events deposit more energy than proton ones. Finally, a comparison was done between both nv-SRAMs. It was observed that the I^{2}C protocol is more susceptible to the SPI one under 15.3-MeV protons and 14.2/8-MeV neutrons. No MCUs / MBUs were observed on this memory under any of these radiation sources.

Next, the SEE sensitivity of a set of COTS emerging non-volatile memories, including FRAMs, MRAMs, and ReRAMs, were studied under different particles. First, FRAMs were tested in all facilities, where "unstable" SEEs, SBUs, "errors-in-row", stuck-at-errors, SEFIs, and hard errors were reported. This classification was possible thanks to the support of Infineon Technologies, who provided a tool to place the affected addresses in the XY plane of the memory. 12 rounds on the CY15B102Q FRAM were done against 15.3-MeV protons. Rounds from 5 to 20 minutes were carried out in static mode and one 31-minute round in dynamic mode, at fluxes ranging from 0.24×10^9 to 8.9×10^9 p/s/cm^2. Five more rounds were carried out on

the CY15B104Q FRAM. This time, fluxes ranged from 0.22×10^9 to 0.51×10^9 p/s/cm^2 with exposure times varying from 20 to 30 minutes. A wide variety of types of SEEs were observed on both FRAMs in these rounds, including unstable SBUs, SBUs, destructive SEEs, SEFIs, and unstable errors-in-row. Both FRAMs were also irradiated against 1-MeV protons. 25 rounds were performed throughout the campaign, including static and dynamic modes. In this case, only destructive SEEs and SEFIs were observed. 13 rounds were also performed under thermal neutrons on these two FRAMs. No errors were observed in static modes, but for the dynamic ones, a few isolated SBUs appeared in the the CY15B104Q. Finally, 6 rounds (3 static tests and 3 dynamic ones) were performed on the FRAMs under 14.8-MeV neutrons. A few SBUs and errors-in-raw were observed in the CY15B102Q this time. It can be concluded that both memories were more sensitive under 1-MeV protons than against thermal and 14.8-MeV neutrons.

Regarding ReRAMs, the MB85AS4MT ReRAM was examined against low-energy protons. Two permanent stuck-at-0's and a destructive SEE occurred. In another campaign, both the MB85AS4MT and MB85AS8MT were exposed to fluxes of 2.1×10^9 or 2.4×10^9 n/cm$^2/s$ under thermal neutrons. The results showed many SEFIs involving communication loss with the memory were observed for the static tests on the MB85AS4MT. Also, a recoverable stuck-at-0 was observed. In all dynamic tests, SEFIs were observed on that memory, too. Furthermore, 15 rounds of irradiation were carried out for the MB85AS8MT ReRAM under thermal neutrons. Contrarily to the tests carried out on MB85AS4MT, the MB85AS8MT showed total immunity against thermal neutrons. However, SEFIs were observed in the 4 dynamic tests made on the MB85AS8MT. Both ReRAMs were also examined under 14.8-MeV neutrons. Similarly, as with thermal neutrons, no errors were detected in any of these memories in the static tests, but for 2 out of the 3 dynamic ones, SEFIs occurred in both memories. Comparing the results for both ReRAMs showed the MB85AS8MT was more robust than the MB85AS4MT when working in static mode.

Regarding MRAMs, 9 and 7 rounds of irradiation were carried out on the MR25H40CDF and MR10Q010CSC, respectively, under thermal neutrons. Only SEFIs were observed in dynamic tests for the MR10Q010CSC. 3 more tests (1 static + 2 dynamic ones) were done on both MRAMs under 14.8-MeV neutrons. All these rounds yielded no errors. Thus, in general, MRAMs proved very resilient against thermal and 14.8-MeV neutrons. These results (in line with previous studies in the literature for similar devices [Nun+07; Ing+19; Haf+12; OBr+13; Hei14; Zha+14; Tsi+13]) indicate that, although memory cells in these emerging memories are remarkably robust against radiation effects, observed vulnerabilities in peripheral circuits indicate a potential critical weakness that should be considered, especially in spatial applications.

In the last part of this Ph.D. thesis, the investigations on the Xilinx Artix-7 XC7A100T FPGA manufactured in bulk 28-nm have been presented under 14.2-MeV and thermal neutrons. Regarding 14.2-MeV neutrons, most errors were observed on the FPGA's CRAM and rarely in its FFs. For the CRAM, SBUs and MCUs with different multiplicities were observed, and the shapes for 3-bit to 8-bit MCUs were also analyzed. The SBU cross-sections for FFs were higher than the CRAM ones. Furthermore, MUSCA-SEP3 was used to predict this device's sensitivity taking as reference a generic 28-nm bulk CMOS technology for the simulations, which matched the predicted ones accurately.

The Artix-7 XC7A100T was also irradiated under thermal neutrons with 6 incident angles: normal front and back incidences, grazing angles in two directions (East-West (EW) and North-South (NS)), 45°, and 135°. In these experiments, most bitflips emerged in the CRAM and a few in the FFs. In this experiment, it was also interesting to note that MBUs were detected, whose occurrence was studied depending on the incident angle of the neutron beam. The sensitivity of FFs was higher than that of the CRAM cells, albeit they were in the same order of magnitude. The sensitivity of this device against MCUs with different multiplicities was not only discussed, but also compared with simulations issued by MUSCA-SEP3. Trends were very close to experimental results. The highest MCU sensitivity was obtained at 45° + front direction, whereas the lowest one was for 90°. Also, the results indicate that the highest MBU cross-sections occurred at 135° and the front direction, and the lowest ones, for 90°. Shapes of 2-bit to 12-bit, 128-bit, and 384-bit MCUs observed on this device were also reported and discussed.

Finally, the radiation effects observed on this FPGA under thermal and 14.2-MeV neutrons were compared. It was detected that thermal neutrons provoked MCUs with higher multiplicities than 14.2-MeV ones. The reasons behind this difference were also studied in detail through MUSCA-SEP3 simulations.

6.2 Future work

The semiconductor industry is involved in many applications, including space and avionics, and is engaged in research and development. Accordingly, the arrival of new components in the market occurs quickly. A part of our future studies will consist in testing new emerging memories, including parallel FRAMs, DRAMs, HyperRAM, and Hyperflash memories.

Whereas this thesis focuses on SEU effects on COTS emerging memories and FPGAs, other destructive failures, such as SEBs and SEGRs, are also highly relevant for radiation hardness assurance. Therefore, studying such events, notably through experimentation and simulations, is also relevant to the Community. It would be interesting to study the results with more particles

(heavy ions), extended energy ranges, and using laser beam. Furthermore, another interesting line of future work will be to study the SEE sensitivity of said memories against alpha particles and muons and/or under different environmental conditions, such as ultra-low temperatures.

Chapter 7

List of publications

7.1 Journals

1. J. C. Fabero, **G. Korkian**, F. J. Franco, G. Hubert, H. Mecha, M. Letiche, and J. A. Clemente, “SEE sensitivity of a COTS 28-nm SRAM-based FPGA under thermal neutrons and different incident angles,” Microprocessors and Microsystems, vol. 96, 2022.

2. **G. Korkian**, D. León, F. J. Franco, J. C. Fabero, M. Letiche, Y. Morilla, P. Martín-Holgado, H. Puchner, H. Mecha, and J. A. Clemente, “Single event upsets under proton, thermal, and fast neutron irradiation in emerging nonvolatile memories,” IEEE Access, vol. 10, pp. 114566–114585, 2022.

3. **G. Korkian**, J. C. Fabero, G. Hubert, M. Rezaei, H. Mecha, F. J. Franco, H. Puchner, and J. A. Clemente, “Experimental and analytical study of the responses of nanoscale devices to neutrons impinging at various incident angles,” IEEE Transactions on Nuclear Science, vol. 67, no. 11, pp. 2345–2352, 2020.

4. J. C. Fabero, H. Mecha, F. J. Franco, J. A. Clemente, **G. Korkian**, S. Rey, B. Cheymol, M. Baylac, G. Hubert, R. Velazco, “Single Event Upsets Under 14-MeV Neutrons in a 28-nm SRAM-Based FPGA in Static Mode,” IEEE Transactions on Nuclear Science, vol. 67, no. 7, pp. 1461–1469, 2020.

5. F. J. Franco, J. A. Clemente, **G. Korkian**, J. C. Fabero, H. Mecha and R. Velazco, “Inherent Uncertainty in the Determination of Multiple Event Cross Sections in Radiation Tests,” in IEEE Transactions on Nuclear Science, vol. 67, no. 7, pp. 1547-1554, July 2020.

7.2 Conferences

1. J. C. Fabero, **G. Korkian**, F. J. Franco, H. Mecha, M. Letiche, and J. A. Clemente, “Thermal Neutron-induced SEUs on a COTS 28-nm SRAM-based FPGA under Different Incident Angles,” in 2021 IEEE 22nd Latin American Test Symposium (LATS), pp. 1–6, 2021.

2. F. J. Franco, J. A. Clemente, **G. Korkian**, J. C. Fabero, H. Mecha and R. Velazco, “Inherent Uncertainty in the Determination of Multiple Event Cross Sections in Radiation Tests,” in RADiations Effects on Components and Systems (RADECS) conference, 2019.

Bibliography

[Abd18] A. M. Abdelwahed. "Addressing the RRAM Reliability and Radiation Soft-Errors in the Memory Systems". Theses. University of Waterloo, (2018). URL: https://uwspace.uwaterloo.ca/handle/10012/13085.

[Abe+19] S. Abe et al. "Impact of Irradiation Side on Neutron-Induced Single-Event Upsets in 65-nm Bulk SRAMs". In: *IEEE Transactions on Nuclear Science* 66.7 (2019), pp. 1374–1380.

[Ada+81] Jr. Adams et al. *"Cosmic Ray Effects on Microelectronics. Part 1. The Near-Earth Particle Environment"*. Tech. rep. Naval Research Lab Washington DC, (1981).

[ADS16] D. Apalkov, B. Dieny, and J. M. Slaughter. "Magnetoresistive Random Access Memory". In: *Proceedings of the IEEE* 104 (Aug. 2016), pp. 1796–1830.

[Agg+19] S. Aggarwal et al. "Demonstration of a Reliable 1 Gb Standalone Spin-Transfer Torque MRAM for Industrial Applications". In: *2019 IEEE International Electron Devices Meeting (IEDM)*. IEEE. (2019), pp. 2–1.

[Ala+17] M. Alayan et al. "Experimental and Simulation Studies of the Effects of Heavy-Ion Irradiation on HfO 2-based RRAM Cells". In: *IEEE Transactions on Nuclear Science* 64.8 (2017), pp. 2038–2045.

[Art+11] L. Artola et al. "In Flight SEU/MCU Sensitivity of Commercial Nanometric SRAMs: Operational Estimations". In: *IEEE Transactions on Nuclear Science* 58.6 (2011), pp. 2644–2651.

[ASP04] J. M. Armani, G. Simon, and P. Poirot. "Low-energy neutron sensitivity of recent generation SRAMs". In: *IEEE Transactions on Nuclear Science* 51.5 (2004), pp. 2811–2816.

[Aus+17] R. A. Austin et al. "RadFxSat: A Flight Campaign for Recording Single-Event Effects in Commercial Off-the-Shelf Microelectronics". In: *2017 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*. (2017), pp. 1–5.

[Aut+14] J. L. Autran et al. "Real-Time Soft-Error Rate Measurements: A review". In: *Microelectronics Reliability* 54.8 (Aug. 2014), pp. 1455–1476.

[Aye03] J. E. Ayers. *"Digital Integrated Circuits: Analysis and Design"*. Taylor & Francis, (2003). ISBN: 9780203486900. URL: https://books.google.es/books?id=QHtalNXHKbsC.

[Bas11] Basic Health Physics. *"Interaction of Photons With Matter"*. Online. Available at https://www.nrc.gov/docs/ML1122/ML11229A667.pdf. (2011).

[Bau05] R.C. Baumann. "Radiation-Induced Soft Errors in Advanced Semiconductor Technologies". In: *IEEE Transactions on Device and Materials Reliability* 5.3 (2005), pp. 305–316.

[BDC99] J. M. Benedetto, G. F. Derbenwick, and J. D. Cuchiaro. “Single Event Upset Immunity of Strontium Bismuth Tantalate Ferroelectric Memories”. In: *IEEE Transactions on Nuclear Science* 46.6 (1999), pp. 1421–1426.

[Bea+15] J. Beaucour et al. “Grenoble Large Scale Facilities for Advanced Characterisation of Microelectronics Devices”. In: *2015 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS).* (2015), pp. 1–4.

[Ben+14] W. G. Bennett et al. “Single-and Multiple-Event Induced Upsets in 1T1R RRAM”. In: *IEEE Transactions on Nuclear Science* 61.4 (2014), pp. 1717–1725.

[Bes93] D. Bessot. “Conception de deux points mémoire statiques CMOS durcis contre l’effet des aléas logiques provoqués par l’environnement radiatif spatial”. Thèse de doctorat dirigée par Velazco, Raoul Microélectronique Grenoble INPG 1993. PhD thesis. (1993), 1 vol. (249 f.) URL: http://www.theses.fr/1993INPG0161.

[Bi+13] J. S. Bi et al. “The Impact of X-Ray and Proton Irradiation on -Based Bipolar Resistive Memories”. In: *IEEE Transactions on Nuclear Science* 60.6 (2013), pp. 4540–4546.

[Bi+19] J. S. Bi et al. “Total Ionization Dose and Single Event Effects of a Commercial Stand-alone 4 Mb Resistive Random Access Memory (ReRAM)”. In: *Microelectronics Reliability* 100 (2019), p. 113443.

[Bol13] R. Bolinder. *“Atmospheric Radiation Effects Study on Avionics: An Analysis of NFF Errors”*. 2013.

[Bos+15] A. L. Bosser et al. “Investigation on MCU Clustering Methodologies for Cross-section Estimation of RAMs”. In: *IEEE Transactions on Nuclear Science* 62.6 (2015), pp. 2620–2626.

[Bos+16] A. L. Bosser et al. “Methodologies for the Statistical Analysis of Memory Response to Radiation”. In: *IEEE Transactions on Nuclear Science* 63.4 (2016), pp. 2122–2128.

[Bos17] A. L. Bosser. “Single-Event Effects from Space and Atmospheric Radiation in Memory Components”. PhD thesis. University of Jyväskylä, (2017).

[Bru+14] G. Bruni et al. “Power Dissipation Effects on 28nm FPGA-based System on Chips Neutron Sensitivity”. In: *2014 22nd International Conference on Very Large Scale Integration (VLSI-SoC).* (2014), pp. 1–6.

[BS00] R. C. Baumann and E. B. Smith. “Neutron-induced boron fission as a major source of soft errors in deep submicron SRAM devices”. In: *2000 IEEE International Reliability Physics Symposium Proceedings. 38th Annual (Cat. No.00CH37059).* (2000), pp. 152–157.

[Buc52] D. A. Buck. *“Ferroelectrics for Digital Information Storage and Switching”*. Tech. rep. Massachusetts Inst of tech Cambridge digital computer lab, (1952).

[Cha19] J. Chauhan. *“Nanomaterial”*. India: Educreation Publishing, (2019).

[Che+14] D. Chen et al. “Single-Event Effect Performance of a Commercial Embedded ReRAM”. In: *IEEE Transactions on Nuclear Science* 61.6 (2014), pp. 3088–3094.

[Chu+12] K. C. Chun et al. “A scaling roadmap and performance evaluation of in-plane and perpendicular MTJ based STT-MRAMs for high-density cache memory”. In: *IEEE journal of solid-state circuits* 48.2 (2012), pp. 598–610.

[Chu+16] R. D. H. Chu et al. “2. Interactions of Electrons and Photons with Matter”. In: *Journal of the International Commission on Radiation Units and Measurements* 8.2 (June 2016), pp. 11–16. ISSN: 1473-6691.

[Chu71] L. Chua. “Memristor-The Missing Circuit Element”. In: *IEEE Transactions on Circuit Theory* 18.5 (1971), pp. 507–519.

[Cle+16] J. A. Clemente et al. “Statistical Anomalies of Bitflips in SRAMs to Discriminate SBUs From MCUs”. In: *IEEE Transactions on Nuclear Science* 63.4 (2016), pp. 2087–2094.

[Cle+17] J. A. Clemente et al. “Sensitivity characterization of a COTS 90-nm SRAM at ultralow bias voltage”. In: *IEEE Transactions on Nuclear Science* 64.8 (2017), pp. 2188–2195.

[Cle+18] J. A. Clemente et al. “SEU Characterization of Three Successive Generations of COTS SRAMs at Ultralow Bias Voltage to 14.2-MeV Neutrons”. In: *IEEE Transactions on Nuclear Science* 65.8 (2018), pp. 1858–1865.

[CML94] YM. Coic, O. Musseau, and JL. Leray. “A study of radiation vulnerability of ferroelectric material and devices”. In: *IEEE Transactions on Nuclear Science* 41.3 (1994), pp. 495–502.

[Cra17] S. Craw. “Manhattan Distance”. In: *Encyclopedia of Machine Learning and Data Mining*. Ed. by Claude Sammut and Geoffrey I. Webb. Boston, MA: Springer US, (2017), pp. 790–791. ISBN: 978-1-4899-7687-1.

[Cyp15] Cypress. *“F-RAM Technology Brief”*. Online. Available at `http://www.cypress.com/`. Revision A. Apr. (2015).

[Dai+17] K. Daisuke et al. “Soft Errors in 10-nm-scale Magnetic Tunnel Junctions Exposed to High-energy Heavy-ion Radiation”. In: *Japanese Journal of Applied Physics* 56.8 (June 2017), 0802B4.

[DAl16] J. S. D’Aleo. “Solar changes and the climate”. In: *“Evidence-based Climate Science”*. Elsevier, (2016), pp. 263–282.

[Dil+04] L. Dilillo et al. “Dynamic Read Destructive Faults in Embedded-SRAMs: Analysis and March Test Solution”. In: *ETS: European Test Symposium*. (2004), pp. 140–145.

[DM03] P. E. Dodd and L. W. Massengill. “Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics”. In: *IEEE Transactions on Nuclear Science* 50.3 (2003), pp. 583–602.

[Dod+15] N. A. Dodds et al. “The Contribution of Low-Energy Protons to the Total On-Orbit SEU Rate”. In: *IEEE Transactions on Nuclear Science* 62.6 (2015), pp. 2440–2451.

[Du+19] B. Du et al. “Ultrahigh Energy Heavy Ion Test Beam on Xilinx Kintex-7 SRAM-Based FPGA”. In: *IEEE Transactions on Nuclear Science* 66.7 (2019), pp. 1813–1819.

[Dur+03] M. Durlam et al. “A 0.18/spl mu/m 4Mb toggling MRAM”. In: *IEEE International Electron Devices Meeting 2003*. IEEE. (2003), pp. 34–6.

[EDN04] R. Edwards, C. Dyer, and E. Normand. “Technical Standard for Atmospheric Radiation Single Event Effects, (SEE) on Avionics Electronics”. In: *2004 IEEE Radiation Effects Data Workshop (IEEE Cat. No.04TH8774)*. (2004), pp. 1–5.

[Eng+05] B. N. Engel et al. "A 4-Mb toggle MRAM based on a novel bit and switching method". In: *IEEE Transactions on Magnetics* 41.1 (2005), pp. 132–136.

[ESA10] ESA-ESTEC. *"Space Engineering, Calculation of Radiation and Its Effects and Margin Policy Handbook"*. Noordwijk, Netherlands: ESA, (2010).

[ESA11] ESA-ESTEC. *"Space Engineering, Product Assurance, Techniques for Radiation Effects Mitigation in ASICs and FPGAs"*. Noordwijk, Netherlands: ESA, (2011).

[ESA14] ESA-ESTEC. *"Single Event Effects Test Method and Guidelines"*. ESCC Basic Specification No. 25100, (2014).

[Esp+04] M. C. Espirito-Santo et al. "Applications of GEANT4 in astroparticle experiments". In: *IEEE Transactions on Nuclear Science* 51.4 (2004), pp. 1373–1377.

[Eve16a] Everspin. *"Everspin Quad SPI MRAM Evaluation Board User Guide, MR10Q010-EVAL1"*. Online. Available at `https://www.everspin.com/file/157384/download`. Revision 1.0. Feb. (2016).

[Eve16b] Everspin. *"Everspin SPI MRAM Evaluation Board User Guide, MR25H00-EVAL"*. Online. Available at `https://www.everspin.com/file/574/download`. Revision 1.0. Feb. (2016).

[Eve18] Everspin. *"1Mb, High Speed Quad SPI MRAM Datasheet"*. Online. Available at `https://www.mouser.com/datasheet/2/144/MR10Q010_Datasheet-1218962.pdf`. Revision 5.6. June (2018).

[Eve20] Everspin. *"4Mb, SPI Serial Interface Memory Data Sheet"*. Online. Available at `https://www.everspin.com/getdatasheet/MR20H40`. Revision 12.6. Aug. (2020).

[Fab+20] J. C. Fabero et al. "Single Event Upsets Under 14-MeV Neutrons in a 28-nm SRAM-Based FPGA in Static Mode". In: *IEEE Transactions on Nuclear Science* 67.7 (2020), pp. 1461–1469.

[Fab+21] J. C. Fabero et al. "Thermal Neutron-induced SEUs on a COTS 28-nm SRAM-based FPGA under Different Incident Angles". In: *2021 IEEE 22nd Latin American Test Symposium (LATS)*. (2021), pp. 1–6.

[Fab+22] J. C. Fabero et al. "SEE Sensitivity of a COTS 28-nm SRAM-based FPGA under Thermal Neutrons and Different Incident Angles". In: *Microprocessors and Microsystems* (2022), p. 104743. ISSN: 0141-9331.

[Fan+14] R. Fang et al. "Total Ionizing Dose Effect of γ-ray Radiation on the Switching Characteristics and Filament Stability of HfOx Resistive Random Access Memory". In: *Applied Physics Letters* 104.18 (2014), p. 183507.

[FLC07] T. Z. Fullem, L. P. Lehman, and E. J. Cotts. "Examination of the utility of commercial-off-the-shelf memory devices as X-ray detectors". In: *2007 IEEE Nuclear Science Symposium Conference Record*. Vol. 2. (2007), pp. 1325–1328.

[FP07] D. Falguere and S. Petit. "A Statistical Method to Extract MBU Without Scrambling Information". In: *IEEE Transactions on Nuclear Science* 54.4 (2007), pp. 920–923.

[Fra+17] F. J. Franco et al. "Statistical Deviations From the Theoretical Only-SBU Model to Estimate MCU Rates in SRAMs". In: *IEEE Transactions on Nuclear Science* 64.8 (2017), pp. 2152–2160.

[Fra+19] F. J. Franco et al. “Influence of Randomness During the Interpretation of Results From Single-Event Experiments on SRAMs”. In: *IEEE Transactions on Device and Materials Reliability* 19.1 (2019), pp. 104–111.

[Fra+20] F. J. Franco et al. “Inherent Uncertainty in the Determination of Multiple Event Cross Sections in Radiation Tests”. In: *IEEE Transactions on Nuclear Science* 67.7 (2020), pp. 1547–1554.

[GA15] H. Guillaume and C. Adrien. “Radiation Effects Investigations Based on Atmospheric Radiation Model (ATMORAD) Considering GEANT4 Simulations of Extensive Air Showers and Solar Modulation Potential”. In: *Radiation Research* 184.1 (2015), pp. 83–94.

[Gad+12] M. J. Gadlage et al. “Impact of Neutron-Induced Displacement Damage on the Multiple Bit Upset Sensitivity of a Bulk CMOS SRAM”. In: *IEEE Transactions on Nuclear Science* 59.6 (2012), pp. 2722–2728.

[Gad+15] M. J. Gadlage et al. “Electron-Induced Single-Event Upsets in 45-nm and 28-nm Bulk CMOS SRAM-Based FPGAs Operating at Nominal Voltage”. In: *IEEE Transactions on Nuclear Science* 62.6 (2015), pp. 2717–2724.

[Gad+17] M. J. Gadlage et al. “Soft Errors Induced by High-Energy Electrons”. In: *IEEE Transactions on Device and Materials Reliability* 17.1 (2017), pp. 157–162.

[GBK17] Y. Gonzalez-Velo, H. J Barnaby, and M. N. Kozicki. “Review of Radiation Effects on ReRAM Devices and Technology”. In: *Semiconductor Science and Technology* 32.8 (2017), p. 083002.

[Geo+03] J. George et al. “SEE sensitivity trends in non-hardened high density SRAMs with sub-micron feature sizes”. In: *2003 IEEE Radiation Effects Data Workshop.* (2003), pp. 83–88.

[GGO03] T. Granlund, B. Granbom, and N. Olsson. “Soft error rate increase for new generations of SRAMs”. In: *IEEE Transactions on Nuclear Science* 50.6 (2003), pp. 2065–2068.

[GP10] S. Gerardin and A. Paccagnella. “Present and Future Non-Volatile Memories for Space”. In: *IEEE Transactions on Nuclear Science* 57.6 (2010), pp. 3016–3039.

[Gra11] T. Granlund. “Guideline for designing and integration of Avionics concerning atmospheric radiation”. In: *Saab report no. LC-09* (2011), pp. 0026–04.

[Grd15] S. Grdanovska. “Characterization of Radiation Damage to a Novel Photonic Crystal Sensor”. PhD thesis. University of Maryland, (2015).

[Grü+86] P. Grünberg et al. “Layered magnetic structures: Evidence for antiferromagnetic coupling of Fe layers across Cr interlayers”. In: *Physical review letters* 57.19 (1986), p. 2442.

[Gup+15] V. Gupta et al. “Heavy-Ion Radiation Impact on a 4Mb FRAM under Different Test Conditions”. In: *2015 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS).* (2015), pp. 1–3.

[HA93] A. Holmes-Siedle and L. Adams. “Handbook of radiation effects”. In: (1993).

[Haf+12] C. Hafer et al. “SEU, SET, and SEFI Test Results of a Hardened 16Mbit MRAM Device”. In: *2012 IEEE Radiation Effects Data Workshop.* (2012), pp. 1–4.

[Han+11] A. Hands et al. "Single Event Effects in Power MOSFETs and SRAMs Due to 3 MeV, 14 MeV and Fission Neutrons". In: *IEEE Transactions on Nuclear Science* 58.3 (2011), pp. 952–959.

[Har+12] R. Harada et al. "Angular Dependency of Neutron-Induced Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM". In: *IEEE Transactions on Nuclear Science* 59.6 (2012), pp. 2791–2795.

[HAS10] J. Heidecker, G. Allen, and D. Sheldon. "Single Event Latchup (SEL) and Total Ionizing Dose (TID) of a 1 Mbit Magnetoresistive Random Access Memory (MRAM)". In: *2010 IEEE Radiation Effects Data Workshop.* (2010), pp. 4–4.

[Hau+18] A. Haungs et al. "The KASCADE Cosmic-ray Data Centre KCDC: Granting Open Access to Astroparticle Physics Research Data". In: *European Physical Journal C* 78.9 (Sept. 2018), p. 741.

[Haz+03] P. Hazucha et al. "Neutron soft error rate measurements in a 90-nm CMOS process and scaling trends in SRAM from 0.25-/spl mu/m to 90-nm generation". In: *IEEE International Electron Devices Meeting.* (2003), pp. 21.5.1–21.5.4.

[He+21] L. He et al. "Research on Single Event Effect Test of a RRAM Memory and Space Flight Demonstration". In: *Microelectronics Reliability* 126 (2021). Proceedings of ESREF 2021, 32nd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, p. 114347. ISSN: 0026-2714.

[Hei+08] D. F. Heidel et al. "Low Energy Proton Single-Event-Upset Test Results on 65 nm SOI SRAM". In: *IEEE Transactions on Nuclear Science* 55.6 (2008), pp. 3394–3400.

[Hei14] J. Heidecker. *"MRAM Technology Status".* (2014).

[HG17] J. Han and G. Guo. "Characteristics of Energy Deposition from 1-1000 MeV Proton and Neutron Induced Nuclear Reactions in Silicon". In: *AIP Advances* 7.11 (2017), p. 115220.

[HH07] D. Harris and S. Harris. *"Digital Design and Computer Architecture".* San Francisco, CA, USA: Morgan Kaufmann Publishers Inc., (2007). ISBN: 0123704979.

[Hir+15] S. Hirokawa et al. "Characterizing Alpha- and Neutron-Induced SEU and MCU on SOTB and Bulk 0.4-V SRAMs". In: *IEEE Transactions on Nuclear Science* 62.2 (2015), pp. 420–427.

[HJG17] A. Holst, J. Jang, and S. Ghosh. "Investigation of Magnetic Field Attacks on Commercial Magneto-Resistive Random Access Memory". In: *2017 18th International Symposium on Quality Electronic Design (ISQED).* (2017), pp. 155–160.

[Hon15] Honeywell. *"HXNV0100 1Megabit 64K x 16 Non-Volatile Magneto-Resistive RAM Datasheet".* Online. Available at `https://aerospace.honeywell.com/content/dam/aerobt/en/documents/learn/products/microelectronics/datasheet/HXVN0100-B-Datasheet.pdf`. Revision B. Mar. (2015).

[Hub+09a] G. Hubert et al. "Operational SER Calculations on the SAC-C Orbit Using the Multi-Scales Single Event Phenomena Predictive Platform (MUSCA SEP^3)". In: *IEEE Transactions on Nuclear Science* 56.6 (2009), pp. 3032–3042.

[Hub+09b] G. Hubert et al. "Operational SER Calculations on the SAC-C Orbit Using the Multi-Scales Single Event Phenomena Predictive Platform (MUSCA SEP^3)". In: *IEEE Transactions on Nuclear Science* 56.6 (2009), pp. 3032–3042.

[Hub+13] G. Hubert et al. "Continuous High-Altitude Measurements of Cosmic Ray Neutrons and SEU/MCU at Various Locations: Correlation and Analyses Based-On MUSCA SEP^3". In: *IEEE Transactions on Nuclear Science* 60.4 (2013), pp. 2418–2426.

[Hug+12] H. Hughes et al. "Radiation Studies of Spin-Transfer Torque Materials and Devices". In: *IEEE Transactions on Nuclear Science* 59.6 (2012), pp. 3027–3033.

[Hut+09] J. M. Hutson et al. "Evidence for Lateral Angle Effect on Single-Event Latchup in 65 nm SRAMs". In: *IEEE Transactions on Nuclear Science* 56.1 (2009), pp. 208–213.

[IF04] F. Irom and F. F. Farmanesh. "Frequency dependence of single-event upset in advanced commercial PowerPC microprocessors". In: *IEEE Transactions on Nuclear Science* 51.6 (2004), pp. 3505–3509.

[ik09] P. Bohá ik. *"MPC5121e Serial Peripheral Interface (SPI)"*. Online. Available at `https://www.nxp.com/docs/en/application-note/AN3904.pdf`. Revision 0. Aug. (2009).

[Ike+05] N. Ikeda et al. "Analysis of Angular Dependence of Proton-Induced Multiple-Bit Upsets in a Synchronous SRAM". In: *IEEE Transactions on Nuclear Science* 52.6 (2005), pp. 2200–2204.

[Ing+19] J. D. Ingalls et al. "Total Dose and Heavy Ion Radiation Response of 55 nm Avalanche Technology Spin Transfer Torque MRAM". In: *2019 IEEE Radiation Effects Data Workshop*. IEEE. (2019), pp. 1–4.

[ISO01] ISO. *"Reference Neutron Radiations: Characteristics and Methods of Production"*. ISO. International Standard ISO 8529-1, (2001).

[ISO02] ISO. *"Calibration Fundamentals of Radiation Protection Devices Related to the Basic Quantities Characterizing the Radiation Field"*. ISO. International Standard ISO 8529-2, (2002).

[ISO98] ISO. *"Reference Neutron Radiations: Calibration of Area and Personal Dosimeters and Determination of Their Response as a Function of Neutron Energy and Angle of Incidence"*. ISO. International Standard ISO 8529-3, (1998).

[J B99] J. Barth. *"The Radiation Environment"*. Online. Available at `https://radhome.gsfc.nasa.gov/radhome/papers/apl_922.pdf`. (1999).

[J C21] J. C. Fabero. *"OpenOCD modification for Virtex-5/Artix-7: GCAPTURE, GRESTORE and readback operations support"*. Online. Available at `http://cort.as/-PUFI`. (2021).

[Ji+19a] Q. Ji et al. "Effects of Total Ionizing Dose on Single Event Effect Sensitivity of FRAMs". In: *Microelectronics Reliability* 95 (2019), pp. 1–7.

[Ji+19b] Y. Ji et al. "Reliability of 8-Mbit Embedded-STT-MRAM in 28-nm FDSOI Technology". In: *IEEE International Reliability Physics Symposium (IRPS)*. (2019), pp. 1–3.

[Joh00] A. H. Johnston. "Scaling and Technology Issues for Soft Error Rates". In: (2000).

[Ju+22] A. Ju et al. "Failure Analysis of Commercial Ferroelectric Random Access Memory for Single Event Effect". In: *IEEE Transactions on Nuclear Science* (2022), pp. 1–1.

[Kas+14] F. L. Kastensmidt et al. "Voltage scaling and Aging Effects on Soft Error Rate in SRAM-based FPGAs". In: *Microelectronics Reliability* 54.9-10 (2014), pp. 2344–2348.

[Kat+18] R. R. Katti et al. “Heavy Ion Bit Response and Analysis of 256 Megabit Non-Volatile Spin-Torque-Transfer Magnetoresistive Random Access Memory (STT-MRAM)”. In: *2018 IEEE Radiation Effects Data Workshop (REDW)*. (2018), pp. 1–4.

[Kat+19] T. Kato et al. “Neutron-Induced Multiple-Cell Upsets in 20-nm Bulk SRAM: Angular Sensitivity and Impact of Multiwell Potential Perturbation”. In: *IEEE Transactions on Nuclear Science* 66.7 (2019), pp. 1381–1389.

[Ke+15] G. Ke et al. “Total Ionizing Dose Sensitivity of Function Blocks in FRAM”. In: *Microelectron. Reliab.* 55.6 (2015), pp. 873–878.

[Kor+20] G. Korkian et al. “Experimental and Analytical Study of the Responses of Nanoscale Devices to Neutrons Impinging at Various Incident Angles”. In: *IEEE Transactions on Nuclear Science* 67.11 (2020), pp. 2345–2352.

[Kor+22] G. Korkian et al. “Single Event Upsets Under Proton, Thermal, and Fast Neutron Irradiation in Emerging Nonvolatile Memories”. In: *IEEE Access* 10 (2022), pp. 114566–114585.

[Kru15] F. Krumeich. “Properties of Electrons, Their Interactions with Matter and Applications in Electron Microscopy”. In: (2015).

[LC04] S. Lin and D. J. Costello. *“Error Control Coding: Fundamentals and Applications”*. Upper Saddle River, NJ: Pearson/Prentice Hall, (2004). ISBN: 0130426725 9780130426727.

[Lee+15] D. S. Lee et al. “Addressing Angular Single-Event Effects in the Estimation of On-Orbit Error Rates”. In: *IEEE Transactions on Nuclear Science* 62.6 (2015), pp. 2563–2569.

[Lia+19] W. Liao et al. “Similarity Analysis on Neutron- and Negative Muon-Induced MCUs in 65-nm Bulk SRAM”. In: *IEEE Transactions on Nuclear Science* 66.7 (2019), pp. 1390–1397.

[Liu+18] T. Liu et al. “Heavy Ion Radiation Effects on a 130-nm COTS NVSRAM Under Different Measurement Conditions”. In: *IEEE Transactions on Nuclear Science* 65.5 (2018), pp. 1119–1126.

[Mae+21] M. Maestro-Izquierdo et al. “Gamma Radiation Effects on HfO2-based RRAM Devices”. In: *2021 13th Spanish Conference on Electron Devices (CDE)*. (2021), pp. 23–26.

[Mal+17] D. Malagón et al. “Soft error Rate Comparison of 6T and 8T SRAM ICs using Mono-Energetic Proton and Neutron Irradiation Sources”. In: *Microelectronics Reliability* 78 (2017), pp. 38–45. ISSN: 0026-2714.

[Mar+12] M. J. Marinella et al. “Initial Assessment of the Effects of Radiation on the Electrical Characteristics of TaO_x Memristive Memories”. In: *IEEE Transactions on Nuclear Science* 59.6 (2012), pp. 2987–2994.

[Mar13] M. J. Marinella. “The Future of Memory”. In: *2013 IEEE Aerospace Conference.* (2013), pp. 1–11.

[Mar21] M. J Marinella. “Radiation Effects in Advanced and Emerging Nonvolatile Memories”. In: *IEEE Transactions on Nuclear Science* 68.5 (2021), pp. 546–572.

[MB95] R. A. Moore and J. M. Benedetto. “Ionizing Radiation-Induced Asymmetries of the Retention Characteristics of Ferroelectric Thin Films”. In: *IEEE Transactions on Nuclear Science* 42.6 (1995), pp. 1575–1584.

[Mey76] W. E. Meyerhof. *“Elements of Nuclear Physics”*. New York: McGraw-Hill, 1976.

[Mik+01] T. Mikolajick et al. “FeRAM Technology for High Density Applications”. In: *Microelectronics Reliability* 41.7 (2001), pp. 947–950.

[Mon+20] E. A. Montoya et al. “Immunity of Nanoscale Magnetic Tunnel Junctions with Perpendicular Magnetic Anisotropy to Ionizing Radiation”. In: *Scientific reports* 10.1 (2020), pp. 1–8.

[Mor+18] Y. Morilla et al. “Progress of CNA to Become the Spanish Facility for Combined Irradiation Testing in Aerospace”. In: *2018 18th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*. (2018), pp. 1–5.

[MSR15] S. Mishra, N. K. Singh, and V Rousseau. *“System on chip interfaces for low power design”*. Morgan Kaufmann, (2015).

[Nai+19] V. B. Naik et al. “Manufacturable 22nm FD-SOI Embedded MRAM Technology for Industrial-grade MCU and IOT Applications”. In: *2019 IEEE International Electron Devices Meeting (IEDM)* (2019), pp. 2.3.1–2.3.4.

[Nat08] National Aeronautics and Space Administration (NASA). *“Space Faring: The Radiation Challenge”*. Online. Available at `https://www.nasa.gov/stem-ed-resources/sf-radiation-challenge-hs-mod1.html`. (2008).

[Nat16a] National Aeronautics and Space Administration (NASA). *“Gamma Rays”*. Online. Available at `https://science.nasa.gov/ems/12_gammarays`. (2016).

[Nat16b] National Aeronautics and Space Administration (NASA). *“Introduction to the Electromagnetic Spectrum”*. Online. Available at `https://science.nasa.gov/ems/01_intro`. (2016).

[Nat16c] National Aeronautics and Space Administration (NASA). *“X-Rays”*. Online. Available at `https://science.nasa.gov/ems/11_xrays`. (2016).

[NI07] D. N. Nguyen and F. Irom. “Radiation Effects on MRAM”. In: *2007 9th European Conference on Radiation and Its Effects on Components and Systems*. (2007), pp. 1–4.

[NJS15] A. Neale, M. Jonkman, and M. Sachdev. “Adjacent-MBU-Tolerant SEC-DED-TAEC-yAED Codes for Embedded SRAMs”. In: *IEEE Trans. Circuits Syst., II, Exp. Briefs* 62.4 (2015), pp. 387–391.

[NM18] Engineering National Academies of Sciences and Medicine. *“Testing at the Speed of Light: The State of U.S. Electronic Parts Space Radiation Testing Infrastructure”*. Washington, DC: The National Academies Press, (2018). ISBN: 978-0-309-47079-7. URL: `https://nap.nationalacademies.org/catalog/24993/testing-at-the-speed-of-light-the-state-of-us`.

[Nol18] S. Nolte. *“PTB Contribution to the Key Comparison CCRI(III)-K11 Comparison of Neutron Fluence Measurements for Neutron Energies of 27 keV, 565 keV, 2.5 MeV and 17 MeV”*. Ed. by Physikalisch-Technische Bundesanstalt. PTB-Bericht: N, Neutronenphysik. Fachverlag NW in der Carl Schünemann Verlag GmbH, (2018).

[Nun+07] T. Nuns et al. “Evaluation of Recent Technologies of Non-Volatile RAM”. In: *2007 9th European Conference on Radiation and Its Effects on Components and Systems*. (2007), pp. 1–8.

[OBr+08] M. V. O'Bryan et al. "Compendium of Recent Single Event Effects Results for Candidate Spacecraft Electronics for NASA". In: *IEEE Radiation Effects Data Workshop.* (2008), pp. 11–20.

[OBr+13] M. V. O'Bryan et al. "Compendium of Recent Single Event Effects for Candidate Spacecraft Electronics for NASA". In: *2013 IEEE Radiation Effects Data Workshop (REDW).* (2013), pp. 1–8.

[OBr+18] M. V. O'Bryan et al. "NASA Goddard Space Flight Center's Compendium of Recent Single Event Effects Results". In: *2018 IEEE Radiation Effects Data Workshop (REDW).* (2018), pp. 1–8.

[Ong77] R. N. Onge. "Energy Spectrum and Flux of Fast Neutrons in the Atmosphere". In: 16.3 (Aug. 1977).

[Ope22] Open On-Chip Debugger. *"Open On-Chip Debugger"*. Online. Available at `http://openocd.org/`. (2022).

[Pet11] E. Petersen. *"Single event effects in aerospace"*. John Wiley & Sons, (2011).

[Phi+12] H. S. Philips Wong et al. "Metal–Oxide RRAM". In: *Proceedings of the IEEE* 100.6 (2012), pp. 1951–1970.

[PN07] I. Pérez-Juste and O. Nieto Faza. "Interaction of Electrons with Matter". In: *Atoms, Radiation, and Radiation Protection*. John Wiley and Sons, Ltd, (2007). Chap. 6, pp. 139–158. ISBN: 978-3-5276-16978.

[Poi+03] C. Poivey et al. "Testing Guidelines for Single Event Transient (SET) Testing of Linear Devices". In: (2003).

[Pra16] R. Prakash. *"Nonvolatile SRAM (nvSRAM) Basics"*. Online. Available at `https://www.infineon.com/dgdl/Infineon-Nonvolatile_SRAM_(nvSRAM)_Basics-Whitepaper-v03_00-EN.pdf?fileId=8ac78c8c7d0d8da4017d0fb1d95b2600&da=t`. Revision B. Aug. (2016).

[Red+15] B. Reddell et al. "Single Event Effects Testing For Low Earth Orbit Missions with Neutrons". In: *2015 IEEE Nuclear & Space Radiation Effects Conference (NSREC 2015).* JSC-CN-32943. (2015).

[Red+17] B. D. Reddell et al. "Compendium of single event effects test results for commercial-off-the-shelf and standard electronics for low earth orbit and deep space applications". In: *2017 IEEE Radiation Effects Data Workshop (REDW).* IEEE. (2017), pp. 1–6.

[Ree08] R. Reed. *"Fundamental Mechanisms for Single Particle-Induced Soft Errors"*. 2008.

[Ren+12] F. Ren et al. "Radiation Tolerance of Magnetic Tunnel Junctions with MgO Tunnel Barriers". In: *IEEE Transactions on Nuclear Science* 59.6 (2012), pp. 3034–3038.

[Rez+18] N. Rezzak et al. "Neutron and Proton Characterization of Microsemi 28 nm PolarFire SONOS-Based FPGA". In: *2018 IEEE Radiation Effects Data Workshop (REDW).* (2018), pp. 1–5.

[Rez+20] M. R. Rezaei et al. "Evaluation of a COTS 65-nm SRAM under 15 MeV Protons and 14 MeV Neutrons at Low VDD". In: *IEEE Transactions on Nuclear Science* 67, no. 10.10 (2020), pp. 2188–2195.

[Rez+22] M. R. Rezaei et al. "Impact of Dynamic Voltage Scaling on SEU Sensitivity of COTS Bulk SRAMs and A-LPSRAMs Against Proton Radiation". In: *IEEE Transactions on Nuclear Science* 69.2 (2022), pp. 126–133.

[Rod20] K. P. Rodbell. “Low-Energy Protons—Where and Why “Rare Events” Matter”. In: *IEEE Transactions on Nuclear Science* 67.7 ((2020)), pp. 1204–1215.

[Sch+03] J. R. Schwank et al. “Radiation Effects in SOI Technologies”. In: *IEEE Transactions on Nuclear Science* 50.3 (2003), pp. 522–538.

[Sch05] D. Schlegel. *“TARGET User’s Manual”*. Physikalisch-Technische Bundesanstalt, (2005).

[Sem18] NXP Semiconductors. *“I^2C-bus specification and user manual”*. Online. Available at `https://www.nxp.com/docs/en/supporting-information/AN12207.pdf`. Revision 1.6. June (2018).

[Set+06] N. Setter et al. “Ferroelectric Thin Films: Review of Materials, Properties, and Applications”. In: *Journal of applied physics* 100.5 (2006), p. 051606.

[Sex03] F. W. Sexton. “Destructive Single-event Effects in Semiconductor Devices and ICs”. In: *IEEE Transactions on Nuclear Science* 50.3 (2003), pp. 603–621.

[SG+02] L. Scheick, S. Guertin, et al. “SEU Evaluation of FeRAM Memories for Space Applications”. In: (2002).

[She+10] X. She et al. “Single Event Transient Suppressor for Flip-Flops”. In: *IEEE Transactions on Nuclear Science* 57.4 (2010), pp. 2344–2348.

[Shi+14] H. Shin et al. “Interleaving Test Algorithm for Subthreshold Leakage-Current Defects in DRAM Considering the Equal Bit Line Stress”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 22.4 (2014), pp. 803–812.

[SL04] E. Stassinopoulos and K. LaBel. “The Near-Earth Space Radiation Environment for Electronics”. In: *Boletin Informativo Space Magazine* 6 (2004).

[SLF10] X. She, N. Li, and W. D. Farwell. “Tunable SEU-Tolerant Latch”. In: *IEEE Transactions on Nuclear Science* 57.6 ((2010)), pp. 3787–3794.

[SLJ12] X. She, N. Li, and D. W. Jensen. “SEU Tolerant Memory Using Error Correction Code”. In: *IEEE Transactions on Nuclear Science* 59.1 (2012), pp. 205–210.

[SLZ17] J. Shen, W. Li, and Y. Zhang. “Assessment of TID Effect of FRAM Memory Cell Under Electron, X-Ray, and Co- 60 γ Ray Radiation Sources”. In: *IEEE Transactions on Nuclear Science* 64.3 (2017), pp. 969–975.

[Sta17] JEDEC Standard. *“Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices”*. Online. Available at `https://www.jedec.org/standards-documents/docs/jesd-89a`. Revision JESD57. Nov. (2017).

[Str+08] D. B. Strukov et al. “The Missing Memristor Found”. In: *nature* 453.7191 (2008), pp. 80–83.

[SZ02] M. D. Stiles and A. Zangwill. “Anatomy of Spin-Transfer Torque”. In: *Physical Review B* 66.1 (2002), p. 014407.

[Tam+15] L. A. Tambara et al. “Heavy Ions Induced Single Event Upsets Testing of the 28 nm Xilinx Zynq-7000 All Programmable SoC”. In: *2015 IEEE Radiation Effects Data Workshop (REDW)*. (2015), pp. 1–6.

[Tau09] H. J. Tausch. “Simplified Birthday Statistics and Hamming EDAC”. In: *IEEE Transactions on Nuclear Science* 56.2 (2009), pp. 474–478.

[Tav10] S. Tavernier. *"Experimental Techniques in Nuclear and Particle Physics"*. Berlin, Heidelberg: Springer, (2010).

[Tec17] Infineon Technologies. *"1-Mbit (128K × 8) Quad SPI nvSRAM CY14V101QS"*. Online. Available at https://www.infineon.com/dgdl/Infineon-CY14V101QS_1-Mbit_(128K_8)_Quad_SPI_nvSRAM-DataSheet-v14_00-EN.pdf?fileId=8ac78c8c7d0d8da4017d0ed151594d8a. Revision M. May (2017).

[Tec18] Infineon Technologies. *"1-Mbit (128K × 8) Serial (I^2C) nvSRAM"*. Online. Available at https://www.infineon.com/dgdl/Infineon-CY14C101J_CY14B101J_CY14E101J_1_MBIT_(128K_X_8)_SERIAL_(I2C)_NVSRAM-DataSheet-v17_00-EN.pdf?fileId=8ac78c8c7d0d8da4017d0ebfc9013449. Revision P. Aug. (2018).

[Tip+06] A. D. Tipton et al. "Multiple-Bit Upset in 130 nm CMOS Technology". In: *IEEE Transactions on Nuclear Science* 53.6 (2006), pp. 3259–3264.

[Tip+08a] A. D. Tipton et al. "Device-Orientation Effects on Multiple-Bit Upset in 65 nm SRAMs". In: *IEEE Transactions on Nuclear Science* 55.6 (2008), pp. 2880–2885.

[Tip+08b] A. D. Tipton et al. "Increased Rate of Multiple-Bit Upset From Neutrons at Large Angles of Incidence". In: *IEEE Transactions on Device and Materials Reliability* 8.3 (2008), pp. 565–570.

[Ton+17] J. Tonfat et al. "Analyzing the Influence of the Angles of Incidence and Rotation on MBU Events Induced by Low LET Heavy Ions in a 28-nm SRAM-Based FPGA". In: *IEEE Transactions on Nuclear Science* 64.8 (2017), pp. 2161–2168.

[Tsi+13] G. Tsiligiannis et al. "Testing a Commercial MRAM Under Neutron and Alpha Radiation in Dynamic Mode". In: *IEEE Transactions on Nuclear Science* 60.4 (2013), pp. 2617–2622.

[Tsi+14a] G. Tsiligiannis et al. "Dynamic Test Methods for COTS SRAMs". In: *IEEE Transactions on Nuclear Science* 61.6 (2014), pp. 3095–3102.

[Tsi+14b] G. Tsiligiannis et al. "Multiple Cell Upset Classification in Commercial SRAMs". In: *IEEE Transactions on Nuclear Science* 61.4 (2014), pp. 1747–1754.

[Tsi+20] A. Tsigkanos et al. "High-Performance COTS FPGA SoC for Parallel Hyperspectral Image Compression with CCSDS-123.0-B-1". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 28.11 (2020), pp. 2397–2409.

[Tur07] J. E. Turner. "Interaction of Heavy Charged Particles with Matter". In: *Atoms, Radiation, and Radiation Protection*. John Wiley and Sons, Ltd, (2007). Chap. 5, pp. 109–137. ISBN: 9783527616978.

[Vel+14] R. Velazco et al. "Evidence of the Robustness of a COTS Soft-Error Free SRAM to Neutron Radiation". In: *IEEE Transactions on Nuclear Science* 61.6 (2014), pp. 3103–3108.

[Vér+03] A. Vértes et al. *"Handbook of nuclear chemistry"*. Vol. 4. Springer, (2003).

[Vil+14] F. Villa et al. "Accelerator-Based Neutron Irradiation of Integrated Circuits at GENEPI2 (France)". In: *2014 IEEE Radiation Effects Data Workshop (REDW)*. (2014), pp. 1–5.

[Vil+16] F. Villa et al. "Multipurpose Applications of the Accelerator based Neutron Source GENEPI2". In: *Nuovo Cimento C Geophysics Space Physics C* 38 (article no. 182, 2016).

[Vla+21] V. Vlagkoulis et al. “Single Event Effects Characterization of the Programmable Logic of Xilinx Zynq-7000 FPGA Using Very/Ultra High-Energy Heavy Ions”. In: *IEEE Transactions on Nuclear Science* 68.1 (2021), pp. 36–45.

[Von93] J. Von Neumann. “First Draft of a Report on the EDVAC”. In: *IEEE Annals of the History of Computing* 15.4 (1993), pp. 27–75.

[Wee+14] S. L. Weeden-Wright et al. “TID and Displacement Damage Resilience of 1T1R HfO_2/ Hf Resistive Memories”. In: *IEEE Transactions on Nuclear Science* 61.6 (2014), pp. 2972–2978.

[Wei+19] J. N. Wei et al. “Single Event Effects in Commercial FRAM and Mitigation Technique using Neutron-induced Displacement Damage”. In: *Microelectronics Reliability* 92 (2019), pp. 149–154. ISSN: 0026-2714.

[Weu+18] C. Weulersse et al. “Contribution of Thermal Neutrons to Soft Error Rate”. In: *IEEE Transactions on Nuclear Science* 65.8 (2018), pp. 1851–1857.

[Wir+14] M. J. Wirthlin et al. “A Method and Case Study on Identifying Physically Adjacent Multiple-Cell Upsets Using 28-nm, Interleaved and SECDED-Protected Arrays”. In: *IEEE Transactions on Nuclear Science* 61.6 (2014), pp. 3080–3087.

[WTH14] M. J. Wirthlin, H Takai, and A Harding. “Soft Error Rate Estimations of the Kintex-7 FPGA within the ATLAS Liquid Argon (LAr) Calorimeter”. In: *Journal of Instrumentation* 9.01 (Jan. 2014), pp. C01025–C01025.

[Xil18] Xilinx. *“UG470: 7 Series FPGAs Configuration User Guide”*. Revision 1.13. Mar. (2018).

[Yua13] X. Yuan. *“Emerging Memory Technologies: Design, Architecture, and Applications”*. Springer Publishing Company, Incorporated, (2013). ISBN: 1441995501.

[Zah+20] F. Zahoor et al. “Resistive Random Access Memory (RRAM): An Overview of Materials, Switching Mechanism, Performance, Multilevel cell (MLC) Storage, Modeling, and Applications”. In: 15.1 (2020), pp. 1–26.

[Zha+14] W. Zhao et al. “A Radiation Hardened Hybrid Spintronic/CMOS Nonvolatile Unit Using Magnetic Tunnel Junctions”. In: *Journal of Physics D: Applied Physics* 47.40 (2014), p. 405003.

[Zha+15] Zh. Zhang et al. “Single Event Effects in COTS Ferroelectric RAM Technologies”. In: *2015 IEEE Radiation Effects Data Workshop (REDW)*. (2015), pp. 1–5.

[Zha+19] P. X. Zhao et al. “Heavy Ion Irradiation Induced Hard Error in MTJ of the MRAM Memory array”. In: *Microelectronics Reliability* 100 (2019), p. 113347.

[Zha+21] P. X. Zhao et al. “Heavy-Ion-Induced Displacement Damage Effects in Magnetic Tunnel Junctions with Perpendicular Anisotropy”. In: *IEEE Transactions on Nuclear Science* 68.5 (2021), pp. 581–587.

[ZWC08] M. Zanata, N. Wrachien, and A. Cester. “Ionizing Radiation Effect on Ferroelectric Nonvolatile Memories and Its Dependence on the Irradiation Temperature”. In: *IEEE Transactions on Nuclear Science* 55.6 (2008), pp. 3237–3245.

[ZZB10] J. F. Ziegler, M. D. Ziegler, and J. P. Biersack. “SRIM – The Stopping and Range of Ions in Matter, 2010”. In: *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms* 268.11 (2010). 19th International Conference on Ion Beam Analysis, pp. 1818–1823. ISSN: 0168-583X.