An analog cell to detect single event transients in voltage references[☆]

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Abstract

A reliable voltage reference is mandatory in mixed-signal systems. However, this family of components can undergo very long single event transients when operating in radiation environments such as space, nuclear facilities, etc., due to the impact of heavy ions. The purpose of the present paper is to demonstrate how a simple cell can be used to detect these transients. The cell was implemented with typical COTS components and its behavior was verified by SPICE simulations and in a laser facility. Different applications of the cell are explored as well.

Keywords: Laser tests, long duration pulses, operational amplifiers, single event transients, voltage references

1. Introduction

Some electronic systems are designed to work in harsh environments, such as avionics, space, nuclear facilities or linear accelerators [1, 2]. In these environments, energetic heavy ions hit the electronic devices generating a high density of free carriers. If this happens in internal capacitances, such as gate oxides or reverse-biased PN junctions, the cloud is swept away by the electric field and an instantaneous current transient occurs, which is transmitted into the system.

With the exception of some mixed-signal components [3, 4], the only expected soft errors in analog devices are single event transients (SETs) due to the absence of memory elements. In particular, some works have reported that voltage references can show a very dangerous kind of SET called "long duration pulse" (LDP) [5, 6]. In special circumstances, the transients last for several hundreds of μs or even 1 ms. This characteristic is critical in analog-to-digital (A/D) or digital-to-analog (D/A) conversions [7]. In general, the output of a D/A or A/D converter is proportional to either V_{REF} or V_{REF}^{-1}. If a peak Δv_{REF} appears, it is easy to demonstrate that the analog or digital output shows a percentage error of $\pm\frac{\Delta v_{REF}}{V_{REF}}$. Voltage references are usually built using a core cell (e.g., band-gap cells or Zener diodes) followed by an operational amplifier (op amp) (Fig. 1). The core cell provides a reference value (V_{CORE}) independent of the power supply or the temperature whereas the op amp stabilizes the system by negative feedback, scales the reference voltage, and improves the output characteristics. Usually, voltage references must provide current to the load. Thus, a simple class-A output stage is an efficient and widely-used solution (Q_O and I_Q in Fig. 1) [5].

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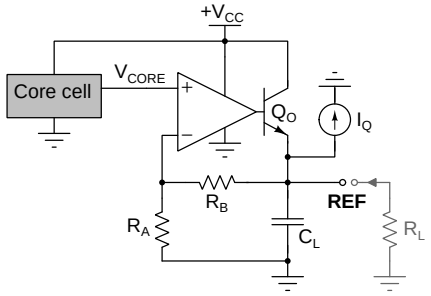


Figure 1: Standard voltage reference. A core cell, biased by the power supply, $+V_{CC}$, provides a stable voltage value (V_{CORE}) that works as the input of a non-inverting amplifier. Thus, $V_{REF} = \left(1 + \frac{R_B}{R_A}\right) \cdot V_{CORE}$. Typically, the output is just a class-A stage consisting of an NPN (or NMOS) transistor, Q_O, and a current source, I_Q, to bias it in the forward-active zone. The capacitor is included to filter noise. R_L represents a hypothetical load.

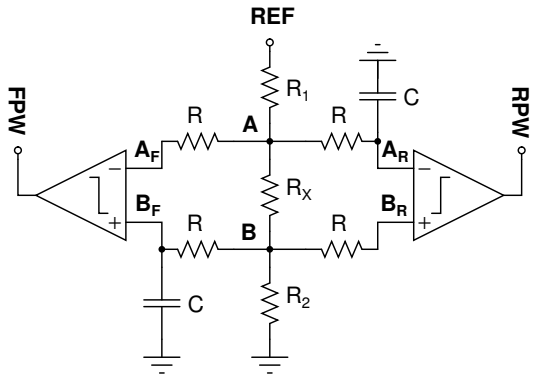


Figure 2: Proposed surveying cell. The output signals are the Rising Pulse Warning, RPW, and the Falling Pulse Warning, FPW. Some resistors are included to minimize the effects of the input bias currents. In comparators with open collector/drain output, additional pull-up resistors (R_{PU}) and a logic power supply ($+V_L$) are necessary.

LDPs in voltage references are a dangerous hazard since they lead to hundreds or thousands of erroneous conversions [5, 8]. In this paper, we are going to demonstrate how a very simple analog cell able to detect SETs beyond a tunable threshold value can help to solve this undesirable issue.

2. The cell and its properties

The proposed cell is shown in Fig. 2. In this cell, only passive components and two comparators are required. The input of the cell is REF and two warning digital signals (Rising Pulse Warning, RPW, and Falling Pulse Warning, FPW) are the outputs. Let us calculate the bias point, Q, accepting that the comparators have a high input impedance. It follows then that:

$$V_{A,Q} = \frac{R_2 + R_X}{R_T} \cdot V_{REF,Q} \tag{1}$$

$$V_{B,Q} = \frac{R_2}{R_T} \cdot V_{REF,Q} \tag{2}$$

R_T being $R_1 + R_2 + R_X$. At the bias point, $V_A = V_{AF} = V_{AR}$ and $V_B = V_{BF} = V_{BR}$ so $\Delta V_{BA} = -\frac{R_X}{R_T} \cdot V_{REF,Q} < 0$. Therefore, the outputs of both comparators are in the LOW state. Now, let us suppose that a transient occurs at REF. This transient can be modeled as a perturbation, $\pm v_{PK}$, around the bias point. Thus, during the transient,

$V^*_{REF} = V_{REF,Q} \pm v_{PK}$. The following step is to set the time constant, $\tau = R \cdot C$, much longer (e.g., one order of magnitude) than the worst-case transient duration. Given that the transient duration is ∼10–1000 μs [5, 6, 9], τ must be selected on the order of 0.1-10 ms. In this situation, the perturbation quickly reaches nodes A and B as well as nodes A_F and B_R, which are open circuits in practice. However, nodes A_R and B_F are not immediately affected due to the presence of the capacitors. Therefore, ΔV_{BA} becomes positive in one of the two comparators and its output switches to HIGH indicating the occurrence of an SET. Namely, rising transients, with $v_{PK} > 0$ trigger RPW, whereas FPW is activated by falling transients.

Now, the cell will be analyzed in a quantitative way. Instead of resolving the circuit in the frequency domain, we are going to use the standard technique in the field of small-signal circuits research, which consists in modeling the capacitors as short-circuits in AC mode. Later, DC and AC contributions will be added using the superposition principle.

Hence, it can be demonstrated that one of the comparators is triggered if v_{PK} falls outside the interval $[-V_{THF}, V_{THR}]$ with:

$$V_{THR} \approx \frac{R_X}{R_2} \cdot V_{REF,Q} \tag{3}$$

$$V_{THF} \approx \frac{R_X}{R_2 + R_X} \cdot V_{REF,Q} \tag{4}$$

if $R \gg R_1, R_2$. Also, if $R = R_1 = R_2$:

$$V_{THR} \approx \frac{2R_X}{R} \left(1 + \frac{1}{2}\frac{R_X}{R}\right) \cdot V_{REF,Q} \tag{5}$$

$$V_{THF} \approx \frac{2R_X}{R} \left(1 - \frac{3}{2}\frac{R_X}{R}\right) \cdot V_{REF,Q} \tag{6}$$

Anyhow, if $R_X \ll R_2$, $V_{THR} \approx V_{THF}$. An interesting feature is that, as the thresholds are defined as percentage values, the cell functions whatever the reference voltage. Finally, the analysis remains valid once the network has reached the bias point. Therefore, the cell does not work immediately after powering-up the system, the delay being on the order of τ.

It is interesting to check how non-idealities compromise the performance of the cell. First of all, let us investigate the effects of the resistor tolerance. For the sake of brevity, only the situation in which $R \gg R_1, R_2$ will be described. According to the error propagation theory, the uncertainty of V_{THR}, ΔV_{THR}, is related to the resistor tolerance as:

$$\frac{\Delta V_{THR}}{V_{THR}} = \frac{\Delta R_X}{R_X} + \frac{\Delta R_2}{R_2} \tag{7}$$

as it is easily deduced from Eq. 3. Therefore, precision resistors are strongly recommended.

Another interesting parameter to take into account is the input offset voltage of the comparators. For example, if $R \gg R_1, R_2$, the rising transients are detected if:

$$v_{PK} > V_{THR} + \frac{R_T}{R_2} \cdot V_{OS,R} \tag{8}$$

and the falling ones if:

$$|v_{PK}| > V_{THF} + \frac{R_T}{R_2 + R_X} \cdot V_{OS,F} \tag{9}$$

$V_{OS,R}$ and $V_{OS,F}$ being the input offset voltages of the comparators that detect **R**ising and **F**alling transients. Another parameter that can affect the performance of the cell is the input bias current of the comparators. In Fig. 2, we can see that every input of the comparators is connected to the nodes AF, AR, BF and BR. This will be the guideline to denominate the corresponding input bias currents. Defining them positive if flowing into the device, calculations show that they contribute to the effective input offset voltage as:

$$\Delta V^*_{OS,R} = \frac{R_X}{R_T}\left[R_2 \cdot (I_{BF} + I_{BR}) - R_1 \cdot (I_{AF} + I_{AR})\right] - R \cdot (I_{BR} - I_{AR}) \tag{10}$$

$$\Delta V^*_{OS,F} = \frac{R_X}{R_T}\left[R_2 \cdot (I_{BF} + I_{BR}) - R_1 \cdot (I_{AF} + I_{AR})\right] - R \cdot (I_{BF} - I_{AF}) \tag{11}$$

The influence of the input bias currents is minimized if currents are extremely low or, if $R_1 = R_2$, identical to cancel each other out.

3. Simulations in SPICE

In order to verify the functioning of the analog cell we carried out simulations using realistic SPICE models of commercial-off-the-shelf (COTS) discrete components found in the literature on electronic systems for space. The voltage reference was created using an LM124A SPICE micromodel in non-inverting configuration, which is an improved version of the one that was successfully used by the authors to investigate SETs in networks with op amps [6, 10, 11].

Concerning the output stage, the NPN transistor was modeled as a typical 2N2222A. Furthermore, the current source, I_Q, was removed since the feedback resistor network, R_A and R_B, managed to correctly bias the transistor in forward-active zone. Other parameters of the simulated voltage reference were $V_{CORE} = 1.25\ V$, $R_A = 33\ k\Omega$, $R_B = 100\ k\Omega$, which yield $V_{REF} = 5.0\ V$.

The cell was implemented using an LM311-like voltage comparator, depicted in [12, 13]. In this case, the SPICE micromodel was developed from the detailed schematic in the manufacturer's datasheet with identical transistor models to those of the LM124A micromodel. Current mirrors biasing the different stages were fitted from the original works by R. Widlar [14, 15]. As the comparator has an open-collector output, an additional pull-up resistor of 10 kΩ was necessary in the simulations.

Different combinations of R_L (0.1, 0.47, 1, and 4.7 kΩ) and C_L (0.1, 0.22, 0.47, and 1.0 μF) were used in the simulations to verify the correct operation of the cell. However, in this paper only the results associated with $C_L = 100\ nF$ and $R_L = 4.7\ k\Omega$ will be shown. The reason of selecting this resistance value is that it is on the order of the equivalent load of, e. g., typical R/2R networks in DACs [16, 17]. Finally, the simulation engine was NGSPICE rework 26, a GNU fork of Berkeley SPICE 3f5[1].

SETs were simulated by means of piece-wise current sources between the reverse biased CB junctions of bipolar transistors in forward active or cut-off zone. In particular, the rising transients were emulated by draining 0.4 pC from a specific transistor of the gain stage, $QR1$, and the falling ones by draining 3 pC from a neighbor transistor, $Q09$, also in the gain stage [6, 10, 11]. Preliminary simulations showed that the duration of the longest transient

[1] http://ngspice.sourceforge.net

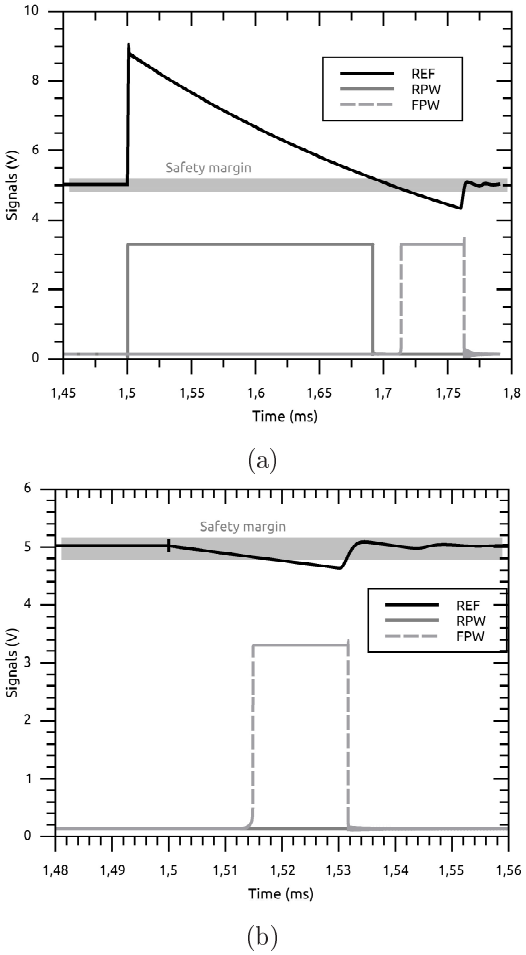


Figure 3: Response of the surveying cell in case of simulated SETs.

was below 250 μs. This value was necessary to determine the network parameters in Fig. 2, which were eventually chosen as $V_L = 3.3\,V$, $R_1 = R_2 = 10\,k\Omega$, $R_X = 200\,\Omega$, $R = 10\ k\Omega$, and $C = 220\,nF$. Therefore the threshold value was set around 200 mV and τ near 2.2 ms. Fig. 3a-b shows the response of the cell when rising (in reality, bipolar) or falling SETs occur, demonstrating that the cell apparently operates as expected. Every time the voltage reference output leaves the safety margin, $5\ V\ \pm\ 200\,mV$ (gray zone in both graphs), one of the logic signals switches to HIGH.

Finally, we would like to clarify the reasons for our choice of components. In actual designs, a dedicated voltage reference (discrete or that included in usual D/A or A/D converters) must be used instead of the system built with the LM124A and accessories. In this work, the voltage reference is built as described only for illustrating purposes. In fact, realistic transients are easily induced in this system and can be used to test the analog cell in typical conditions. Moreover, the LM311 was selected since it is still used in some designs and its behavior under radiation is well understood. Other newer, faster, and more reliable voltage comparators can be used in custom implementations.

4. Experimental results

Even though the theoretical behavior of the cells is quite simple and has been corroborated by simulations, the conclusive test is to confront the cell with an actual SET. An interesting and cheap option to induce SETs are laser facilities, which have become an excellent option to study heavy ions effects. These tests are specially accurate in old bipolar technologies, with transistor sizes of some tens of μm [18]. The laser wavelength at the UCM-CLUR [6, 10] was 800 nm, and the spot size of the focused laser was around 1 μm, much smaller than the typical transistors that make up the LM124A. The laser setup is thoroughly explained in other works by the authors [6, 10, 11, 13].

As in the simulations, the voltage reference was built using an LM124A as core op amp, biased by a unipolar 12-V power supply. External parameters were chosen identical to those of the simulations but, due to technical reasons, the voltage reference was build with two Si diodes in series configuration in such a way that $V_{REF} \approx 5.4\,V$. Finally, V_L, or logic power supply, was set to $+5\,V$. The LM124A, in ceramic package, was decapsulated mechanically to make the internal devices accessible. $QR1$ and $Q09$ were located on the surface of the decapsulated LM124A as shown in [6, 10] and illuminated by the laser light (Energy $\sim$ 50 pJ). According to [5, 8], the laser is equivalent to a heavy ion with LET$\sim$ 50 MeV·cm^2/mg. Results are shown in Fig. 4a-b. Both graphs demonstrate that the analog cell does detect SETs raising one of the outputs from LOW to HIGH. For the sake of clarity, only one of the digital signals is shown in each graph.

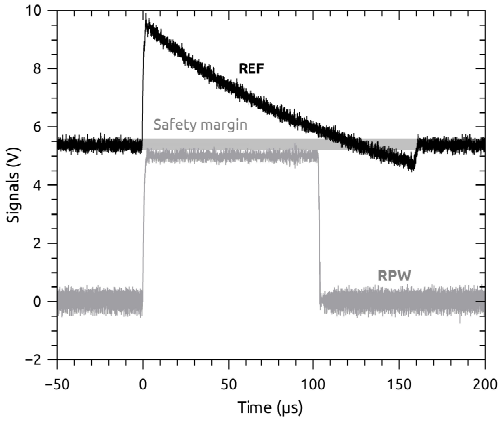
The cell was tested with different combinations of R_L (0.1, 0.47, 1, and 4.7 kΩ) and C_L (0.1, 0.22, 0.47, and 1.0 μF) and the detection was always correctly done. Only when the transient was very long ($\sim$100 μs), the signal apparently switched to LOW state before REF returned to the safety margin. This is attributed to the slow but unavoidable accumulation of charge in the capacitors, which shifts the threshold levels upwards.

An interesting point is the delay between the transients and the logic signals. Defining $t_{50\%}$ as the time needed by the comparator to reach 50% of the final logic value (2.5 V), the LM311 delay ranged from 0.6 to 0.8 μs depending on the value of the pull-up resistor At any rate, this delay is much shorter than the transient duration (some tens or hundreds of μs). On the other hand, switching from HIGH to LOW is almost instantaneous whatever the pull-up output resistor is. This delay should be shorter if this comparator is replaced by more advanced components.

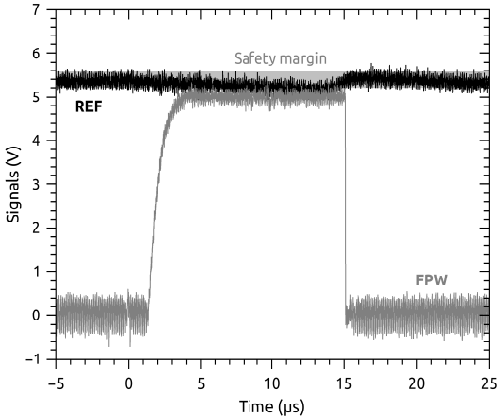
5. Discussion

5.1. Load effects

Several factors must be studied before using this cell in actual systems. First of all, it is necessary to determine how the cell affects the surveyed voltage reference. The load regulation is a typical parameter of voltage references that evaluates the voltage drop associated with the output current. Typical commercial voltage references such as the 5-V REF02 have a load regulation value below 0.01 %/mA. Accepting this value, the actual analog cell tested in the laser facility ($R_1 = R_2 = 10\,k\Omega$, $R_X = 100\,\Omega$, $R_T = 20.1\ k\Omega$) induces a negligible drop of $\sim$ 100 μV. However, voltage references liable to undergo SETs could be used in environments where total ionizing dose (TID) or displacement damage (DD) are expected (e.g., space, nuclear facilities, etc.). The load regulation is a parameter that increases with the permanent radiation damage. Even more, in very irradiated devices, the output stage of the voltage reference is so damaged that it cannot provide enough current to bias load resistors even on the order of 10 kΩ [17, 19].



(a)



(b)

Figure 4: Response of the surveying cell in actual SETs. For the sake of clarity, only the main warning signal is shown.

Finally, in spite of the fact that the cell is a two-pole/two-zero network, spontaneous oscillations were not observed during the tests whatever the values of R_L and C_L were.

5.2. Reliability of the cell

Additionally, it is reasonable to assume that the analog cell is exposed to the same kind of radiation as the surveyed voltage reference. First of all, SETs can occur also in the comparators. However, there are some reasons to believe that this is a minor threat. In the LM111 family, LOW-to-HIGH transients are typically very short ($\tau \lesssim 1\,\mu s$) and can even disappear if the pull-up resistor is large enough [12, 13, 20]. On the contrary, transients in voltage references can last for tens or hundreds of μs [5]. Besides, the threshold linear energy transfer (LET) value of the comparators dramatically decreases if the input voltage difference moves away some tens of mV from the switch threshold [20]. Finally, as it is shown in the following section, some applications are hardly affected by these transients.

Also, voltage comparators can experience an offset voltage drift as well as an increase of the input bias currents due to accumulated damage (TID, DD) [21]. The influence of the input offset voltage increase is enhanced in case of choosing a very large value of R_1 as deduced from Eq. 8 and 9. Besides, Eq. 10-11 shows that, if the currents are identical in the four inputs and $R_1 = R_2$, their influence vanishes. To conclude, as the input voltage difference is some tens of volts at the most, pernicious effects related to the asymmetric polarization of the inputs seem to be unlikely [21].

5.3. Mitigation of SETs

In voltage references, rising transients are very long due to the trapped charge inside the load capacitor (C_L in Fig. 1) [5, 6, 11]. A simple way to mitigate the transients is using the RPW signal to activate a low impedance path to drain the capacitor (e.g. the NMOS in Fig. 5a). This structure was tested in the laser facility using the IRFD014, a commercial discrete NMOS transistor, and $R_P = 100\,\Omega$. Fig. 5b shows the signals obtained with identical loads to those of Fig. 4a. The first conclusion is that the peak voltage hardly changes from Fig. 4a to Fig. 5b. Unfortunately, this strategy makes the transient shorter but not smaller. Second, the RPW signal rises more slowly due to the influence of the parasitic capacitor at the NMOS transistor gate. Finally, the transient duration is reduced from $150\,\mu s$ to hardly $30\,\mu s$. Even more, the most significant initial positive peak is reduced from $110\,\mu s$ to $12\,\mu s$.

The transient detection is more effective if FPW and RPW signals are NORed to create a single warning signal, $WARN$. For instance, microprocessors or FPGAs that process the digital signal coming from an ADC can use the $WARN$ signal to dismiss data obtained during the transient. Moreover, combined with a backup voltage reference, it can be used to set a constant value of reference voltage independently of the occurrence of SETs. The idea is shown in Fig. 6. If the $REF1$ signal is correct, $FPW = RPW = LOW \rightarrow WARN = HIGH$. In case a transient occurs at $REF1$, the NOR gate output switches to LOW activating a single pole, double throw (SPDT) switch that selects a backup reference voltage, $REF2$. Formally, the system compares $REF1$ with its copies in the capacitors and, in case of disagreement, the system selects the third option, $REF2$. Defining $REFC$ as the voltage in the capacitors, it is easy to deduce that REF is the output of the algorithm

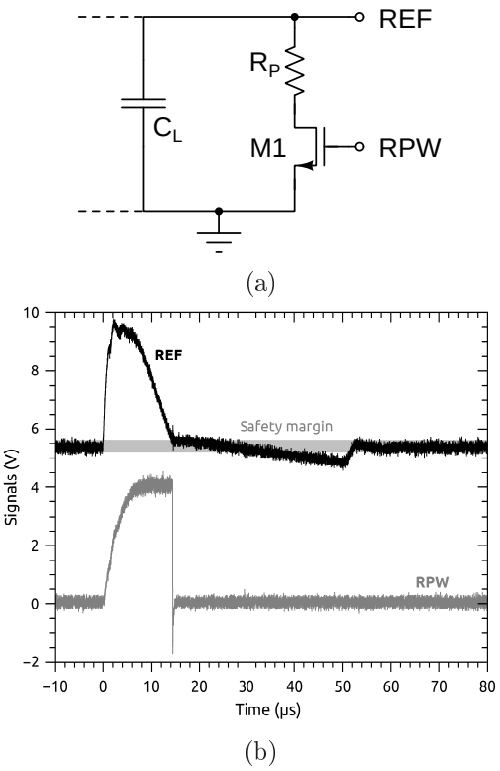


Figure 5: Mitigation of transients using the analog cell. An NMOS, controlled by the RPW signal, is in OFF state and switches to linear zone if $RPW = HIGH$ (a). The second graph shows the mitigated transient (b).

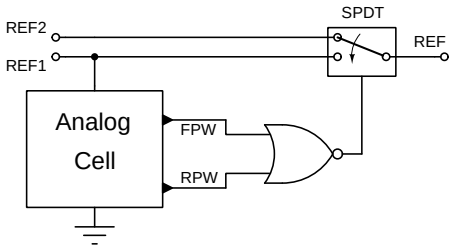


Figure 6: A circuit to keep the reference voltage constant.

$$if\ (REF1 = REFC)\ then\ REF = REF1$$

$$else\ REF = REF2$$

If $REF1$, $REFC$, and $REF2$ were logic signals instead of analog ones, the algorithm would be formally equivalent to a majority voter for Triple Modular Redundancy (TMR).

Transients are rare events so it is very improbable that both references fail simultaneously. Typically, COTS components appropriate for this circuit are built in high-voltage CMOS technologies. However, if damage by accumulated radiation is expected, the NOR gate can be chosen from the SiGe family [22, 23] while the analog switch can be the SW06, with only bipolar and JFET transistors and therefore very tolerant to TID damage. Finally, it must be taken into account that SETs in the comparators or the NOR gate do not affect the effective output (REF in Fig. 6).

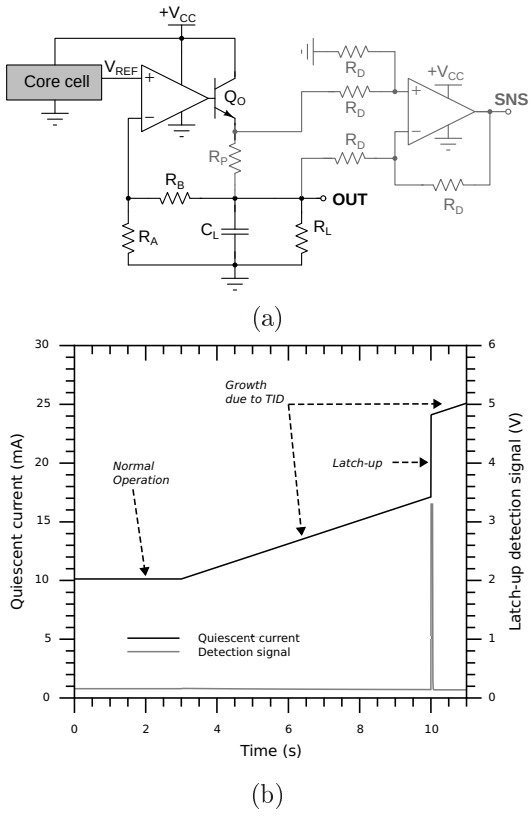


Figure 7: Typical circuit (in gray) to measure the quiescent current needed by a load (a). SPICE simulation of the behavior of the analog cell which surveys the SNS signal (b). From $t = 3s$ on, the quiescent current slowly increases due to a TID damage, but the cell is not triggered. At $t = 10s$, a latch-up occurs and is detected by the cell ($R_1 = R_2 = R = 10\ k\Omega$, $R_X = 100\,\Omega$, $C_L = 1\,\mu F$, $R_P = 100\,\Omega$, and $R_D = 20\,\Omega$).

192 *5.4. Other potential applications*

193 The cell can also be useful during the preparation of heavy-ion or laser tests. When a researcher wants to
194 characterize an analog device with a constant output value in a radiation facility, the typical procedure consists in
195 setting the oscilloscope trigger to a threshold level and register every transient going beyond this level. Unfortu-
196 nately, some low-end oscilloscopes have no bipolar trigger. In other words, they can be set to detect rising or falling
197 transients, but not both simultaneously. The analog cell solves this problem since the $WARN$ signal can trigger
198 the oscilloscope whichever the kind of transient is.

199 Another application is the detection of latch-up in accelerated radiation tests. One of the advantages of the cell
200 is its independence of the DC level of the surveyed voltage signal. Also, shifts in this voltage are not detected if
201 they are slow. Fig. 7a shows a differential amplifier measuring the voltage drop across a sense resistor, R_P. The
202 output voltage, V_{SNS}, which is proportional to the output current, is surveyed by the analog cell. SPICE simulation
203 results are shown in Fig. 7b. One can see that the analog cell is only triggered by the latch-up and not by the slow
204 drift. Obviously, this detection technique is only appropriate for static tests as the cell will show false detections if
205 there are sudden requirements of current (e. g., while writing/reading a memory).

6. Conclusion

A simple analog cell is proposed to detect single event transients in voltage references. This cell was implemented with discrete passive components and two typical voltage comparators and its correct functioning demonstrated by means of SPICE simulations and in a laser facility. Also, it can be used to mitigate the transients making their duration much shorter or to select a backup voltage reference in case the main one fails. Finally, it can simplify the setup of static tests of components in heavy-ion or laser facilities since it allows the use of low-end oscilloscopes and the simple detection of latch-up.

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