Impact of High Particle Flux in Radiation Ground Tests with Protons

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***Abstract*—This abstract presents an experimental study of the impact of using a high flux in radiation ground tests on the measured cross-section of SRAMs. Experimental results obtained with 15 MeV protons will show that using a high particle flux makes the measured cross-section increase by almost 1 order of magnitude.**

***Index Terms*—COTS, SRAM, proton tests, radiation hardness, reliability, soft error.**

I. INTRODUCTION

RADIATION is a notable challenge in semiconductor devices, since it can seriously affect their normal operation in space missions, avionics, and even on Earth's surface [1]. Therefore, the impact of the so-called Single Event Effects (SEEs) has to be studied and taken care of. A common way of assessing the reliability of systems is by performing accelerated radiation-ground tests, such as neutron, proton and heavy-ion (HI) tests [2].

However, not only must a facility provide the correct type of particle with the desired energy, but also the test conditions must be as realistic as possible in order to issue results that can be extrapolated to the actual conditions. This is a challenge for researchers, since there are a number of factors that affect the device sensitivity, apart from the energy and type of particle. Hence these conditions must be reproduced in the radiation-ground test, or at least, accounted for, so as to provide accurate estimations.

One of these factors is the angle of incidence of the particle [3]. For ionizing particles, it is well-known that, as the incident angle with respect to the normal one increases the effective Linear Energy Transfer (LET) by, at least as first approach, a factor $1/cos(\theta)$, θ being the tilt angle [4]. In addition, the probability of multiple events increases with such angle of incidence. Environmental temperature also plays an important role. For instance, [5] showed that MCU sensitivity increases at elevated temperatures. Operating voltage also affects the sensitivity of modern devices, since the critical charge needed to trigger a SEE decreases at low VDD [6], [7]. It also has been shown that some memories can suffer from Total Ionizing Dose (TID)-SEE synergistic effect, which increases the sensitivity against neutrons and protons [8], [9].

Other factor that, if neglected, might lead to an incorrect interpretation of the observed events is the total particle fluence in the same round of data retrieval. The reason is that two independent events that coincidentally affect nearby cells can be mistakenly identified as a single one with higher multiplicity [10]. The probability of this phenomena happening increases with the number of observed events, which, in turn, increases with the particle fluence. Therefore, if a radiation ground experiment with a too high fluence was carried out, the number of such "false events" would not be negligible and the results should be corrected accordingly. In such an experiment, the probability of occurrence of Multiple Bit Upsets (MBUs) would increase too, which might break Error Correcting Codes (ECC) [11], but such a study is out of the scope of this work.

This abstract discusses an additional factor that has been found to affect the measured cross-section of a given device. It was observed that, in proton radiation ground experiments, increasing the flux (ranging from 9.7×10^7 to 4.9×10^9 p/cm^2/s) leads to measuring higher cross-sections in the device. This phenomena was previously described by other authors in the literature, for heavy ions. In [12], the effect of high HI fluxes on several SRAM-based FPGAs with and without Error Detection And Correction (EDAC) is discussed, and it was concluded that these techniques are more sensitive to higher fluxes. However, it is not clarified if this phenomena is due to accumulation of simpler events (as discussed in [10]), the high particle flux itself (as discussed in this abstract) or both. In [13], the authors present experimental results with heavy ions at fluxes ranging from 10 up to 10^4 ions/cm^2/s on various devices (bulk and SOI SRAMs, D flip-flops and a PROM). The cross-section is almost constant for all the devices up to 10^3 ions/cm^2/s. After that, the cross-sections start to increase with the flux and the trend is different depending on the device. The same increase was for various HI energies (13MeV to 99MeV). The same authors, in [14], extend this work with GEANT4 and TCAD simulations and they discuss the physical aspects of the phenomena.

Herein a similar effect is discussed, for protons instead of HI. Tests were made on two Commercial-Off-The-Shelf

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(COTS) SRAMs, manufactured with bulk 130-nm and 65-nm CMOS technologies, under 10 MeV and 15 MeV protons. The experimental proton fluxes were within the especified range in the ESCC Basic Specification No. 25100, by ESA [15], which specifies that *"the high energy proton accelerator shall be capable of delivering protons [...] with a variable flux ranging from* 10^5*p/cm*^{2}*/s to at least* 10^8*p/cm*^{2}*/s on the device under test"*. In all the cases, the authors made sure to account for the possible presence of false multiple events, by using the equations presented in [10]. Hence, the phenomena described in this paper was not because of that. Tests under increasing and decreasing fluxes were performed to investigate if this strange behavior is due to accumuladed ionizing dose.

II. Experimental Setup

The proton irradiation test campaigns took place at CNA (Centro Nacional de Aceleradores), in Spain [16]. The experiments were performed using the external beam line installed in the 18/9 IBA compact cyclotron laboratory. A primary 18 MeV proton beam is tuned in the isochronous cyclotron, with fix RF system frequency (42 MHz). Only the current intensity on the PIG source (Penning ionization gauge), is modified in between the runs depending on the desired ion current density. The beam is extracted to the external line and passes through a $100\,\mu\mathrm{m}$ aluminium foil, placed as window. The optimized parameters, for ion transmission and minimum environmental background, are maintained during all the campaigns. The Device Under Test (DUT) was placed on a remotely controllable table at 56 cm from the exit nozzle, so that the final proton energy at the surface was 15 MeV, as calculated with the SRIM2013 code [17]. The memories were not decapsulated, therefore the proton energy at the sensitive area was slightly lower. The uniformity of the flux was better than 90% in the exposed area of interest, maintaining the flux stability within 5% during each experimental run. The proton flux monitoring is performed measuring the beam current into an electrically isolated graphite collimator behind the exit window. A medium flux value is calculated in accordance with the pulses registered by the counter.

The DUT was controlled by a microcontroller board based on the Atmel SAM3X8E ARM Cortex-M3 CPU running at up to 84 MHz. The microcontroller is connected to a computer system in order to provide power and store the results. The system was completely tested before and after the radiation, to guarantee that the observed errors were due to radiation and not consequences of a problem in the experimental setup. Everything in the radiation room except the DUT itself was shielded with thick aluminum plates, whereas the computer was in another room for controlling and monitoring the process.

III. Experimental Results and Discussions

Experiments were done on CY62167GE30-45ZXI bulk 65-nm and CY62167DV30LL-55ZXI bulk 130-nm COTS SRAMs, under 15 MeV and 10 MeV protons. Due to the lack of space, the latter are not presented in this abstract and they will be discussed in the extended version. 90-nm SRAMs were also tested but underwent catastrophic latchups during the tests so no useful data could be taken. All the tests were run under 1 minute of radiation time. Table I shows the run sequence of the experiments on three 65-nm memories and a 130-nm one. Devices (a) and (c) were tested by increasing the flux from the minimum one available in the laboratory set-up ($\sim 1\times10^8$p/cm^2/s) to the maximum one. The flux and fluence values are given with an accuracy of 90%. In order to rule out the possibility of the total dose accumulation effect, tests on device (b) were run starting from the highest flux in a decreasing manner.

TABLE I

Run sequence of the irradiation campaigns including the total number of bitflips, SBUs and 2-bit MCUs

Device	Flux (p/cm^2/s) $\times10^8$	Fluence (p/cm^2) $\times10^{10}$	SBUs	2-bit MCUs	Total Bitflips
65-nm (a)	1.0	0.6	55	14	86
	2.2	1.3	209	64	403
	4.3	2.6	921	231	1508
	6.6	4.0	2070	523	3362
	12	7.2	5672	1349	9128
	34	20	17311	3748	27271
65-nm (b)	43	25.8	22885	4463	34765
	25	15.0	10739	2390	16934
	12	7.2	3611	901	5824
	6.6	3.9	1465	343	2338
	3.2	1.9	389	93	638
	2.7	1.6	271	67	423
	1.6	0.9	120	23	181
	1.1	0.6	46	13	78
65-nm (c)	2.2	1.3	171	35	260
	3.2	1.9	378	85	583
	5.1	3.1	929	250	1525
	15	9.9	5674	1306	8926
	31	19	14590	3009	22466
130-nm (d)	1.2	0.7	118	14	162
	1.6	0.7	172	47	277
	2.1	1.3	336	51	492
	3.0	1.8	626	107	906
	4.7	2.8	1386	190	1999
	9.6	5.8	5111	763	7343
	16	9.6	11072	1669	15993
	29	17	25823	3423	36989
	49	29	57307	4866	77778

Primary results show that increasing the particle flux makes the number of bitflips skyrocket. For device (a), increasing the flux from 9.7×10^7p/cm^2/s to 3.4×10^9p/cm^2/s (increased by 35 times) drastically inflate the total number of bitflips by 317 times. Similar trends can be observed for all the 65-nm memories, regardless of increasing or decreasing tests. For device (d), the 130-nm memory, even if the total number of bitflips is higher, when matching it against the 65-nm device at the same fluxes, a similar impact is observed.

To have a better insight into this phenomena authors extracted the number of SBUs/MCUs from the whole set of

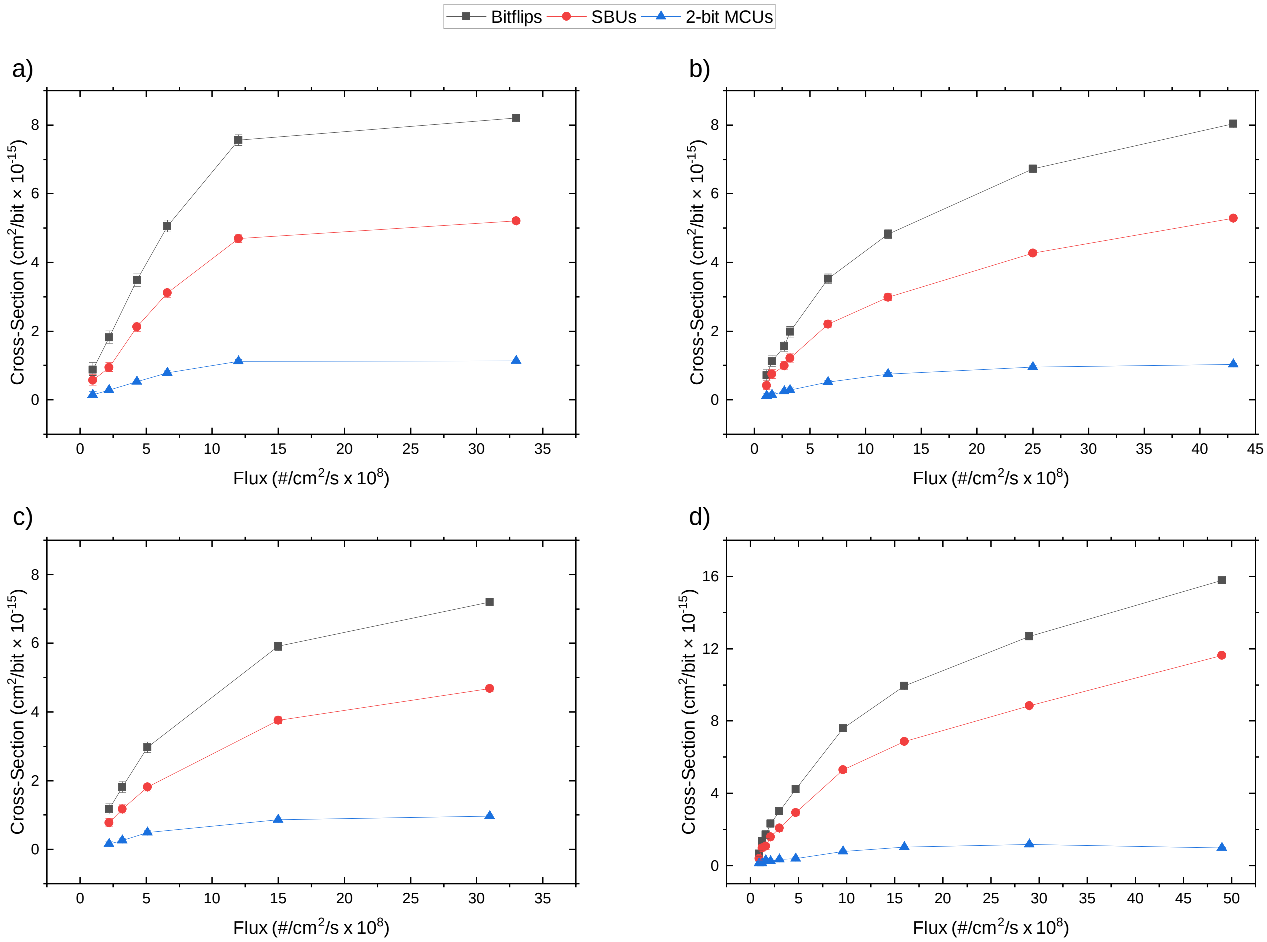

Fig. 1. Cross-section vs flux of 65-nm ((a), (b) and (c) are corresponding to Table I) and 130-nm (d) memories under 15 MeV protons

bitflips. Proprietary unscrambling information from Cypress Semiconductor was used for this purpose, which allowed relating addresses involved in the same multiple events. Any isolated bitflip observed in the memory is presented as an SBU. Affected addresses located at a Manhattan distance equal or lower than 3 were grouped in the same MCU.

To eliminate the effect of false MCUs in the results, the authors used the equations presented in [10] that estimate the number of false 2-bit events. Since efficiently estimating the number of false events of larger multiplicity is not possible[1], they are not presented in Table I. However, the effect of larger MCUs can be seen in the table, by comparing the total number of bitflips with the sum of the SBUs and 2-bit MCUs.

To be able to compare the results precisely, experimental cross-sections for each event type were calculated. Fig. 1 shows the corresponding results to Table I. All the plots include error bars for the experimental cross-section calculations however they are smaller than the size of the symbols in most of the cases. In this figure, plots (a) and (c) are the results for the 65-nm memory with increasing flux sequence and plot (b) is for the same build technology in an inverted sweep. The results for the 130-nm memory are presented at plot (d). It can be seen that the speed of the increase in cross-sections is steeper when the flux raises from 10^7 to 10^8p/cm^2/s, for all the tests. Further increasing the flux has a lower impact on the cross-section, especially for the 65-nm memories.

Performing the reverse sweep (Fig. 1.b) does not show any significant difference in the final results. Minor deviations can be attributed to sample-to-sample variations. No major difference is observed between the behaviors of the three 65-nm devices that were tested (Figs. 1.a-c) either. For the 130-nm results (Fig. 1.d), even if the total sensitivity of this technology against proton radiation is higher, the same phenomena can be observed too. It is important to notice that this phenomena cannot be due to false events [10]. Indeed, considering all the large size MCUs as false events and adding them to the total number of SBUs, will just alter the SBU cross-section lines marginally to the total event cross-sections.

It should be mentioned that, to discard the possible effect of the environmental radiation background coming from the experimental bunker, another set of tests were carried out. The front side of the DUT was shielded with an enough thick layer of aluminum to stop the primary beam while being placed in the same position as previous tests. No bitflips were noted after 1 minute of radiation with the flux being equal to 4×10^9p/cm^2/s.

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[1] Such estimations still remain an open problem [18], which is out of the scope of this work

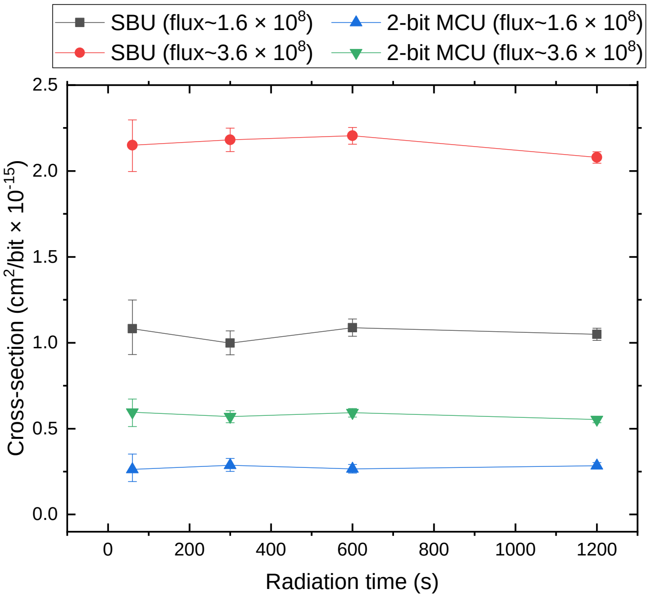

Fig. 2. Cross-section vs. radiation time of the 65-nm memory for two different fluxes: 1.6×10^8 and 3.6×10^8p/cm^2/s

By definition, total particle fluence is directly proportional to the radiation flux and exposure time of the DUT against the beam. Therefore, changes in total fluence can be made by means of altering flux or radiation time. The tests discussed above were carried out by increasing flux; but authors performed additional tests to study whether or not the radiation time affects devices' sensitivity. Two sets of tests were performed with two different fluxes (1.6×10^8 and 3.6×10^8p/cm^2/s), and said fluxes were always kept constant in each set. Fig. 2 shows the cross-sections of the same 65-nm memory. The radiation times ranged from 60 to 1200 seconds.

Even though the behaviour is not completely flat, it can clearly be observed that the irradiation time does not affect the total sensitivity of the device. Authors believe that the small fluctuations in the results are due to inconsistencies in the flux measurements for each radiation time.

Meanwhile, the cross-section of each event type (SBUs and 2-bit MCUs) at a flux of 3.6×10^8p/cm^2/s is constantly double than the other test (flux = 1.6×10^8p/cm^2/s). However, comparing the number of MCUs with larger multiplicities shows that performing the tests with higher radiation time increases the probability of observing large MCUs. These larger-size events can be a result of the accumulation of the SBUs or smaller MCUs. However, such a study is out of the scope of this work.

The origin of this phenomena can come from multiple and rapid hits to the cells of the DUT. This may prevent the cells to lose the charge and result in a bitflip by double hits. Another explanation can be due to the secondary particles after the protons hit the cover layer of the DUT. As mentioned before it is noted in previous studies that SRAMs show higher sensitivity to high flux HI. More studies need to be done on this aspect and more details will be included in the full extended paper.

IV. CONCLUSIONS

Experimental proof of dependency of the event cross-sections against 15 MeV protons radiation flux is presented in this abstract. CY62167GE30-45ZXI bulk 65-nm and CY62167DV30LL-55ZXI bulk 130-nm COTS SRAMs were tested in this study. Results show that increasing the radiation flux in the range of 10^8 to 10^9p/cm^2/s inflates the sensitivity of these devices up to 10 times. The results were similar regardless of changing the flux in increasing or decreasing manner, which excludes the possibility of the TID biasing the results. Altering the fluence by increasing the radiation time does not show any significant effect on the cross-section of the 65-nm memory. The results of the further tests with 14 MeV neutrons and 10 MeV protons along with detailed discussions about the physical aspects of this phenomena will be presented in the extended version.

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