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Conference Paper · February 2015

DOI: 10.1109/CDE.2015.7087508

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Thermal stability study of AlGaN/GaN MOS-HEMTs using Gd_2O_3 as gate dielectric

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***Abstract*—Thermal stability of AlGaN/GaN MOS-HEMTs and -diodes using Gd_2O_3 are investigated by means of different thermal cycles and storage tests up to 500ºC for one week. IV DC and pulsed characteristics of the devices before and after the processes are evaluated and compared with conventional HEMTs. Results show that the devices with Gd_2O_3 dielectric layer have lower leakage current and a more stable behavior during thermal treatment processes compared with conventional devices. In fact, an excellent on/off ratio of about 10^8 and a stable V_t is observed after storage at high temperature. The beneficial effects of Gd_2O_3 on trapping effects of MOS-HEMTs are also discussed.**

Keywords—AlGaN/GaN; Gd_2O_3; HEMTs; MOS-HEMTs; thermal stability; high-k dielectric

I. INTRODUCTION

AlGaN/GaN-based high electron mobility transistors (HEMTs) are key devices in high power and high frequency applications [1, 2]. However, high gate leakage currents and thermal stability issues are two of the problems which need to be solved to improve device reliability [3].

To reduce the gate leakage current, metal–oxide–semiconductor HEMTs and MOS-HEMTs with thin dielectric layers, such as Al_2O_3 [4], HfO_2 [5] and Gd_2O_3 [6], deposited between gate and barrier layer, have been studied. In particular, Gd_2O_3 is a promising candidate for the gate dielectrics on GaN due to its high dielectric constant, low electrical leakage currents and reduced interfacial density of states (D_{it}) with GaN [6]. Previous publications have shown the use of Gd_2O_3 grown by electron-beam heating [6] or molecular beam epitaxy (MBE) [7] on GaN or AlGaN/GaN structures. Thermal stability of GaN based HEMTs has been studied [8, 9], but very little work has been devoted to the study of Gd_2O_3-AlGaN/GaN MOS-HEMTs.

In this study, conventional diodes and HEMTs and Gd_2O_3 based MOS-diodes and MOS-HEMTs are fabricated simultaneously by the same procedure. The MOS devices have a thin layer of Gd_2O_3 under the gate metal, deposited by high pressure sputtering [12]. Electrical characterization of the devices is carried out at room temperature before and after several thermal treatments.

II. EXPERIMENTAL DETAILS

(MOS-)HEMTs and (MOS-)diodes were processed simultaneously on the same piece of wafer: AlGaN/GaN heterostructures grown on (111) silicon wafer with a GaN cap (2 nm) layer by metal-organic chemical vapor deposition. The Al content and the thickness of the AlGaN layer was 31.6% and 22.5 nm, respectively. The GaN layer was unintentionally doped, with a thickness of 0.1 μm. Cross sections of the (MOS-)HEMTs are sketched in Fig. 1.

A 20 nm Ti/120 nm Al/40 nm Ni/50 nm Au metal stack was used for ohmic contacts, e-beam evaporated and then rapid thermally annealed at 850ºC for 30s using a two-step ramp in N_2 ambient. Afterwards, device isolation was achieved by etching 100 nm deep trenches using inductive coupling plasma etching with a Cl_2/Ar based recipe. The contact resistance (R_c) of the ohmic contacts and the sheet resistance (R_{sheet}) of the 2-dimensional electron gas were 0.86 Ω·mm and 263 Ω/□ respectively, calculated using transmission line method technique [10].

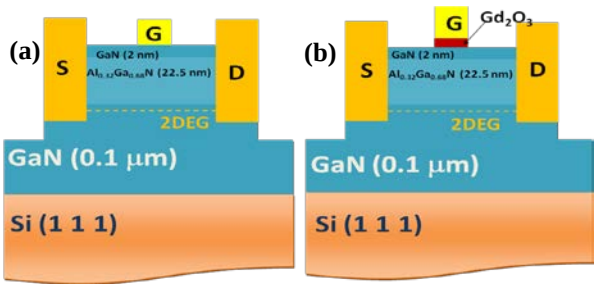

Figure 1. Schematic cross-section of (a) conventional HEMTs and (b) Gd_2O_3 based MOS-HEMTs

Prior to the gate metallization, half of the sample was covered by photo resist and on the other half, high pressure sputtered Gd_2O_3 films [11, 12] were deposited after the gate definition. The Gd_2O_3 layer thickness (4.2 ± 0.3 nm) and roughness (root mean square of 2.1 nm) were evaluated by atomic force microscopy. Ni (20 nm)/Au (200 nm) gates were defined by e-beam and standard lift-off techniques.

The gate length of the (MOS-)HEMTs is 1.2 μm and the width is 50 μm. The distance between gate and

drain is 5 μm. The Schottky and MOS diodes (with and w/o Gd_2O_3) have a square shape with a 100 μm side.

Several thermal treatments were conducted as described in Table 1. Before and after each treatment the same electrical measurements procedure was carried out on the devices at room temperature, including: thermal annealing at 500°C for 5 minutes; thermal cycle from room temperature (RT) to 425°C with a step of 100°C; and thermal storage at 500°C for one week in total.

TABLE I. MEASUREMENTS PROCESS IN THE STUDY

Process	Temperature	Time	Characterization
#1	500°C	5 mins	Before/after
#2	RT to 425°C (step 100 °C) then to RT	40 mins/step	Before/during/after
#3	500°C	1 week	Before and after each day

The electrical measurement procedure carried out as described in Table I was: current-voltage (I-V) and capacitance-voltage-frequency (C-V-f) characterization of the diodes using an Agilent 4156C semiconductor parameter analyzer and an HP4284A LCR analyzer; DC and pulsed I-V measurements on the HEMTs using a system formed by a Yokogawa DLM2000 digital oscilloscope and an Agilent 81150A pulse function arbitrary noise generator remotely controlled by a PC. The pulsed I-V measurement was a double pulsed (gate and drain) measurement at different quiescence points ($V_{DS,\,Q}$, $V_{GS,\,Q}$) = (0 V, 0 V), (0 V, -8 V) and (15 V, -8 V), with a pulsed width of 400 ns and a duty cycle of 0.01%.

III. RESULTS AND DISCUSSION

I-V characteristics of the MOS and Schottky diodes at RT before and after each thermal process are shown in Fig.2. The reverse gate current of MOS-diodes before any test is 4 orders of magnitude smaller than that of the Schottky diodes. A similar trend is observed after each thermal process, showing an advantage of using Gd_2O_3 films as gate dielectric in HEMTs for high temperature applications. In addition, Schottky diodes show an abrupt increase in forward leakage current (from 0.1 A/cm^2 to 200 A/cm^2) after storage of one day at 500°C, leading to permanent device degradation. This degradation is not observed in the MOS-diodes. From the capacitance measurements, the dielectric constant of the Gd_2O_3 layer is calculated to be in the 11-13 range, similar to the previously reported results [13]. Interestingly, no significant change is found in the capacitance in accumulation region during the thermal processes, which suggests that no damage is caused to the dielectric layer during the thermal treatment.

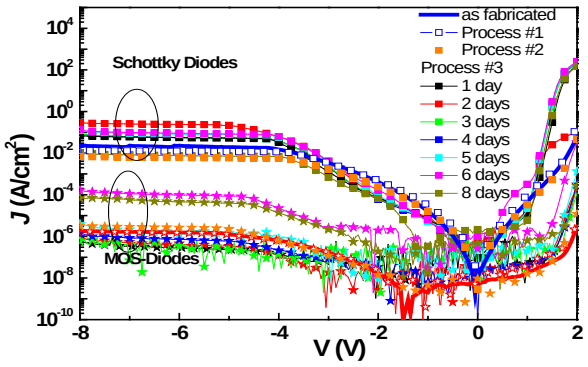

Figure 2. Gate leakage current density of Gd_2O_3 based MOS-Diodes and Schottky Diodes before and after thermal treatments

Figure 3 shows the output characteristics of the (MOS-)HEMTs before and after each thermal process. In order to clarify the figure, only the "after one day" curve is plotted for process #3. No significant changes are observed in the maximum drain currents ($I_{DS,max}$) at V_{GS}= 0 V of both MOS-HEMTs and HEMTs before any thermal process and after processes #1 and #2. However, after one day at 500ºC (from process #3), the HEMT devices show a decrease of 20% in the $I_{DS,max}$ and a 77% increase in the on-resistance (R_{on}), from 6.5 Ω·mm to 11.5 Ω·mm. In contrast, MOS-HEMT devices are stable and showed almost no change in the $I_{DS,max}$ and R_{on} even after one week at 500ºC (process #3). As on-resistance is an important issue in AlGaN/GaN based HEMTs for power applications [14], MOS-HEMTs with Gd_2O_3 dielectric layer are very suitable for those applications at harsh environments.

The transfer characteristics of the devices before and after each process are shown in Fig. 4. The off-state drain current of HEMTs show a decrease about two orders of magnitude after the #1 and #2 processes. However, it increases drastically about four orders of magnitude after one day at 500ºC, showing a permanent degradation, as observed previously. In contrast, the off-state drain current values of MOS-HEMTs show only a change within one order of magnitude before and after the thermal processes, and it is four orders of magnitude lower than the HEMTs. In addition, an excellent on/off current ratio of 10^8 in the MOS-HEMTs is observed, indicating an excellent charge modulation even after one week at 500ºC, as shown in Fig. 4 (b).

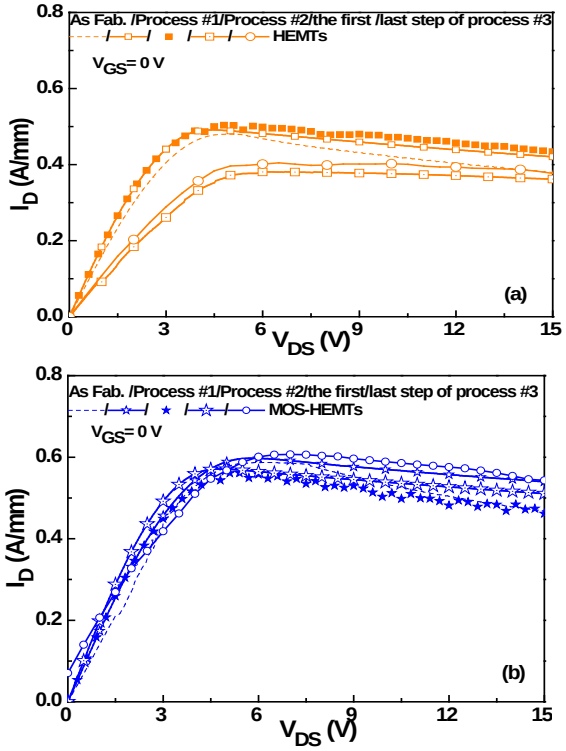

Figure 3. I_D-V_D of (a) AlGaN/GaN conventional HEMTs and (b) Gd_2O_3-AlGaN/GaN MOS-HEMTs from process #1, #2, the first and last steps of process #3

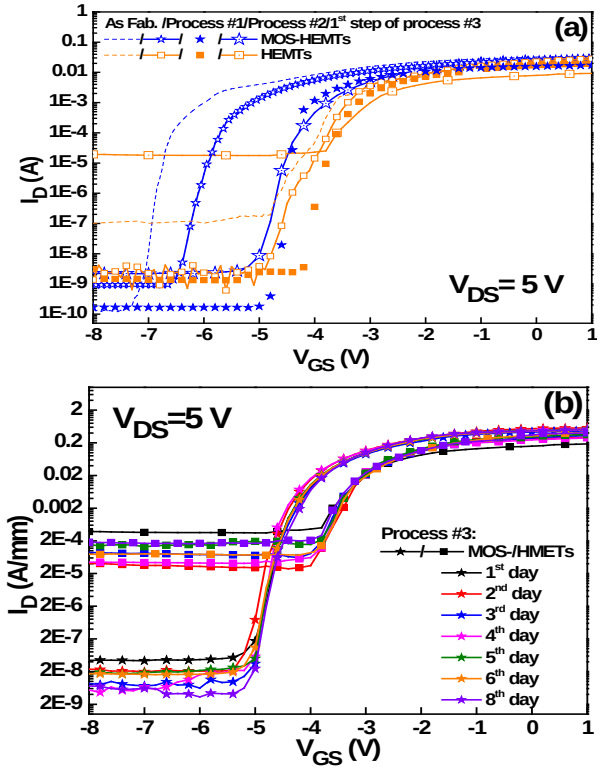

Figure 4. I_{DS}-V_{GS} characteristics of AlGaN/GaN conventional HEMTs and Gd_2O_3-AlGaN/GaN MOS-HEMTs at V_{GS}=0.1 V from (a) Process #1, #2, the first check of process #3, and (b) process #3

The threshold voltages (V_t) of the MOS-HEMTs shows a positive shift during the stability tests at high temperature: from -6.8 V before the thermal processes, to -5.8 V after process #1, and to -4.8 V after process #2 (Fig. 5a). However, no significant change is observed during process #3 (Fig. 5b). Therefore, V_t becomes stable after process #2, suggesting that a soft annealing should be necessary after the Gd_2O_3 deposition to enhance the thermal stability of the MOS-HEMTs.

Moreover, Fig. 5a shows a significant decrease (~75%) in maximum transconductance at V_{DS}=0.1 V in the conventional HEMTs after one day storage at 500°C. This decrease is consistent with the degradation behaviors previously observed in the devices. Furthermore, the peak transconductance of the MOS-HEMTs is about 40% higher than that of the conventional HEMTs during the thermal storage process #3 (Fig. 5b), supporting the convenience of using MOS-HEMTs for high temperature applications compared with conventional HEMTs.

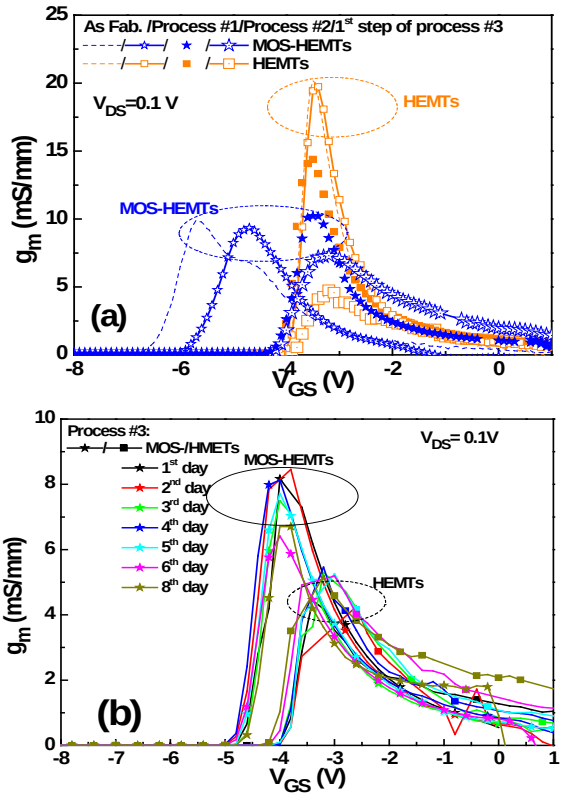

Figure 5. Transconductances of AlGaN/GaN HEMTs and Gd_2O_3-AlGaN/GaN MOS-HEMTs at V_{GS}=0.1 V from (a) process #1, #2, the first check of process #3, and (b) process #3

Figure 6 shows the current collapse and the associated degradation from the double pulsed measurements. $I_{DS}^{pulsed}/I_{DS}^{ref}$ was defined at different quiescence points ($V_{DS,Q}$, $V_{GS,Q}$) = (0 V, -8 V) (gate lag) and (15 V, -8 V) (drain lag), taken ($V_{DS,Q}$, $V_{GS,Q}$) = (0 V, 0 V) (no self-heating) as a reference.

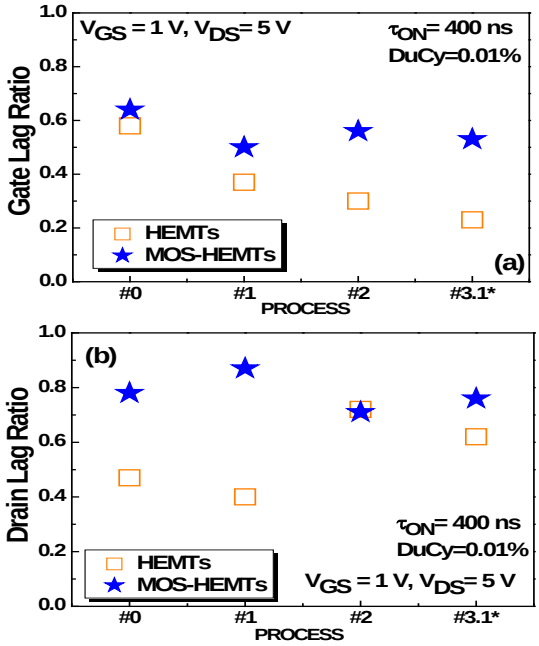

Figure 6. (a) Gate lag ratio and (b) Drain lag ratio of HEMTs and Gd_2O_3 MOS-HEMTs from pulse measurements, * Process #3.1: the first step of process #3

Results show that MOS-HEMTs have more stable gate lag ratio (0.56±0.06) and drain lag ratio (0.78±0.07) compared with HEMTs during all processes. This further proves that the MOS-HEMTs with Gd_2O_3 dielectric layer have better stability with temperature. In addition, the gate lag ratio in HEMTs shows a 60% decrease after one day during process #3 respect to the as-fabricated devices, which could be related to the increase of surface states or traps. This is not observed in the MOS-HEMTs, showing that the thin dielectric layer helps to diminish the traps on the surface of the heterostructure, even without any additional surface passivation between gate and drain.

IV. CONCLUSIONS

In summary, AlGaN/GaN MOS devices with a thin layer of Gd_2O_3 under the gate are fabricated, and their thermal stability are studied and compared by means of three thermal treatment processes. Results show that the devices with Gd_2O_3 dielectric layers have a reduced gate leakage current and a more stable behavior during the thermal treatments, especially during the thermal storage process. The conventional HEMTs show degradation after a one day's thermal storage at 500°C: increased gate leakage current and on-resistance, reduced maximum drain current, maximum transconductance and gate lag ratio, whereas MOS-HEMTs show less degradation. This demonstrates that MOS-HEMTs using Gd_2O_3 dielectric have improved time tolerance toward harsh environments (500°C in this study). Besides, the results suggest that a soft thermal annealing process could be adequate to achieve reliable working MOS-HEMTs with Gd_2O_3 dielectric.

ACKNOWLEDGMENTS

The work is supported by the Spanish Ministerio de Ciencia e Innovación, projects RUE (CSD2009-00046), CAVE (TEC2012-38247) and TEC2010-18051, and FPI grant (BES-2011-043798). The authors acknowledge Ms. Maria del Carmen Sabido and Ms. Alicia Fraile Chamizo for technical assistance.

REFERENCES

[1] U. K. Mishra, L. Shen, T. E. Kazior, and W. Yi-Feng, "GaN-Based RF Power Devices and Amplifiers," Proceedings of the IEEE, vol. 96, pp. 287-305, 2008.

[2] J. Das, J. Everts, J. Van den Keybus, M. Van Hove, D. Visalli, P. Srivastava, et al., "A 96% Efficient High-Frequency DC-DC Converter Using E-Mode GaN DHFETs on Si," Electron Device Letters, IEEE, vol. 32, pp. 1370-1372, 2011.

[3] S. Mizuno, Y. Ohno, S. Kishimoto, K. Maezawa, and T. Mizutani, "Large Gate Leakage Current in AlGaN/GaN High Electron Mobility Transistors," Japanese Journal of Applied Physics, vol. 41, p. 5125, 2002.

[4] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, and H. Zhou, "Temperature-dependent forward gate current transport in atomic-layer-deposited Al_2O_3/AlGaN/GaN metal-insulator-semiconductor high electron mobility transistor," Applied Physics Letters, vol. 98, p. 163501, 2011.

[5] X. Sun, O. I. Saadat, K. S. Chang-Liao, T. Palacios, S. Cui, and T. P. Ma, "Study of gate oxide traps in HfO_2/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by use of ac transconductance method," Applied Physics Letters, vol. 102, p. 103504, 2013.

[6] A. Laha, H. J. Osten, and A. Fissel, "Influence of interface layer composition on the electrical properties of epitaxial Gd_2O_3 thin films for high-k application," Applied Physics Letters, vol. 90, p. 113508, 2007.

[7] L. B. Chang, A. Das, R. M. Lin, S. Maikap, M. J. Jeng, and S. T. Chou, "An observation of charge trapping phenomena in GaN/AlGaN/Gd_2O_3/Ni–Au structure," Applied Physics Letters, vol. 98, pp. -, 2011.

[8] J. H. Leach and H. Morkoc, "Status of Reliability of GaN-Based Heterojunction Field Effect Transistors," Proceedings of the IEEE, vol. 98, pp. 1127-1139, 2010.

[9] D. Maier, M. Alomari, N. Grandjean, J. F. Carlin, M. A. Diforte-Poisson, C. Dua, et al., "Testing the Temperature Limits of GaN-Based HEMT Devices," Device and Materials Reliability, IEEE Transactions on, vol. 10, pp. 427-436, 2010.

[10] T. Y. Edward, "III-V Nitride Semiconductors: Applications and Devices" CRC Press, 2002.

[11] M. A. Pampillon, C. Canadilla, P. C. Feijoo, E. San Andres, and A. d. Prado, "High pressure sputtering as a viable technique for future high permittivity dielectric on III--V integration: GdO_x on InP demonstration," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, vol. 31, p. 01A115, 2013.

[12] M. A. Pampillon, P. C. Feijoo, E. San Andres, and M. L. Lucia, "Optimization of in situ plasma oxidation of metallic gadolinium thin films deposited by high pressure sputtering on silicon," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, vol. 31, p. 01A112, 2013.

[13] Y. V. Gomeniuk, "Determination of interface state density in high-k dielectric-silicon system from conductance-frequency measurements," Semiconductor Physics, Quantum Electronics & Optoelectronics, vol. 15, pp. 1-7, 2012.

[14] J. Donghyun and J. A. del Alamo, "Mechanisms responsible for dynamic ON-resistance in GaN high-voltage HEMTs," in Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium on, 2012, pp. 333-336.