Electrical characterization of MIS capacitors fabricated from ECR-PECVD silicon oxide and silicon nitride bilayer films

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In this study, a comparative electrical characterization of Al/SiN_x/Si and Al/SiN_x/SiO_2/Si MIS structures has been carried out. Both SiO_2 and SiN_x films have been deposited by using electron-cyclotron resonance plasma-enhanced chemical vapor deposition method. *C–V* results show that samples without SiO_2 have more defects than those with SiO_2. Deep-level transient spectroscopy and conductance transient measurements demonstrate that as for the samples containing the SiO_2 film, these defects are mostly concentrated in the insulator/semiconductor interface, whereas in the other case defects are spatially distributed into the insulator.

1. Introduction

In recent years great effort has been devoted to improve metal-insulator-semiconductor field-effect-transistor (MISFET) device performance and reliability. An important issue is the control of the metal/insulator interface quality, and therefore the development of new characterization techniques to carry out a detailed study of such interfaces.

In this paper we report the electrical characteristics of MIS capacitors with SiO_2/SiN_x gate stack dielectric layers. Results are compared with SiN_x gate layers, for different values of the dielectric film thickness. Both SiO_2 and SiN_x films have been deposited by using the electron-cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD) method, which has been proved to be a low-damage deposition process [1, 2]. Standard measurements, such as deep-level transient spectroscopy (DLTS), provide the energy distribution of interfacial state density, but they do not provide information about the spatial distribution. However, conductance transient analysis allows us to obtain three-dimensional defect maps, i.e., the energetical and spatial distribution of defects [3]. Our results reveal that the spatial distribution in the $SiN_x/SiO_2/Si$ interfaces is different from that in the SiN_x/Si ones. Whereas in the former case these defects are mostly concentrated in the insulator/semiconductor interface, in the latter they are spatially distributed into the insulator.

2. Experimental

2.1. Sample description

MIS devices were obtained as follows: substrates used were n-Si (5 Ω cm, (1 0 0) orientation), on which we have previously deposited Al back electrodes by thermal evaporation. After a cleaning step with organic solvents, we deposited a layer of silicon dioxide over one half of the samples by using the electron-cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD) method. The O_2 gas flux was 30 sccm during 3 h. The silicon dioxide thickness was around 9 nm. Then, all the samples underwent an ECR-PECVD $SiN_{1.44}$ film deposition. Gases employed in this deposition were N_2 (8.76 sccm) and pure SiH_4 (1.76 sccm), with three different deposition times (4 m 19 s, 8 m 38 s, and 12 m 57 s), in order to obtain three different thicknesses of silicon nitride (29, 50, and 74 nm). We thus obtained two samples of each silicon nitride film thickness: one with a silicon oxide layer deposited over the silicon substrate, and another one without it. Table I summarizes the silicon dioxide and silicon nitride thickness of all the samples. In all the ECR-PECVD depositions, chamber pressure and substrate temperature were kept at 100 W and 200 °C, respectively. Al dots (1.24×10^{-3} cm^{-2}) were thermally evaporated through a shadow mask as gate electrodes.

2.2. Electrical characterization

To study the interface quality of MIS structures, we have applied the following techniques: capacitance–

TABLE I Silicon dioxide and silicon nitride thickness

Sample	SiO_2 thickness (nm)	$SiN_{1.44}$ thickness (nm)
1A	9 nm	29 nm
1B	Without	29 nm
2A	9 nm	50 nm
2B	Without	50 nm
3A	9 nm	74 nm
3B	Without	74 nm

voltage (C–V), DLTS and conductance transient analysis.

C–V measurements were carried out at room temperature and at 77 K, with the sample in a light-tight, electrically shielded box. The measurement set-up involved a 1 MHz Boonton 72B capacitance meter and a Keithley 617 programmable electrometer. Both room-temperature and 77 K C–V curves obtained for all the samples clearly exhibit hysteresis phenomena, thus indicating that the interface-state distribution follows the well-known disorder-induced gap state (DIGS) model [4, 5]. According to this model, interface states are distributed both in energy and in space. Emission and capture of free electrons by states located in the insulator far from the interface can occur by means of tunneling mechanisms. As emission and capture kinetics are slow and not symmetrical, the capacitance value depends both on the direction and on the speed of the voltage variation and, thus, hysteresis effects are observed.

DLTS measurements, between 77 and 300 K, were carried out using an 1 MHz Boonton 72B capacitance meter and an HP54501 digital oscilloscope to record the capacitance transients. A Keithley 617 programmable electrometer is used together with an HP214B pulse generator to introduce the quiescent bias and the filling pulse, respectively. To obtain the interface-trap distribution within the forbidden gap, the bias voltage is chosen so that the MIS capacitor is just at the limit between depletion and weak inversion. Also, a 200-μs wide pulse high enough to drive the capacitors into accumulation is applied in order to fill all interface traps. The interface-trap distribution was deduced from DLTS measurements by means of the expressions reported elsewhere [6].

Moreover, we have measured conductance transients, which provide quantitative information about the disordered induced gap states. As we have published elsewhere [7–10], from the experimental conductance transients, we can obtain the DIGS state density as a function of the spatial distance to the interface and of the energy position. The experimental set-up consists of an HP 33120A arbitrary waveform generator to apply the bias pulse and an EG&G 5206 two-phase lock-in analyzer to measure the conductance. An HP 54501A digitizing oscilloscope records the complete conductance transient. Samples were cooled in darkness in an Oxford DN1710 cryostat. An Oxford ITC 502 controller was used to keep the temperature constant during the measurements.

3. Results and discussions

Fig. 1 shows 1 MHz–room temperature C–V curves obtained for all the samples, bias varying from accumulation to depletion. We can observe that samples

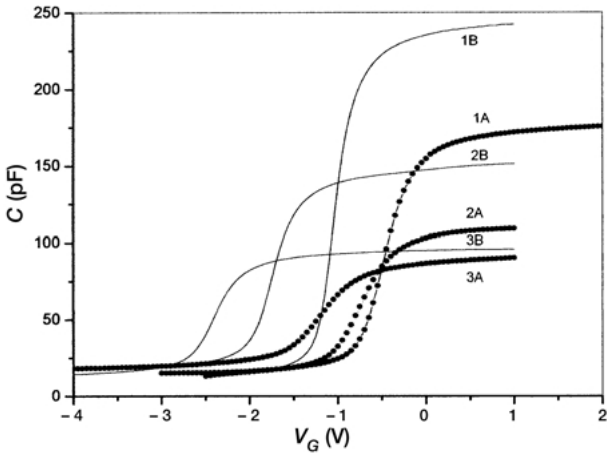

Figure 1 1 MHz–room temperature C–V curves obtained for the samples studied.

without any SiO_2 film exhibit larger flat-band voltage displacement than samples containing the SiO_2 film. Also, for both sets of samples, the thicker the silicon nitride film, the larger is the flat-band voltage displacement.

As for the interface trap distribution, Fig. 2 summarizes the results obtained by DLTS. We can see that samples without any SiO_2 film show a lower interfacial state density than the samples containing the SiO_2 film. On the other hand, for both sets of samples, the thicker the silicon nitride film, the lower is the interfacial state density.

These results seem to be contradictory, but conductance measurements help to clarify this subject. Indeed, Fig. 3 shows conductance transients measured at room temperature and 100 kHz. As the DIGS density is proportional to transient height, we can conclude that samples without any SiO_2 film have a higher DIGS density than samples containing the SiO_2 film.

Moreover, by recording conductance transients at several temperatures (between 200 and 300 K) and frequencies (between 100 Hz and 100 kHz), we can obtain the complete three-dimensional defect map of all of the samples. In Figs. 4 and 5 we show the maps corresponding to the samples with SiO_2 and without SiO_2, respectively. In these, the E_C–E' axis is referred to the semiconductor, i.e. negative values mean energies

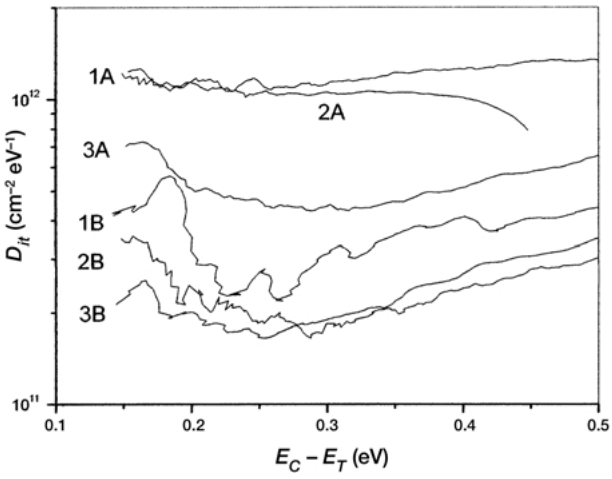

Figure 2 Interfacial state density obtained by using DLTS.

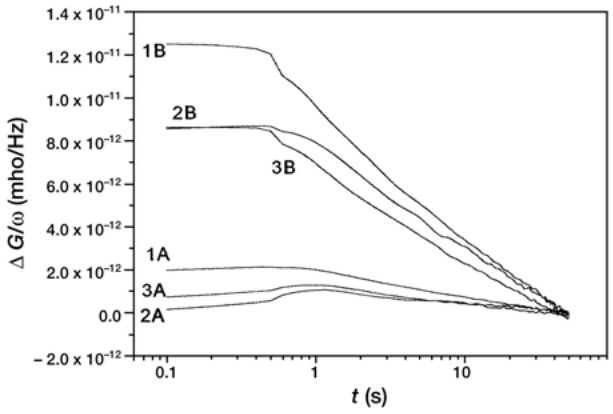

Figure 3 100 kHz–room temperature conductance transients.

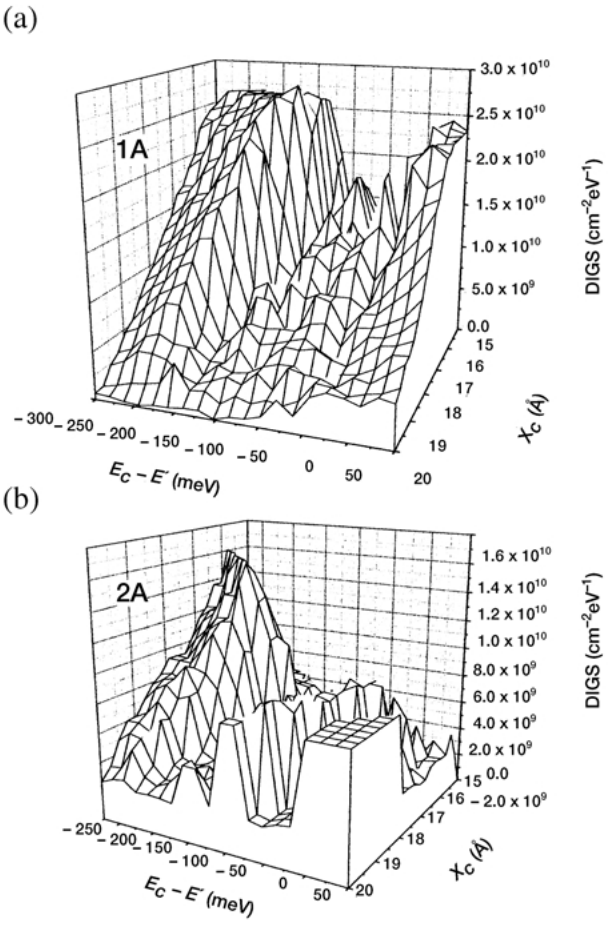

Figure 4 Three-dimensional defect maps corresponding to the samples $Al/SiN_x/SiO_2/Si$.

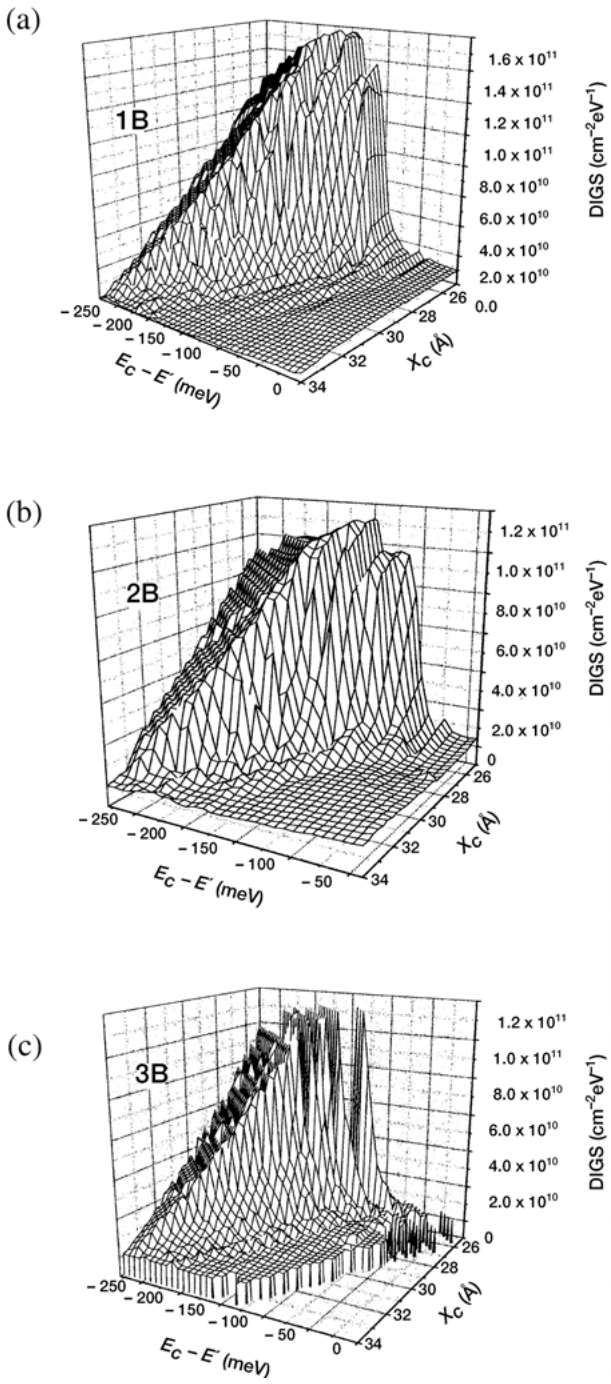

Figure 5 Three-dimensional defect maps corresponding to the samples $Al/SiN_x/Si$.

corresponding to the silicon conductance band. The X_c axis is the insulator depth measured from the interface. We can conclude that:

(i) In samples with SiO_2 DIGS states are spatially located very close to the Si/SiO_2 interface, and their energy positions belong to the silicon band gap.

(ii) In samples without SiO_2 the DIGS states are spatially located far away from the interface into the dielectric bulk, and their energy positions belong to the silicon conductance band.

(iii) In both sets of samples, the thicker the silicon nitride layer, the lower is the DIGS density.

(iv) The DIGS density is very much higher for samples non-oxidized than for the oxidized ones.

4. Conclusions

In this work we have electrically characterized silicon nitride-MIS structures fabricated on oxidized and non-oxidized silicon substrates. *C–V* results show that non-oxidized samples have more defects than the oxidized ones. DLTS and conductance transient measurements demonstrate that as for the oxidized samples, these defects are mostly concentrated in the insulator/semiconductor interface, whereas in the case of non-oxidized samples they are spatially distributed into the insulator bulk. These results demonstrate that the electrical characterization of MIS structures by using only DLTS measurements could induce erroneous conclusions, whereas conductance transient analysis provides a complete picture of DIGS distribution.

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