Single Events in a COTS Soft-Error Free SRAM at Low Bias Voltage Induced by 15-MeV Neutrons

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Abstract

This paper presents an experimental study of the sensitivity to 15-MeV neutrons of Advanced Low Power SRAMs (A-LPSRAM) at low bias voltage little above the threshold value that allows the retention of data. This family of memories is characterized by a 3D structure to minimize the area penalty and to cope with latchups, as well as by the presence of integrated capacitors to hinder the occurrence of single event upsets. In low voltage static tests, classical single event upsets were a minor source of errors, but other unexpected phenomena such as clusters of bitflips and hard errors turned out to be the origin of hundreds of bitflips. Besides, errors were not observed in dynamic tests at nominal voltage. This behavior is clearly different than that of standard bulk CMOS SRAMs, where thousands of errors have been reported.

Index Terms

COTS, LPSRAM, neutron tests, radiation hardness, reliability, soft error, SRAM

I. Introduction

MODERN electronic systems are designed to minimize power consumption. In standby mode, non-critical devices can be switched off, only keeping connected to the power supply the main parts of the system. However, the information inside CMOS memories is volatile so they cannot be switched off completely. It has been reported that static random access memories (SRAMs) can keep the information even if the bias voltage falls down to 15-20% of the nominal value [1]. Very often, the combinational logic that interacts with the memory cells does not work until the bias voltage returns to the nominal value. Nevertheless, the information does not disappear.

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The problem is that, as the bias voltage decreases, the critical charge to trigger a single event upset (SEU) decreases as well [2], [3]. This is also valid for other single events, such as multiple cell/bit upsets (MCU, MBU), etc., with the possible exception of the single event latch-ups (SEL). This fact has led to the demonstration that even electrons, the lightest charged particles, may provoke bitflips in 45-nm CMOS SRAMs at ultra-low bias voltage [1].

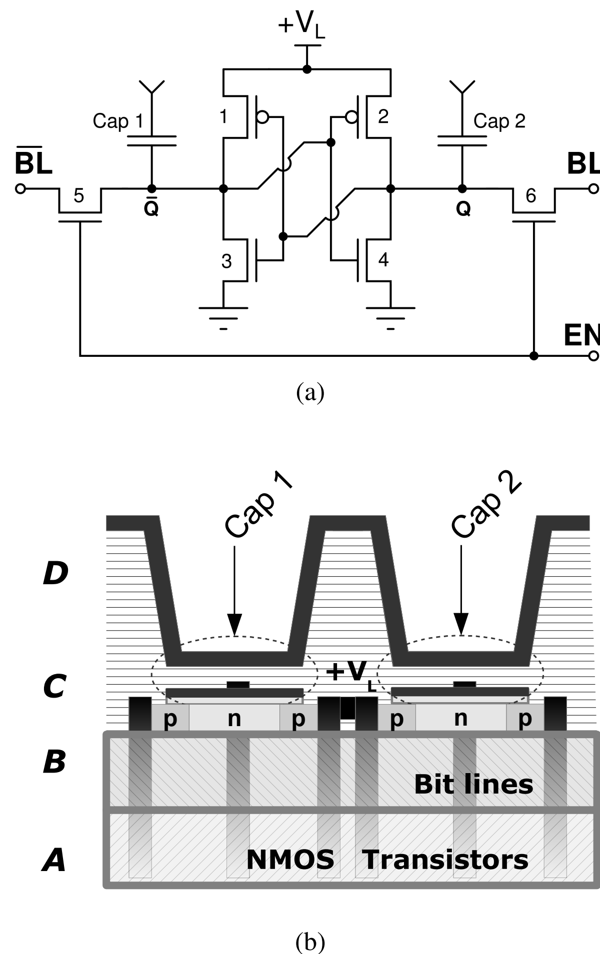


Figure 1. A typical 6T SRAM cell with extra capacitors (a). 3D-implementation of the circuit (b).

Recently, a new kind of SRAM has drawn the attention of different research groups. These memories, built by Renesas Electronics in 150-nm CMOS technology, are called Advanced Low Power SRAMs (A-LPSRAM) [4]. Devices in 110-nm are expected to be available within 2015-2016. Their main characteristic is that the individual 6-transistor cells are not built in planar technology but in a 3D structure (Fig. 1) with advantages such as the minimization of the cell area, the incorporation of capacitors that make less probable the occurrence of bitflips, and the removal of the parasitic *pnpn* structures prone to trigger latch-ups. According to [5], the value of the capacitors are on the order of 20 fF, and the common plate is ground. To the authors' knowledge, the first independent tests under radiation on A-LPSRAMs were performed at the NASA GSFC to investigate heavy ion effects [6]. Recently, the behavior of these memories under very energetic protons has been explored in order to propose its use in the CERN LHC upgrade [5]. Also, the memories were tested under 15-MeV neutrons at the GENEPI2 facility at nominal bias voltage [7].

However, the tolerance to radiation of these memories has not still been investigated in harder conditions such as low-bias

voltage or dynamic operation, where single events are easier to occur. As it was previously stated, bitflips are much more likely to occur when the circuit operates at ultra-low bias voltage, not far from the minimum power supply that allows the retention of data. Also, it has been demonstrated that typical static tests underestimate the cross sections, so dynamic tests are necessary [8]–[10] for a full understanding of the occurrence of single events.

This paper investigates the behavior of A-LPSRAMs under 15-MeV neutrons at bias voltages between a little above the minimum value, and the nominal bias voltage, both in static and in dynamic mode. The experimental setup is described in Section II, including details about the radiation facility. Section III is devoted to show the experimental results. Relevant phenomena are discussed in Section IV.

A short version of this manuscript was presented at the IEEE European Conferences on Radiation Effects on Components and Systems (RADECS 2015), held in Moscow (Russia) [11]. In the present version, more details about the experimental setup and results are offered as well as a much extended discussion about the underlying physical mechanisms.

II. Experimental Setup

Tests were carried out on one sample of an A-LPSRAM with a capacity of 8 Mbit built in 150-nm technology and configured as 1M×8 bits. According to the manufacturer, the nominal bias voltage ranges from 2.7 to 3.6 V. However, it was verified that even at 600-650 mV bias voltage, the information previously written was not lost. Besides, the combinational blocks were operational even with a bias voltage value as low as 1.9 V. Below this value, the read-out system does not work.

A. Description of the GENEPI2 Neutron Source

The GEnerator of NEutrons Pulsed and Intense (GENEPI2) is under operation at LPSC (Laboratoire de Physique Subatomique et de Cosmologie) in Grenoble (France) [12], [13]. This accelerator, originally developed to produce neutrons for nuclear physics experiments, was used for the first time in 2013 to irradiate different types of SRAMs.

GENEPI2 is an electrostatic accelerator producing neutrons by impinging a deuteron (ions of Deuterium ($^2_1$H)) beam onto a fixed target. The target contains either Tritium ($^3_1$H or T) or Deuterium ($^2_1$H or D) according to the required neutron energy. After acceleration, ions of Deuterium (d) produce neutrons by one of the following processes:

- d + T $\rightarrow$ n + ^{4}He
- d + D $\rightarrow$ n + ^{3}He

An ion source, held at high voltage, generates the deuteron beam by ionizing Deuterium gas. The beam is shaped by a series of electrodes, and then accelerated at 250 kV through an accelerating column. After magnetic selection by a dipolar electromagnet, deuterons are guided through a $\sim$ 5 m long transport line, including focusing and steering elements. The beam line terminates with the target made of a Tritium or Deuterium compound.

From the target, the neutrons spread in all the directions. When using tritium, the average neutron energy is 14.2 MeV. For our radiation campaigns, we only consider, to first approximation, the neutrons emitted forward. In this case, the neutron energy is maximal at 15 MeV.

Neutrons are emitted from the target in the whole accelerator room. The topside of the SRAM to irradiate is set facing directly the target at a distance determined to match the required neutron flux. Further neutron flux adjustments can be made by

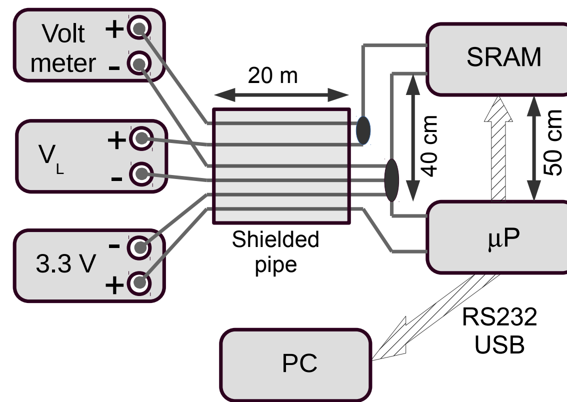


Figure 2. Schematic of connections and length of the cables. A 100-μF capacitor was placed between the power supply and ground in the microcontroller board, and a smaller one (100 nF) in the SRAM board. The cable shield was connected to the ground output of the 3.3 V power supply.

varying the average beam intensity on target. While the SRAMs are fully exposed to neutrons, the readout electronic platform is protected by a dedicated neutron shielding.

Neutron production is monitored throughout the experiments to determine the neutron dose for each irradiation. Early 2015, a fresh tritium target was installed, generating a maximum neutron flux of 4.5 $\times$ 10^7 $n \cdot cm^{-2} \cdot s^{-1}$. Under these conditions, Devices Under Test (DUTs) are exposed to a fluence of 1.6 $\times$ 10^{11} $n \cdot cm^{-2}$ within one hour.

B. Test system

The memory was written and read by means of a PIC18F85J90 microcontroller. This microcontroller used a 20-MHz quartz clock and, experimentally, it was observed that it could work even with a bias voltage of 1.9 V.

In the low-bias voltage static tests, the microcontroller and the SRAM were biased by two independent power supplies. That of the microcontroller was fixed to 3.3 V, and that of the SRAM was tunable from 0 to 3.3 V. The SRAM bias voltage was measured with a Keithley 2001 multimeter directly at the memory board. The three grounds (two for the power supplies, and one for the multimeter) were connected near the SRAM board for an accurate measurement. That means that six shielded cables, with a length of 20-m each, were necessary to build the electronic system (Fig. 2).

In low-bias voltage static tests, address and data buses, as well as enable signals of the SRAM were set to ground in order to avoid the activation of over-voltage protection structures present in the memories. Thus, a 0x00 word was always written in the first address of the memory, 0x00000, no matter the pattern was. Let us bear in mind that only 8 bits were sacrificed in a memory with 8 Mbits and that it also allows testing and debugging the capacity to detect the bitflips.

It is important to highlight that the reading and writing processes were always performed at 3.3 V independently of the value of the power supply biasing the SRAM during the low-bias voltage tests. The microcontroller board and the SRAM were no more than 50 cm away from each other.

Initially, it was intended to perform tests with several patterns. However, as the tests were included in a larger campaign of experiments, it was decided along the way to focus the tests on the classical checkerboard pattern, 0x55, due to logistic reasons. Thus, most of the data on the static tests shown in the paper were obtained with this pattern.

Within the same 15-MeV neutrons neutron tests campaign, other two bulk CMOS SRAMs from a different manufacturer, in 90 & 130-nm technologies, were tested in identical conditions and with the same test set-up as the Renesas devices. As the behavior of this family of devices under neutron radiation has been thoroughly studied and results presented in this paper agreed with those reported in the literature [14], [15], we concluded that the measurement system was correctly designed and mounted so the results presented in this paper are not due to bugs in the test setup.

Previously, it was verified that data were correctly retained in the SRAMs after one hour observation at 0.70 V. Thus, bitflips observed in the experiments are related to 15-MeV neutrons neutron radiation and not to other effects.

Table I
TIME SEQUENCE OF THE IRRADIATIONS

Round	Pattern	Kind	V_L	Fluence	Corrupted addresses
A	0x00	Stat.	0.70	2.04	342
B	0x55	Stat.	0.80	2.04	131
C	0x55	Stat.	0.90	2.04	1
D+E	0x55	Stat.	1.00	6.11	0
F	0x55	Stat.	0.70	2.04	130
G	0x55	Stat.	0.75	2.05	338
H	0x55	Stat.	0.85	2.04	312
I	N/A	Dyn.	3.30	0.68	Aborted
J	0x55	Stat.	0.90	4.07	5
K	0x55	Stat.	0.85	2.04	129
L	0x55	Stat.	0.80	2.05	132
M	0x55	Stat.	0.75	2.04	134
N	0x55	Stat.	0.70	2.04	133
O	0x55	Stat.	0.95	6.11	2
P	N/A	Dyn.	3.30	4.28	0
Q	N/A	Dyn.	2.20	4.28	0
			V	$\times 10^9\ n/cm^2$	

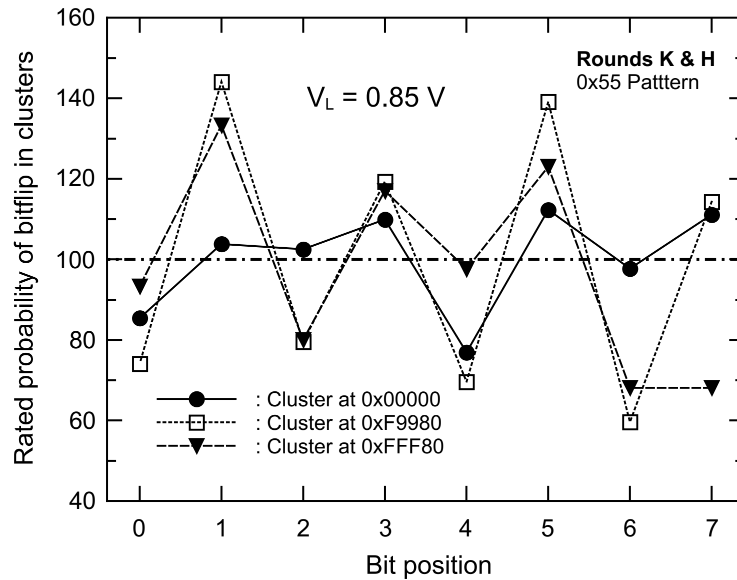
III. RESULTS

As shown in Table I, the tests were performed in successive steps. As there was not any hint to predict the behavior of the memories with ultra-low bias voltages, the irradiations were performed in long steps, next choosing intermediate values, and eventually repeating voltage values at the end of the experiments.

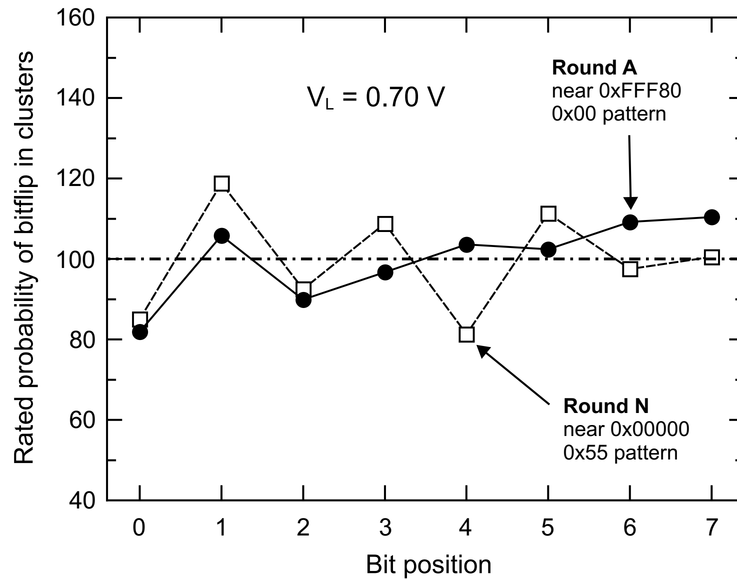
Table I shows the total number of addresses, containing from one to eight bitflips, that were detected in each round. One can see that, at very low voltage values, the content in hundreds of addresses are corrupted, either with single bitflips or with MBUs. To the authors' opinion, detected errors fall in three categories: clusters of bitflips, hard errors at low bias voltage, and SEUs.

A. Static low bias voltage tests

1) Clusters of bitflips: Test rounds with hundreds of bitflips are characterized by the occurrence of ”clusters of errors” (rounds A-B, F-H, K-N). It is necessary that the bias voltage be 0.85 V or below. The corruption of words occurs as simple



(a)



(b)

Figure 3. Probability of a bit to flip in addresses within clusters. (a) shows that bits in odd positions are more likely to switch with 0x55 pattern, above all in clusters near the end of the address vector. (b) shows that the 0x00 pattern does not contain the saw-shape observed with 0x55.

bitflips or MBUs of diverse multiplicity, and concentrated in very close logical addresses. In particular, the distance between the lowest and highest logical address of each cluster is around 128. Even more, upper and lower boundaries are close to consecutive integer multiples of 128 (e.g., in Round A, $0\text{x}F9980 = 7987 \times 128$ and $0\text{x}F99FF = 7988 \times 128 - 1$). Table II shows the characteristics of the clusters observed with bias voltage of 0.85 V. In Round H, four clusters of different sizes and with errors of multiplicity up to 7 were registered starting in different logical addresses and finishing near the end of the logical address vector. In Round K, in spite of the fact that the external parameters (bias voltage and pattern) were identical to those of Round H, the cluster appeared at the beginning of the memory. In our experiments, clusters only appeared at the

beginning or near the end of the logical address vector and intermediate logical addresses were not observed. Finally, clusters were never simultaneously observed at both regions in the same round.

The occurrence of clusters seems to be independent of the pattern. Table III demonstrates that they can be observed either with 0x00 or 0x55 patterns. The comparison of both tables puts in evidence another interesting characteristic: the clusters near the end of the address vector share the boundaries indicating that only some blocks of 128 words are prone to undergo this phenomenon. Only at 0.75 V a fifth cluster near the end was observed between 0xFEB80 and 0x$FEBFF$ addresses.

Another interesting feature of the clusters is that the position of the flipped bits depends on the pattern and cluster location. In every cluster of bitflips, it was determined the position of the flipped bits in the affected addresses and was calculated the number of times that positions from 0 (LSB) to 7 (MSB) appeared, n_k, $k \in [0, 7]$. Later, the mean value of expected bitflips was calculated, $\bar{n} = \frac{1}{8}\sum n_k$ as well as the normalized probability of a position to be flipped, $n_k/\bar{n}$, (Fig. 3). In Fig. 3(a), saw-shaped lines associated with clusters near 0x$FFFFF$ indicate that bits in odd positions of the 8-bit word are more likely to flip than those in even ones. This behavior seems to appear also in the clusters around 0x00000 but the difference between peaks and valleys seems to be not so significant.

Fig. 3(b) compares the bitflip probability with different patterns at 0.7 V. The saw-shaped line appears again with checkerboard pattern but little deviation from the mean value is observed with the all-zeroes pattern, with the possible exception of the least significant bit, 0. This behavior could be related to that presented in [5], where it was reported that transitions from 0 to 1 were 25% more likely than the opposite in irradiations with high-energy protons at nominal voltage. Indeed, our results show clear coherence with the results presented by those authors.

2) Hard errors at low bias voltage: An off-line study of the addresses where bitflips occurred showed that some of them reappeared from round to round. For example, it was observed that, from round K and below 0.90 V, the word stored in 0x$4D69C$, supposed to be 0x55, systematically changed into 0x$D5$, behavior not observed in the pristine memory. It is important to clarify that these addresses did not belong to clusters of bitflips. This unexpected phenomenon led to study the memories after the irradiation. Thus, the memory was checked at the nominal voltage writing the 0x55 pattern and reading the information, and these addresses seemed to work correctly. However, if the bias voltage falls to 0.7 V, bitflips in the problematic addresses appeared again. Besides, after changing the pattern to 0x00 and 0xFF, other problematic addresses were observed. In particular, this phenomenon was observed in seven addresses of the memory (Table IV), in all cases only one bit in every 8-bit word being affected.

Table II
CHARACTERISTICS OF CLUSTERS OF BITFLIPS WITH $V_L = 0.85\,V$ AND PATTERN OF 0X55

Round	Start	End	Affected addresses	Addresses with $1 \le N \le 8$ flipped bits								Total bitflips
				1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	
H	0xF9980	0x$F99FF$	94	41	41	10	2	0	0	0	0	161
H	0xFE982	0x$FE9FF$	55	47	7	0	1	0	0	0	0	65
H	0xFF180	0x$FF1FC$	35	29	6	0	0	0	0	0	0	41
H	0xFFF80	0x$FFFFE$	127	2	9	27	34	31	20	4	0	540
K	0x00001	0x0007F	127	1	4	12	26	27	34	17	6	655

The error identified as address #6 in Table IV was not detected during the radiation tests since the checkerboard pattern, 0x55, is not altered. Besides, errors identified in addresses #2 and #7 should have been detected in the tests but they were not. The authors believe that the bit was affected during the last rounds, when dynamic tests at nominal voltages were performed. The more interesting fact is that when the memory was checked one week after the end of the tests, addresses called #3 and #4 in Table IV worked fine. This fact indicates the existence of some kind of annealing.

These hard errors are quite similar, but not equivalent, to the well-known stuck bits, in which the information inside the bit cannot be changed, with the difference that they only occur if there is a cycle of low bias voltage.

3) Single event upsets: Once the bitflips appearing in clusters of errors and those present in different radiation rounds were removed, there was a set of bitflips with characteristics agreeing with those expected in single event upsets: isolation, randomness, occurrence in only one round, etc. Therefore, in spite of the fact of lacking information about the physical SRAM structure, the authors believe that they must be classified as SEUs, kind of event already observed by other authors [5], [6]. Curiously, this kind of events was not the main contribution to the whole set of errors. For instance, only 4 SEUs were detected combining the two rounds at 0.7 V, the worst-case situation, with a 0x55 pattern (Rounds F and N). In round A, the only one with this bias voltage of 0.7 V and 0x00 pattern, the results were similar: only 3 out of 342 bitflips could be considered as SEUs.

Fig. 4 shows the dependence of the SEU cross-section with the bias voltage for the 0x55 pattern. As the number of errors is not high, error bars are wide and little information can be obtained. The linear fit of the dots indicates that the cross section decreases for higher values of the bias voltage, as usually happens in other SRAMs. However, the error margin is too large ($\frac{d\sigma}{dV_L} = (-2.8 \pm 4.2)\ cm^2 \cdot V^{-1}$) to conclusively state that this behavior occurs. Above 1 V, no SEUs were observed. Using the procedure explained in [7] and references therein, the conclusion is that for this kind of radiation the SEU cross-section for 15-MeV neutrons at $V_L = 1\ V$ is below $7.2 \cdot 10^{-17}\ cm^2/bit$ with 95%-confidence. This figure reduces in more than one order of magnitude the first estimation presented in a previous work, $2.0 \cdot 10^{-15}\ cm^2/bit$ at $V_L = 3.3\,V$ [7]. In this value, possible undetected MCUs are included.

Due to the scarcity of samples, it is not suitable to assert if both transitions ($0 \rightarrow 1$ and $1 \rightarrow 0$) are equiprobable for 15-MeV neutrons or the $0 \rightarrow 1$ transition is enhanced 25% as reported in [5] for high energy protons.

Table III
CHARACTERISTICS OF CLUSTERS OF BITFLIPS WITH $V_L = 0.70\ V$ AND PATTERN OF 0X00 (ROUND A) OR 0X55 (ROUNDS F, N)

Round	Start	End	Affected addresses	Addresses with $1 \leq N \leq 8$ flipped bits								Total bitflips
				1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	
A	0xF9980	0xF99FF	98	0	6	29	28	25	10	0	0	396
A	0xFE981	0xFE9FF	70	0	4	25	11	27	3	0	0	280
A	0xFF180	0xFF1FC	42	0	1	19	3	16	3	0	0	169
A	0xFFF80	0x$FFFFF$	128	1	5	28	47	28	17	2	0	539
F	0x00000	0x0007F	128	2	7	16	27	28	37	9	2	613
N	0x00001	0x0007F	127	0	7	16	18	35	31	15	5	640

Table IV
ADDRESSES WITH CORRUPTED INFORMATION AT 0.7 V AND OFF-LINE

Written Pattern	Address	Read Word	First Det.	Id.
0x00	0x4D69C	0x80	Round K	#1
	0x8BAE7	0x08	Off-line	#2
	0x9CE7B	0x02	Round J	#3
	0xC27AC	0x80	Round M	#4
	0xEDD7F	0x80	Round L	#5
0xFF	0x31BD9	0xF7	Off-line	#6
	0x42FE3	0xFE	Off-line	#7

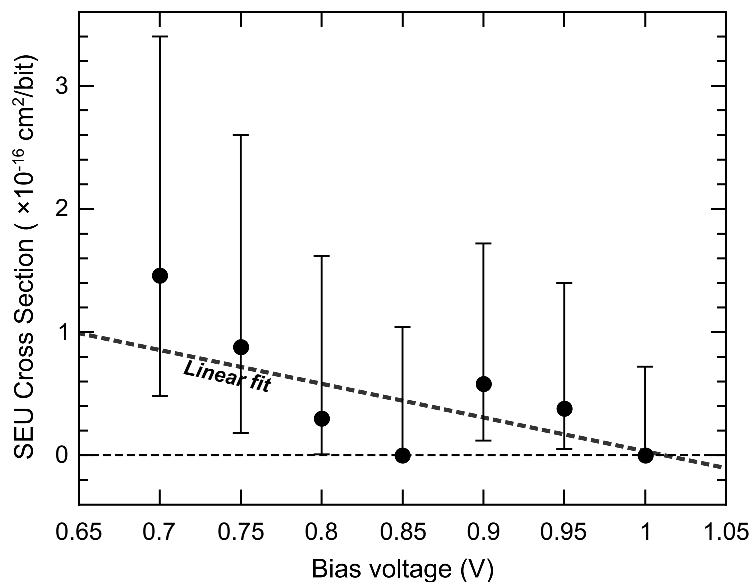


Figure 4. 15-MeV neutrons cross-section for the A-LPSRAM at ultra-low bias voltage for classical SEUs (neither clusters nor hard errors included). Error bars were calculated with 95%-confidence from the number of events using the standard technique shown in [7], [16]. If MCUs had occurred, they would have been included in the cross section values.

B. Dynamic tests

Dynamic tests were also carried out. Read and write operations were performed while the memory was irradiated. The MARCH-C algorithm was executed during these tests [10]. It is a well-known algorithm that, as indicated in Eq. 1, comprises 6 consecutive elements that involve reading (r) or writing (w) 0's or 1's in the memory:

$$\begin{gathered}\{\uparrow (w0); \uparrow (r0, w1); \uparrow (r1, w0); \\ \downarrow (r0, w1); \downarrow (r1, w0); \uparrow (r0)\}\end{gathered} \tag{1}$$

The elements that comprise two operations (for instance, $\uparrow (r0, w1);$) indicate that the memory positions are overwritten with 0's or 1's immediately after they are read. The arrows indicate if the memory is read or written in an ascending or descending order.

Dynamic tests at 3.3 V and 2.2 V were carried out until reaching a fluence of $4.28 \times 10^9\ n/cm^2$. The latter value was used instead of the threshold one of 1.9 V in order to prevent the microcontroller from slowing down. No errors were observed during these tests. As stated in Section III-A3, the conclusion is that the cross section is below $1.0 \cdot 10^{-16}\ cm^2/bit$ for this

phenomenon under 15-MeV neutrons.

IV. Discussion

A. Classical SEUs

In a previous work, it was concluded that the 15-MeV neutrons SEU cross section in A-LPSRAM memories was two orders of magnitude below those of its counterparts in bulk CMOS technology [7]. However, as other authors have reported SEUs with protons and heavy ions [5], [6], it was likely that SEUs appeared at low values of bias voltage since there is evidence that, at least in bulk CMOS memories, the cross section exponentially grows as the bias voltage approaches the minimum value [17]. Our results provide hints of this dependence on the bias voltage values near 0.65 V but by no means as dramatical as in bulk CMOS memories. As a conclusion, A-LPSRAMs can be safely used with 1-V bias voltage in systems exposed to neutron radiation below 15-MeV neutrons.

Fig. 5 shows the threshold injected charge value, obtained from SPICE simulations, required to trigger a SEU. SRAM cells were modeled using BSIM49 SPICE models of CMOS transistors freely available on the MOSIS website [18]. As at the time of writing this manuscript there was not information about 150-nm technologies, we decided to investigate 130 & 180 nm, believing that the behavior of the 150-nm devices must be somewhere between those of both families. The transistors were modeled with minimal channel length values and the PMOS width three times that of the NMOS to center the switching voltage. The capacitors were supposed to be of 20 fF, as stated in [5]. Simulations were run on NGSpice 26, a free BSD-licensed fork of SPICE 3f5 [19]. Current sources emulating the neutron hit connected the ground node and the drain of the NMOS transistor in the inverter with HIGH output, in OFF state. Besides, the current sources were modeled using the technique shown in [20].

Interesting information is provided by Fig. 5 to explain the absence of exponential growth near the minimum bias voltage value. Apparently, the addition of a capacitor increases two or three times the threshold charge to trigger a SEU. For example, the ratio between the values of the stored charge with and without capacitors is 1.80 in the 130-nm cell at 3.3 V. But this ratio increases to 4.7 at 1.0 V, where both cells are fully operative. However small this growth may seem, it is an achievement that makes the occurrence of SEUs at ground level much more difficult. According to O'Bryan [6], the linear energy transfer (LET) threshold for heavy ions is ~ 1.7 MeV/cm^2/mg, which is above the maximum LET value of ions issued from the decay of radioactive impurities, thermal neutrons, etc. (~ 1.4 MeV/cm^2/mg [7]).

The SEU tolerance of A-LPSRAM even at very low bias voltage values can be explained as follows. Fig. 6 shows the physical structure of a CMOS inverter with LOW input and HIGH output. The single event transient (SET) that would eventually lead to the bitflip is a current pulse between the drain of the OFF NMOS transistor and its bulk, connected to ground. The current pulse must remove the charge stored in capacitances near this node, mainly the gate-drain of the PMOS transistor in linear zone. In [21], it is postulated that the injected critical charge to provoke a SEU is:

$$Q_{CRIT} \approx \frac{1}{2} \cdot C_{node} \cdot V_L + I_r \cdot \tau_{flip} \quad (2)$$

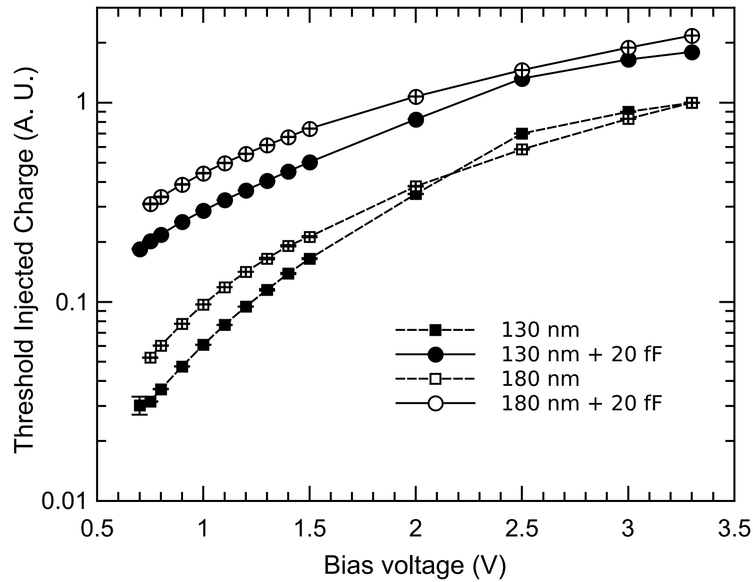


Figure 5. Injected charge vs. power supply with and without capacitors. For both technologies, the injected charge to trigger the SEU at $V_L = 3.3\,V$ without capacitors is supposed to be 1.

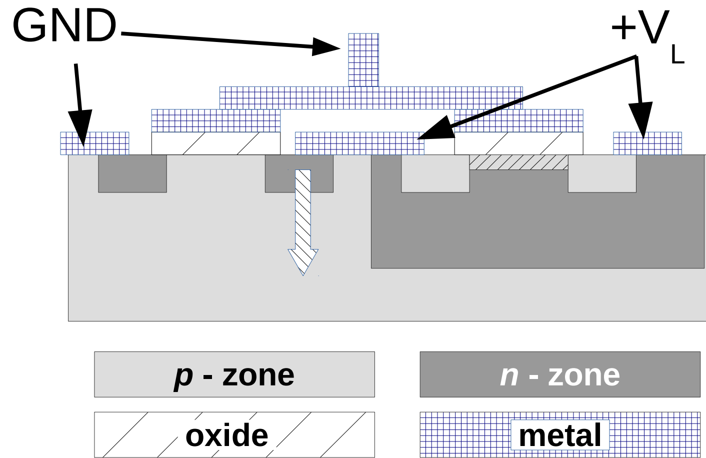


Figure 6. Schematic of a CMOS inverter with LOW input. Actually, this is more a planar structure than a 3D device similar to that of Fig. 1 but, for illustrating purposes, we have chosen this structure since it is easier to visualize.

C_{node} being the equivalent capacitance at the hit node, I_r the restore current coming from the PMOS transistor, and τ_{flip} the required time to switch the cell state. The value of I_r must be proportional to the PMOS transistor conductance, $g_m \propto (V_L - |V_{TH,P}|)$. The problem in Eq. 2 comes from the fact that the critical charge would only vanish near $V_L = 0$ and not near the minimum power supply, $\sim 0.6 - 0.65\,V$, as Fig. 5 shows. One way to solve this question consists in supposing that the main contribution to the node capacitance is the PMOS gate-to-drain capacitance in linear mode, in which the stored charge is proportional to $V_L - |V_{TH,P}|$. Another contribution to the node capacitance such as the reverse-biased PN junction between the NMOS drain & bulk is proportional to V_L, but is probably negligible. Thus, Eq. 2 becomes:

$$Q_{CRIT} \approx$$

$$\frac{1}{2}\left(C_{node,1}\cdot\left(V_L-|V_{TH,P}|\right)+C_{node,2}\cdot V_L\right)+I_r\cdot\tau_{flip} \quad (3)$$

and this expression approaches 0 when $V_L \sim 0.6 - 0.65\ V$ if $C_{node,1} \gg C_{node,2}$. This explains the fact that bitflips are more likely to occur with low values of the power supply. On the contrary, in the A-LPSRAM cells, the charge accumulated in the protecting capacitor is $C_P \cdot V_L$, C_P being 20 fF in SPICE simulations. This capacitor increases the value of $C_{node,2}$, making it no longer negligible so, even near the minimum power supply, the charge to be removed is still significant. Finally, it is important to note that the collection volume is roughly the depletion zone between the NMOS drain and bulk, which is a reverse biased PN junction with a width proportional to $\sqrt{V_L + V_{BI}}$, V_{BI} being the built-in voltage around 0.6-0.7 V. This fact partially compensates the decrease of the critical injected charge in both kinds of cells.

B. Radiation Tolerance in Dynamic Tests

Another interesting feature of this family of memories is the absence of errors during dynamic tests. As the system was controlled by a microcontroller with a 20-MHz clock, it was not possible to make the SRAMs work near their speed limit as suggested in [9], [10]. In practice, work frequency is about 5 MHz but not higher. However, it was observed in our experiments that speed was not the main factor but the activation of the logic structures that allow controlling the array of memory cells. Thus, in the same 15-MeV neutron radiation campaigns, some SRAMs in 90-nm bulk CMOS technology showed thousands of events when they were tested in identical conditions to those of the A-LPSRAMs. This good robustness in the dynamic test can be attributed to the absence of physical structures prone to trigger microlatchups. As mentioned in Section I, one of the advantages of the 3D-structure of the A-LPSRAMs is the removal of *pnpn* paths where latch-up (destructive or microlatchup) originates. According to [9], [10], multiple events observed in dynamic tests can be classified into, at least, four categories. In these works, one of the categories is called Type-B MCUs and it appears after the occurrence of a microlatchup that propagates along a block containing an array of memory cells. As the block is isolated from the rest of the device by some sort of physical barriers, the latchup does not destroy the device and it is observed as sets of some tens of events. As A-LPSRAMs are immune to microlatchups, this phenomenon cannot occur. In fact, they behave as magnetorresistive random access memories (MRAM), in which 6-T CMOS memory cells are replaced by magnetorresistive cells, in such a way that CMOS technology is restricted to the much smaller peripheral combinational blocks and where bitflips have never been observed neither in static nor in dynamic tests [8], [22].

Other exotic errors reported in the dynamic tests related to the occurrence of single event functional interrupts (SEFIs), called Type-C and Type-D MCUs in [9], were not observed for the A-LPSRAM. Whether this absence of SEFIs in dynamic tests is inherent to the A-LPSRAMs or that 15-MeV neutrons neutrons are not energetic enough cannot be asserted.

C. Origin of the Hard Errors

Hard errors at low voltage share some properties with standard stuck bits. Like these well-known hard errors [23], those observed in the A-LPSRAMs vanish days or weeks after the irradiations, and whichever information is written, the bit ends up returning to a stable value. Nevertheless, differences are also evident making inappropriate their classification as “stuck bits”:

errors keep latent until a low bias-voltage cycle. Also, it is not possible to deduce from the results if the number of errors is proportional to the accumulated neutron fluence.

In the authors' opinion, the hard errors reported in this paper and classical stuck bits share a similar origin: microdose effects [24]. Indeed, it is easy to demonstrate that the CMOS inverters inside a SRAM cell only work if

$$V_L > V_{THN} + |V_{THP}| \tag{4}$$

V_L being the power supply value, and V_{THX} the threshold voltages of the transistors in the inverters. This relation is deduced from the fact that SRAM cells are made up of CMOS inverters, and in this structure the bias voltage must be high enough to prevent both transistors from being simultaneously OFF. Typically, microdose effects occur with heavy ions, but secondary ions generated after the collision of a neutron with silicon nuclei have similar ionizing properties. It is well-known that the negative threshold voltage of PMOS transistors always decreases but, in the case of the NMOS, the positive threshold voltage increases or decreases depending on several physical parameters.

Therefore, if the absolute value of the threshold voltage of one of the transistors increases, the minimum bias voltage for the affected cell locally grows. As the power supply decreases down to a value very close to the minimum value for pristine devices, even a shift of some tens of millivolts in Eq. 4 for one specific cell throws it outside the safety region. Thus, during the low bias voltage cycle, the affected cell is switched off, losing the stored information and when the bias voltage returns to the nominal value, the cell goes to the preferred state after powering up, that can be the same as the original written bit or not. In this last case, a bitflip would be observed.

D. Cluster of bitflips as SEFIs

Due to the absence of information about the way the memories are built, the mechanism leading to the appearance of clusters of bitflips is not fully understood. As the reading and writing steps were performed at 3.3 V, the malfunction of the sense amplifier is not the reason of this error. However, the omnipresence of 128 indicates that the memory may be organized in blocks of 128 8-bit words (1024 bits) and this casts light about the origin of the phenomenon.

A good strategy to find out the origin of the clusters is to find equivalent phenomena in the literature, mainly in the works by Tsiligiannis [9], [10]. The first idea is to compare the clusters of bitflips with the Type-B MCUs, already depicted in Section IV-B, and related to the propagation of micro latch-ups eventually stopped by the borders of the block. However, in other technologies, latch-ups usually appear only at high values of bias voltage, exactly the opposite behavior observed in the A-LPSRAMs. Moreover, A-LPSRAMs are supposed to be latchup-free. Also, it was not necessary to switch the memory off to make it working properly again.

One possibility is that, if every block is biased by its own driver, single event transients can lead to a spurious decrease in the bias voltage of the block that erases the stored information. This is roughly equivalent to the Type-D MCUs observed in [9], [10], which were attributed to drops in the power lines. The difference is that Type-D events in bulk CMOS SRAMs were supposed to be caused by transient drops in the local power supply value after the occurrence of microlatchups. But as microlatchups do not occur in A-LPSRAMs, the voltage drops would be the result of other phenomena, such as, e. g., single

event transients in the drivers of the power lines. This may explain why clusters do not occur above $0.85\ V$ since even the largest transients would not reach the threshold value to delete the information in the cells. This mechanism clearly explains the dependence on the pattern depicted in Fig. 3. After the transient, the erased cell returns to its preferred or natural state. If there are more cells with a preferred state of 1 than with 0, those cells previously written with 1 are more liable to return to a value that coincides with the original content. Thus, they would be never detected as bitflips and, apparently, the error rate with 1 would be lower than otherwise. With the 0x55 pattern, 1s are in even positions explaining the saw-shaped lines in the graph. At any rate, other explanations can be proposed.

It is likely that the row & column decoders play an important but not understood role in this phenomenon. In other memories in the range of several Mbits and from the same manufacturer, the datasheets indicate that 7 address bits ($2^7 = 128$) are used for the column decoder, leaving the rest for the row decoder. The abundance of clusters in the addresses between 0x00000 and $0x000EF$ and around $0xFFFFF$ could be related to the fact that the address bus was set to 0x00000 in the experiments. Further work should be done to elucidate the characteristics of this phenomenon.

V. Conclusions

This paper has presented experimental evidences of the sensitivity to 15-MeV neutrons of an 8-Mbit A-LPSRAM, manufactured in 150-nm CMOS technology by Renesas Electronics, when powered up at low bias voltage. Results issued from radiation ground tests confirmed that, above 1 V, the memory has a cross section lower than $7.2\times10^{-17}\ cm^2/bit$ with a 95%-confidence. Below that voltage, new kinds of errors were identified: clusters of bitflips in groups of addresses whose first and last elements were approximately and never more than 128 positions away, and hard errors that were only visible at low voltage, even when the memory is no longer exposed to radiation.

These experiments should be completed in the future with similar experiments with other kinds of radiation, such as high-energy neutrons or heavy ions. At any rate, they have demonstrated that the behavior of the A-LPSRAM memory is different to classical bulk CMOS devices in similar test conditions.

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