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Interface quality study of ECR-deposited and rapid thermal annealed silicon nitride Al/SiN_x:H/InP and Al/SiN_x:H/$In_{0.53}Ga_{0.47}As$ structures by DLTS and conductance transient techniques

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Abstract

In this article, we study the influences of the rapid thermal annealing temperature and dielectric composition on the electrical characteristics of ECR-deposited silicon nitride SiN_x:H–InP and SiN_x:H–InGaAs interfaces. *C–V*, deep level transient spectroscopy (DLTS) and conductance transient analysis have been applied. As for InP cases, DLTS results reveal that rapid thermal annealing application increases interfacial state density. In contrast, transient conductance measurements show that disorder induced gap-state (DIGS) damage density diminishes when RTA is applied. So, we can conclude that RTA treatments take out the insulator damage to the interface. In the InGaAs-n cases, we have observed that DIGS damage evolution with RTA temperature is opposite to the interfacial state density. This behaviour seems to suggest some temperature activated defect exchange between the insulator and the interface. Finally, as for the insulator composition influence on the interface quality of the InGaAs-n samples, DLTS results suggest that the intermediate x values (1.43 and 1.50) provide better interfaces than extreme x values. Conductance transient measurements add complementary information: insulator damage increases when x increases. Hence, $x = 1.43$ seems to be the best choice to improve the overall interface quality.

1. Introduction

The fabrication of III–V materials, metal–insulator–semiconductor structures to be used in field-effect transistors presents some problems related to insulator–semiconductor interface quality. In this sense, it is crucial to use a growth dielectric technique, which minimizes damage effects on a semiconductor surface, as electron cyclotron resonance plasma enhance chemical vapour deposition (ECR-CVD) [1,2]. In our previous works, we have demonstrated that this is a suitable method to obtain excellent SiN_x:H–InP and SiN_x:H–$In_{.53}Ga_{.47}As$ interfaces. We have also reported on the use of rapid thermal annealing treatments to improve interface quality [3–6].

2. Experimental

MIS-InP structures were obtained by using 5×10^{15} cm^{-3}-unintentionally doped n-type (1 0 0) InP wafers. Gases employed in the insulator deposition vacuum chamber were N_2 and pure SiH_4, with two different values of the flux gases ratio. We have obtained 500 Å-thick SiN_x films with two different insulator composition values, $x = 0.97$ and $x = 1.43$. Substrate temperature was 200°C during the process. After deposition, argon-atmosphere RTA processes were carried out for 30 s at temperatures varying between 400 and 700°C. Finally, Al dots were thermally evaporated on the top layer,

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whereas a AuGe/Au electrode was evaporated on the InP back surface. In a similar way, we have obtained n-type and p-type MIS-InGaAs structures by using Zn-doped $In_{.53}Ga_{.47}As$ (1.1×10^{16} cm^{-3}) and S-doped $In_{.53}Ga_{.47}As$ (6.6×10^{15} cm^{-3}) substrates. The ratio between silicon and nitrogen in the SiN_x films ranged from $x = 0.97$ to $x = 1.55$. This time only the intermediate composition value ($x = 1.5$) samples underwent RTA treatments.

Room temperature 1 MHz Capacitance–voltage curves obtained for all the samples clearly exhibit hysteresis phenomena, thus indicating that interface states distribution follows the DIGS model [7–9]. Emission and capture of free electrons by states located far from the interface can occur by means of tunnelling mechanisms. As emission and capture kinetics are slow and not symmetrical, the capacitance value depends both on the direction and on the speed of the voltage variation.

DLTS between 78 and 300 K was carried out, in order to determine the energy distribution of interface states, D_{it}. A comparison of these profiles provides us information about the dielectric composition and RTA temperature influence on the interface quality, both for InP and $In_{.53}Ga_{.47}As$ substrates. By applying the adequate quiescent and pulsed bias values, DLTS is also useful to determine the presence of deep levels in the semiconductor bulk.

As DLTS technique does not provide information about the damage spatial distribution, we have measured conductance transients corresponding to several work temperatures and frequency values. The basis of this technique is shown in Fig. 1 [10]. From the experimental conductance transients, $G(t)$, we can obtain the DIGS state density (N_{DIGS}) as a function of the spatial distance to the interface (x_c) and of the energy position, as follows:

$$N_{DIGS} = \frac{\Delta G/\omega}{0.4qA}, \tag{1}$$

$$x_c(t) = x_{on} \ln(\sigma_0 v_{th} n_s t), \tag{2}$$

$$E' - E(x_c, t) = H_{eff} + kT \ln\left(\frac{\sigma_0 v_{th} N_c}{\omega/1.98}\right) - \frac{kT}{x_{on}} x_c(t), \tag{3}$$

where $x_{on} = \hbar/2\sqrt{2m_{eff}H_{eff}}$ is the tunnelling decay length, σ_0 is the carrier capture cross-section value for $x = 0$, v_{th} is the carrier thermal velocity in the semiconductor, and n_s is the free carrier density at the interface. Finally, H_{eff} is the insulator–semiconductor energy barrier for minority carriers and E' means the carrier energy band edge at the insulator (E'_c for electrons and E'_v for holes).

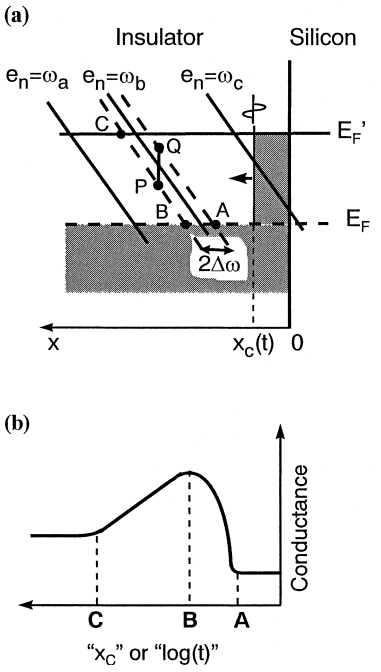

Fig. 1. (a) Schematic band diagram of an insulator semiconductor interface illustrating the capture of electrons by DIGS continuum states during a conductance transient. (b) General shape of the conductance transient.

3. Results and discussion

Fig. 2(a) shows interface state DLTS results corresponding to $Al/SiN_{0.97}$:H/InP structures. Similar curves have been obtained for the $Al/SiN_{1.43}$:H/InP samples. We can see that RTA treatments between 400°C and 700°C seem to make worse the insulator–semiconductor interface. In our previous works [4–6], we reported an interface state density decrease for RTA temperatures lower than 600°C, because nitrogen atoms filled some phosphorous vacancies. In that study, the dielectric nitrogen content values were higher than in the present case, so we can conclude that a value of x lower than 1.55 is not enough to anneal the interface. Moreover, this time, we dispose of transient conductance measurements, which provide us complementary information. As we can see in Fig. 2(b), the height of conductance transient diminishes when annealing temperature increases. Since damage density is proportional to transient height, we can conclude that RTA treatments take out the insulator damage to the interface. Fig. 2(c) shows DIGS damage density as a function of the distance from the interface and of the energy position measured from the insulator conduction band edge, as obtained following the procedure indicated in paragraph 2. In contrast, in Fig. 3(a), we can see that RTA temperatures between 500 and 600°C provide a decrease

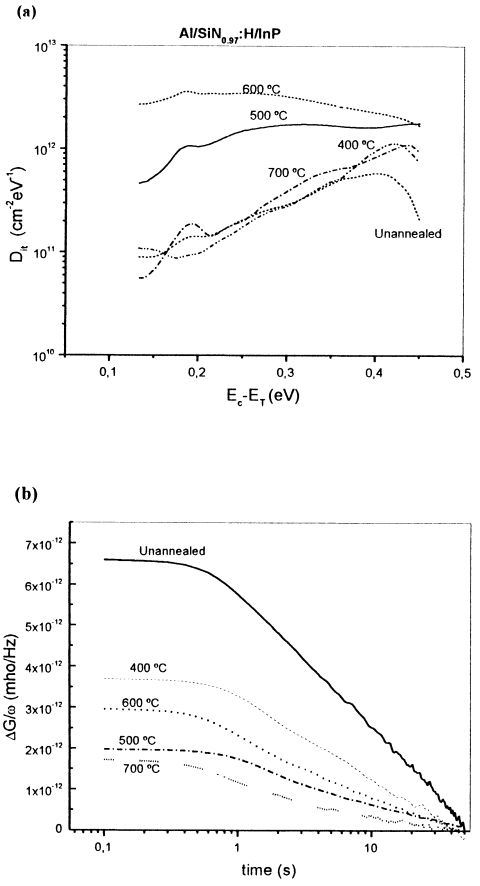

Fig. 2. Results obtained for $Al/SiN_{0.97}$:H/InP structures: (a) interfacial state density measured by DLTS technique; (b) room-temperature-200 KHz-conductance transients; (c) DIGS damage density.

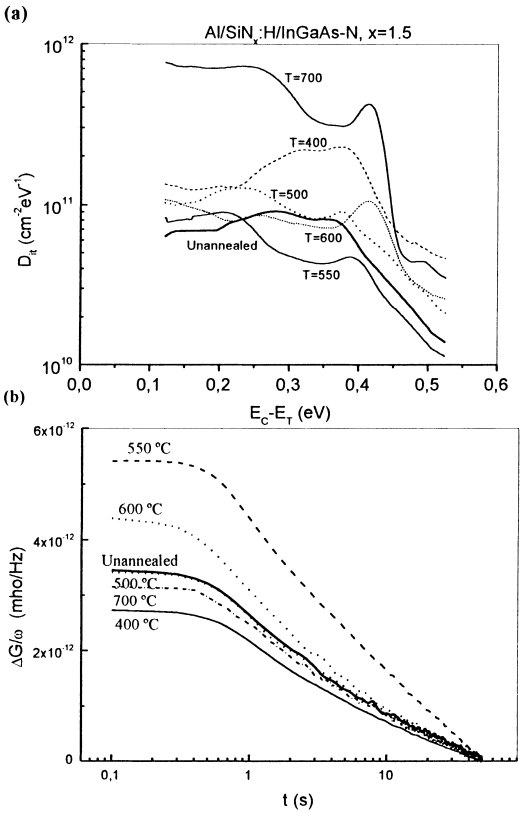

Fig. 3. Results obtained for $Al/SiN_{1.5}$:H/InGaAs-n structures: (a) interfacial state density measured by DLTS technique; (b) room-temperature-200 KHz-conductance transients.

of interfacial state density in the $Al/SiN_{1.5}$:H/$In_{.53}Ga_{.47}As$-n samples, whereas annealing temperatures of 400 and 700°C do increase it. Conductance transients' inspection (Fig. 3(b)) reveals that insulator damage evolution with RTA temperature is opposite to interfacial state density, i.e. extreme temperature values diminish insulator damage, whereas intermediate temperature values increase it. This behaviour seems to suggest some temperature activated defect exchange between the insulator and the interface.

As for the insulator composition influence on the interface quality, Fig. 4 shows DLTS spectra (a) and conductance transients (b) corresponding to unannealed Al/SiN_x:H/$In_{.53}Ga_{.47}As$-n structures, x varying between 0.97 and 1.55. DLTS results suggest that intermediate x values (1.43 and 1.50) provide better interfaces than extreme x values. Conductance transient measurements add complementary information: insulator damage increases when x increases. Hence, $x = 1.43$ seems to be the best choice to improve the overall interface quality.

Finally, from our DLTS measurements, we have found that ECR processes produce a deep level located at about 0.19 eV below the InP conduction band edge.

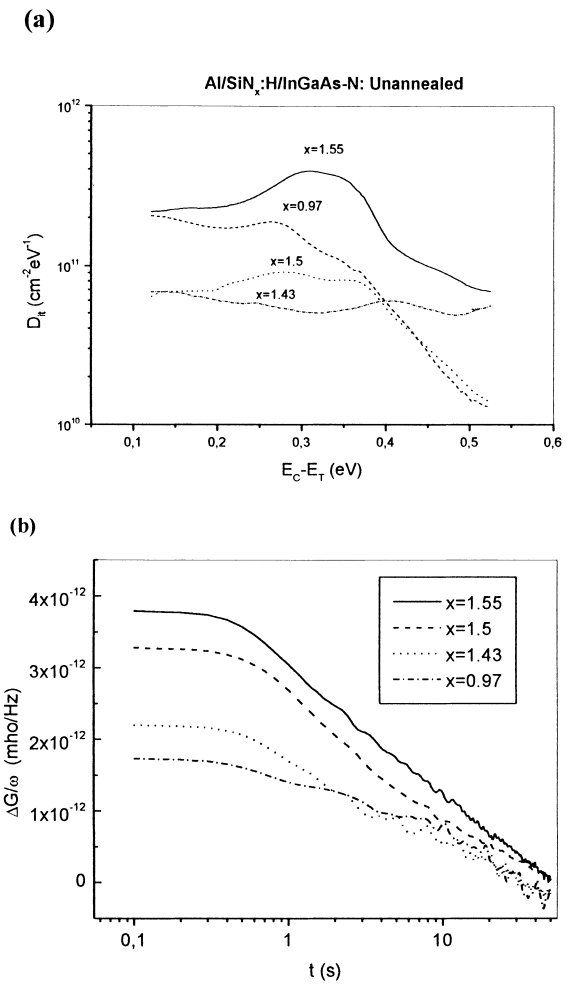

Fig. 4. Results obtained for unannealed Al/SiN$_x$:H/InGaAs-n structures: (a) interfacial state density measured by DLTS technique; (b) room-temperature-200 KHz-conductance transients.

This deep level is present in all the samples except in those that underwent 700°C RTA, which exhibited a deeper deep level (E_C-0.24 eV). We have already reported identical results corresponding to silicon nitride dual layer Al/SiN$_x$:H/InP structures [6], and a tentative explanation of the physical nature of the detected deep levels was proposed elsewhere. As for unannealed and RTA annealed n-type In$_{.53}$Ga$_{.47}$As samples, we have detected a deep level located at about 0.42 eV below the conduction band edge. On the other hand, both unannealed and RTA annealed p-type In$_{.53}$Ga$_{.47}$As samples exhibit a deep level located at about 0.32 meV above the valence band edge.

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