

High-k gate stacks on low bandgap tensile strained Ge and GeSn alloys for Field Effect Transistors

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Abstract:

We present the epitaxial growth of Ge and $\text{Ge}_{0.94}\text{Sn}_{0.06}$ layers with 1.4% and 0.4% tensile strain, respectively, by reduced pressure chemical vapor deposition on relaxed GeSn buffers and the formation of high-k/metal gate stacks thereon. Annealing experiments reveal that process temperatures are limited to 350°C to avoid Sn diffusion. Particular emphasis is placed on the electrical characterization of various high-k dielectrics, as 5nm Al_2O_3 , 5nm HfO_2 or 1nm Al_2O_3 /4nm HfO_2 , on strained Ge and strained $\text{Ge}_{0.94}\text{Sn}_{0.06}$. Experimental capacitance-voltage characteristics are presented and the effect of the small bandgap, like strong response of minority carriers at applied field, are discussed via simulations.

KEYWORDS: strained Ge, GeSn, high-k dielectrics, low bandgap alloys

Recently, Germanium and Germanium-Tin (GeSn) have attracted great interest to integrate nanoelectronics and photonics to realize more energy efficient circuits. Ge offers the highest bulk hole mobility amongst all semiconductors^{1,2}. Its integration into microelectronics was hindered mainly because of the poor structural and electrical properties of the high-k/Ge interface. Recent work on surface passivation of bulk Ge crystals^{3,4} and gate dielectric deposition on those surfaces^{5,6} has paved the way towards the integration of Ge into high performance metal oxide semiconductor field effect transistors (MOSFETs). Low bandgap semiconductors with a direct gap are particularly desired for novel low power devices such as tunnel-field effect transistors (Tunnel-FET).^{7,8} In this context, the electronic band structure of Ge can be tuned by applying biaxial tensile strain⁹ or by Sn alloying¹⁰ towards a fundamental direct bandgap which enhances the tunneling probability and thus the ON-current of Tunnel-FETs^{8,11,12}. Vertical Tunnel-FET structures using strained Ge channels were recently proposed based on InGaAs¹³ and GeSn¹¹ buffer substrates. Under biaxial strain both the indirect (L-valley) as well as the direct (Γ -valley) bandgap shrink significantly with strain and Ge becomes direct at a strain level of about 1.5%. The alloying with Sn shifts the direct transition to lower tensile strains. In addition to a direct bandgap, strained GeSn layers offer smaller effective masses for both, holes and electrons¹⁴, making their use advantageous for drift based devices as MOSFETs. Tensile biaxial strain in Ge and GeSn alloys is very promising, however, its experimental implementation using a simple and Si-based compatible process is challenging. The breakthrough in the growth of high quality

epitaxial GeSn^{15,16} and SiGeSn^{17,18} alloys enables a new degree of freedom in group IV strain engineering.

Based on these achievements a study of high-k/metal gate stacks on tensile strained Ge and GeSn alloys on appropriate buffers and their epitaxial growth is presented. Furthermore, the thermal stability of these novel materials is reported as this is most relevant for future device developments. Different high-k dielectrics have been deposited in order to study the interface passivation via electrical measurements at temperatures ranging from 80 K to 300 K.

Ge/GeSn heterostructures were grown in an industry compatible AIXTRON TRICENT® reduced-pressure chemical vapor deposition reactor on 2.5 μm thick Ge virtual substrates (VS) on 200 mm Si(100) wafers. The Ge-VS exhibits a weak tensile strain of about 0.16% and a threading dislocation density close to $1 \times 10^7 \text{ cm}^{-2}$. Partially relaxed GeSn layers with thicknesses between 200 and 300 nm were grown on top of these Ge-VS and capped with 50 to 70 nm thick Ge layers. A schematic of a MOSFET with a tensile strained Ge channel and source/drain NiGe(Sn) stressors as well as a possible layer structure of p-i-n Tunnel-FET with strained Ge and GeSn alloys are shown in Fig 1a,b.

The biaxial tensile strain in the Ge epilayer increases with the Sn concentration and the degree of strain relaxation of the GeSn buffer. Different Ge strains, namely 0.7%, 1.1% and 1.4%, were achieved by modifying the Sn content in the buffer (details in S.I.). The X-ray diffraction (XRD) reciprocal space map (RSM) of 70 nm thick 1.4% strained Ge on 300 nm Ge_{0.89}Sn_{0.11}/ Ge-VS heterostructure is shown in Fig. 1c. It is obvious that this GeSn buffer technology facilitates complex strained heterostructures adaptable for specific devices designs. A Transmission Electron Microscope (TEM) image of such a heterostructure consisting of 30 nm tensile strained Ge_{0.94}Sn_{0.06} layer with a 10 nm strained Ge layer to separate the top tensile Ge_{0.94}Sn_{0.06}

from the compressive $\text{Ge}_{0.09}\text{Sn}_{0.11}$ buffer is presented. The TEM images prove the high quality of the 0.4% tensile strained $\text{Ge}_{0.94}\text{Sn}_{0.06}$ / $\text{Ge}/\text{Ge}_{0.89}\text{Sn}_{0.11}$ buffer/Ge-VS structure with no indication of defects, such as threading dislocations, related to strain relaxation of the strained top.

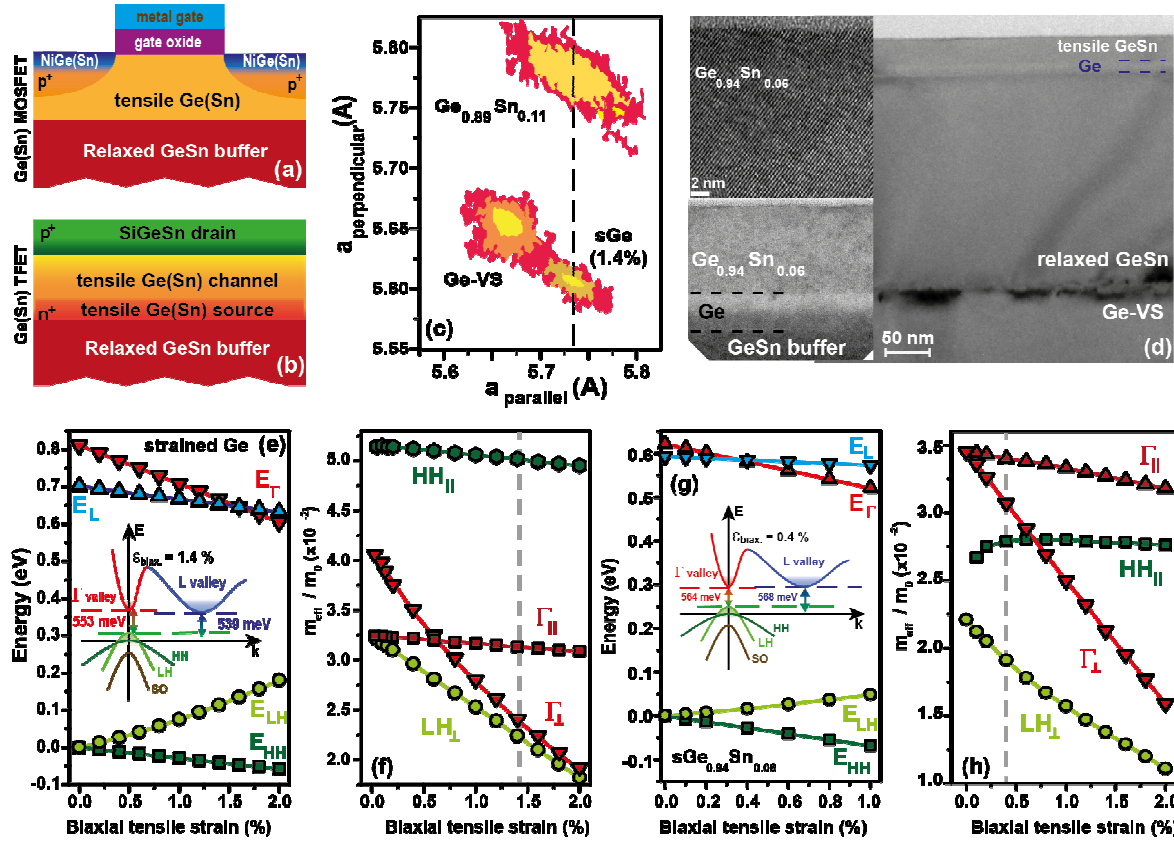


Figure 1: Schematics of possible (a) MOSFET and (b) TFET devices based on tensile strained Ge(Sn) layers. (c) XRD RSM of strained Ge/GeSn/Ge-VS heterostructures indicating 1.4% biaxial tensile strain in the top Ge layers. (d) TEM micrographs of the strained $\text{Ge}_{0.94}\text{Sn}_{0.06}/\text{Ge}/\text{Ge}_{0.89}\text{Sn}_{0.11}/\text{Ge-VS}$ structure. The inset shows the high crystallinity of the top GeSn layer. (e-h) Effect of biaxial strain on the (e,g) electronic band structure and (f,h) electron and hole effective masses at 300 K. The schematic band structure of Ge and GeSn under tensile strain of 1.4% and 0.4%, respectively are shown as inset.

Figure 1e-h show the Ge and $\text{Ge}_{0.94}\text{Sn}_{0.06}$ bandgaps and the electron and hole effective masses at 300 K as a function of strain, as calculated with the 8x8 **k.p** method including strain¹⁹. The biaxial strain lifts the degeneracy of heavy-hole (HH) and light-hole (LH) valence bands, hence the LH band population increases. The Γ -valley electron and the LH band effective masses decrease with increasing tensile strain.

In the following we present the formation of high-k dielectric stacks on strained Ge(Sn) /GeSn heterostructures and corresponding metal oxide semiconductor (MOS) capacitors, an essential ingredient of MOSFETs. After diluted “HF:HCl-last” wet cleaning step the strained Ge(Sn) samples were loaded into an atomic layer deposition reactor where three different high-k dielectric stacks were deposited: 5 nm Al_2O_3 , 1 nm Al_2O_3 /4 nm HfO_2 or 5 nm HfO_2 (details in SI) In addition, a 5 min *in-situ* O_3 dry oxidation step was performed before or after the deposition of the first 1 nm Al_2O_3 . The O_3 dry oxidation produces a controlled interfacial GeO_x growth which improves the Ge surface passivation.²⁰ The MOS capacitor formation is completed by the deposition of Pt as metal contact and Forming Gas Annealing (FGA) at different temperatures (300°C - 400°C) for 10 min in H_2 (4 %)/ N_2 (96 %) ambient.

The thermal stability of the strained heterostructures was investigated prior to electrical characterization. Due to the low solid solubility of Sn in Ge, Sn tends to segregate towards the surface in metastable GeSn layers²¹. Hence, we investigated MOS structures at different FGA temperatures. Figure 2b,d shows elemental Time-of-Flight Secondary Ion Mass Spectroscopy (ToF SIMS) depth profiles for Al_2O_3 capped strained Ge and strained GeSn heterostructures annealed at 300°C (broken lines) and 350°C (solid lines). For the FGA at 300°C the Sn signals (green dashed line) indicate homogeneous Sn distribution within the GeSn layers, with sharp

Ge/GeSn interfaces for the 300°C FGA. Only moderate Ge diffusion (blue dashed line) into Al_2O_3 layers is observed. XRD-RSM measurements confirmed that the lattice constant remained unchanged during this FGA; *i.e.* full elastic strain is conserved. Increasing the FGA temperature to 350°C induces strong diffusion of Sn from the GeSn layers into the strained Ge layer reaching the Al_2O_3 (see also S.I.). Detailed analyses of all Ge and Sn isotopes proved that Ge reaches even the high-k surface, while Sn stops within the dielectric layer. In conclusion, at 300°C Sn diffusion is sufficiently slow to preserve the chemical purity of the Ge layer and the initial strain. Therefore, for all MOS capacitors the deposition of both, Al_2O_3 and HfO_2 dielectrics, the O_3 oxidation and the FGA were performed at 300°C. The TEM images in Fig. 2a,c show both, the strained Ge and GeSn MOS capacitors formed with 5 nm HfO_2 dielectric after FGA annealing at 300°C. The crystalline quality of the layer is conserved and a smooth interface strained Ge(Sn)/ HfO_2 observed. High resolution TEM images allow the estimation of an interface layer of about 0.8 nm.

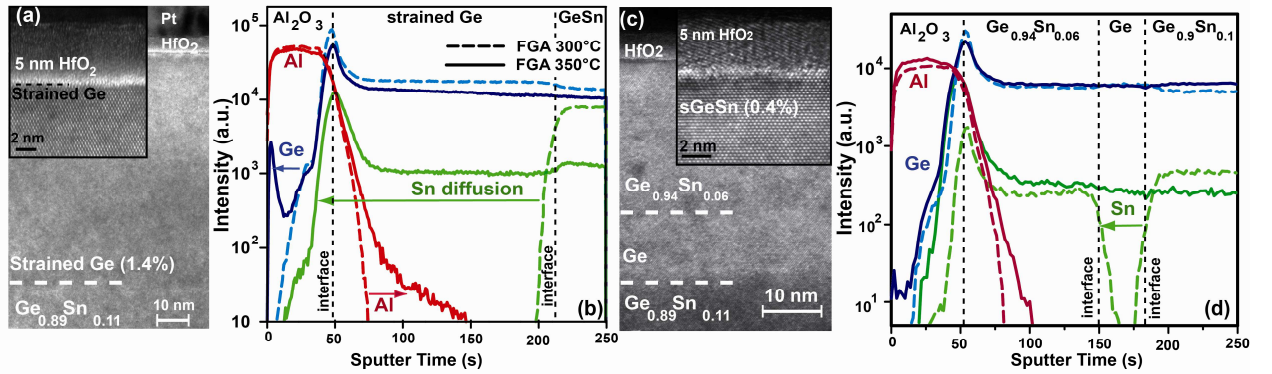


Figure 2 (a,c) TEM micrographs of the 5 nm HfO_2 /strained Ge(Sn)/Ge_{0.89}Sn_{0.11}/Ge-VS structures. The insets in shows the interface HfO_2 /strained Ge(Sn) with the thin interface layer (~ 0.8 nm) formed during the O_3 oxidation. (b,d) ToF-SIMS spectra of Al_2O_3 /strained Ge/

Ge_{0.905}Sn_{0.095} after FGA at 300°C (dashed lines) and 350°C (solid line). At 350°C Ge diffuses to the surface while Sn diffusion stops within the dielectric layer.

In the following we address the challenges due to the very low bandgap in respect of correct electrical characterization of the tensile Ge(Sn)/high-k MOS capacitors. Calculation of the ideal C-V characteristics with a custom-made numerical tool²² allows assessing the effect of the bandgap energy on the inversion response. Figure 3a shows that inversion response occurs at smaller applied bias and strongly increases with the decrease of the bandgap. Moreover, for smaller bandgaps, *e.g.* ~ 0.54 eV, as for 1.4% tensile strained Ge, the inversion response is very strong even at high frequency (1 MHz). The minority carrier response causes severe imprecisions of the conductance methods for the determination of the density of interface traps (D_{it})²³. The effect of thermal carrier generation can be suppressed at low temperatures. The resonance frequency of a trap level, given by Fermi-Dirac statistics, depends mostly on the energy difference with the band edges and on temperature²⁴. Figure 3b shows the resonance frequencies of trap levels in Ge calculated by taking into account the temperature dependence of the effective density of states of the conduction and the valence bands, the variation of the Ge bandgap and of the electron thermal velocity. The dashed lines represent the estimated characteristic trap frequency for 1.1% strained Ge using bulk Ge parameters²⁵. The trap energy regions within the bandgap which can be scanned using the standard 1 kHz – 1 MHz instrumental frequency range, becomes narrow and shift towards the band edge energy when the measurement temperature is decreased. The above discussion states that for strained Ge and GeSn semiconductors the extraction of D_{it} is not straightforward as for the case of Si or SiGe alloys.

For each strained Ge(Sn)/high-k combination, a comparison was made with reference MOS structures on Ge-VS using identical conditions. The intrinsic carrier concentration in GeSn

buffers estimated via electrochemical capacitance voltage measurements is at $1 \times 10^{17} \text{ cm}^{-3}$. In Fig. 4a the room temperature capacitance-voltage (C-V) measurements at modulation frequency of 1 MHz are displayed for three differently processed Ge based MOS structures.

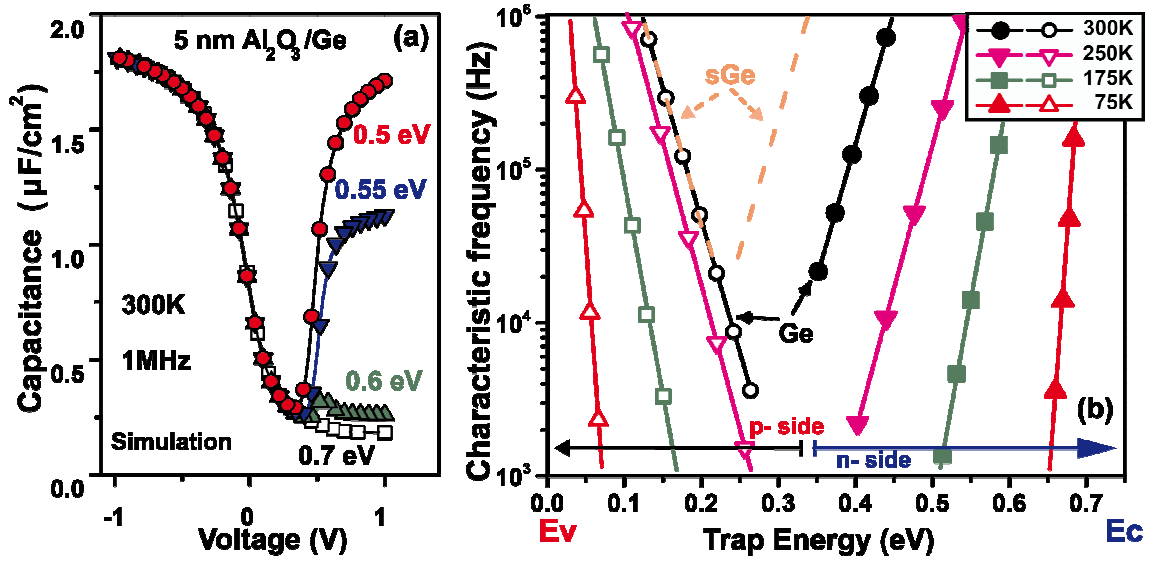


Figure 3: (a) C-V simulations for $\text{Al}_2\text{O}_3/\text{Ge}$ using Ge bandgap as parameter (b) Calculated resonance frequency of trap levels in Ge for different temperatures and for Ge with strain level of 1.1%. The temperature dependence of the effective density of states, bandgap and electron thermal velocities are calculated using data from Ref.²⁵. The data for strained Ge (thick dashed lines) refer only to 300 K. Ge bulk parameters are used.

As expected, the highest capacitance in accumulation, at the same oxide thickness of 5 nm, is obtained for HfO_2 due to a higher effective dielectric constant compared to the Al_2O_3 and $\text{Al}_2\text{O}_3/\text{HfO}_2$ stacks. For the investigated gate stacks neither humps, due to interface traps, nor frequency-dependent flatband voltage (V_{FB}) shifts, stemming from a high D_{it} , were observed. While the conductance method is well suited to quantify the D_{it} at the high-k/semiconductor

interfaces when the admittance is governed by the majority carrier response^{26,27}, attention has to be paid to the large minority carrier density in Ge²⁸, as discussed above. Thus, our extracted D_{it} levels at room temperature of about $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for 5 nm Al_2O_3 and $5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for 5 nm HfO_2 on Ge, should be considered as upper limits due to the interaction of interface traps with majority as well as minority carriers³⁵.

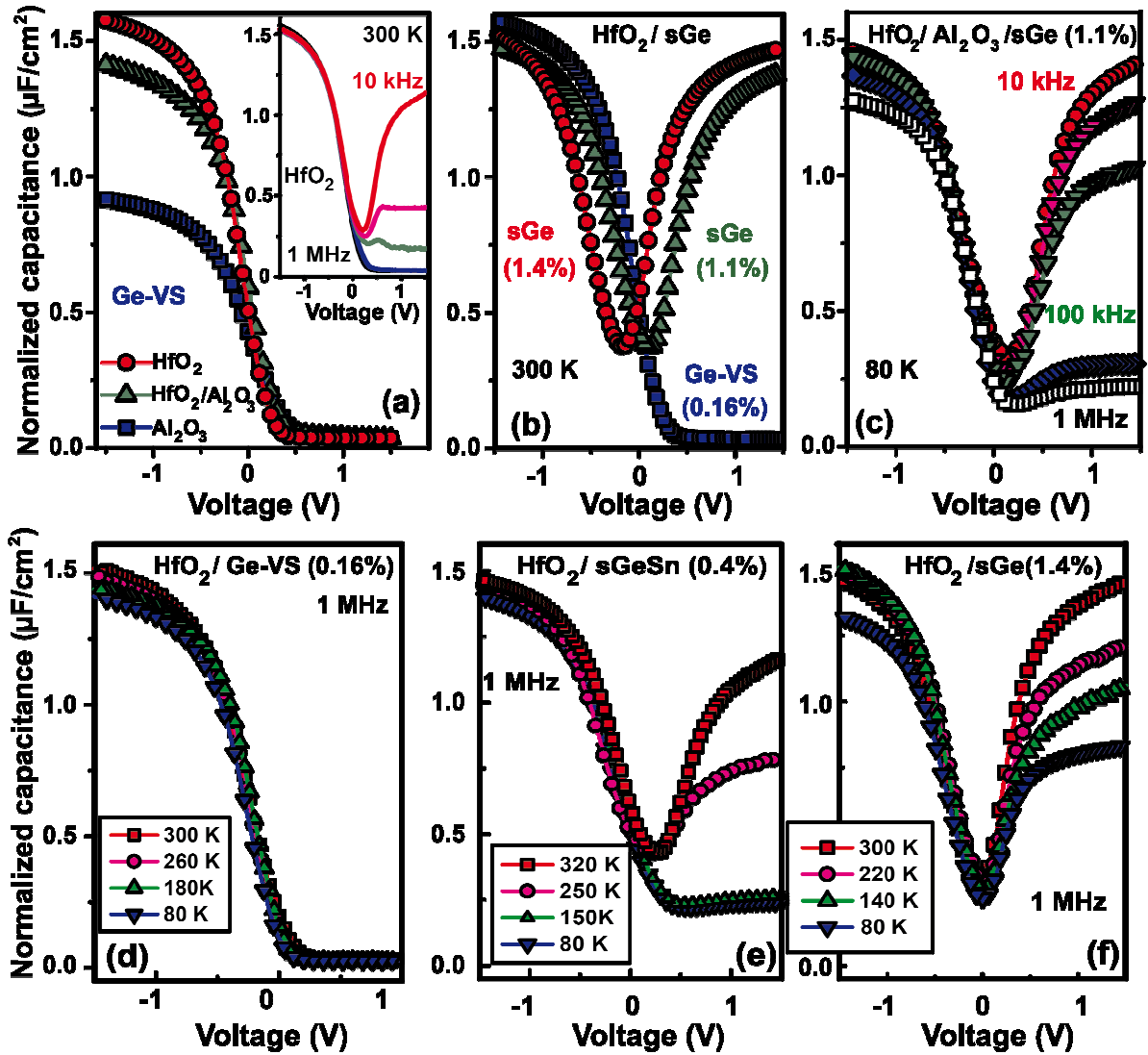


Figure 4: (a) C - V curves of different high- k stacks on Ge-VS measured with 1 MHz at 300 K. The frequency dispersion for $\text{HfO}_2/\text{Ge-VS}$ is shown as inset; (b) comparison of C - V at 1 MHz for

5 nm HfO₂ on Ge-VS and on 1.1% and 1.4% strained Ge, respectively. (c) Effect of frequency on the C-V response for 1 nm Al₂O₃/4 nm HfO₂/ Ge (1.1% strain) structure at 80 K. (d-f) Temperature dependence of 1 MHz C-V characteristics for 5 nm HfO₂ on (d) Ge-Vs, (e) strained GeSn (0.4%) and (f) strained Ge (1.4%).

Figure 4b shows that for 1.4% strained Ge MOS capacitors an inversion capacitance close to the accumulation capacitance is obtained at 300 K at high frequency of 1 MHz. With increasing strain in Ge the weak inversion (minority carriers) appears before the depletion (majority carriers). This effect has been already reported in literature for cubic Ge²⁸. Inversion emerges at smaller applied bias and becomes stronger with the decrease of bandgap, e.g. with increase of strain in the Ge layer. Moreover, the carriers are able to follow the external applied field over the complete frequency range typically used in CMOS characterization. This is a characteristic of low bandgap materials, as strained Ge(Sn) and represents one of the findings of our investigations. In applications, low gate voltages allow reduced losses in electronic circuits since less energy is required to switch the MOSFET devices.

The temperature dependence of the C-V characteristics for HfO₂ based gate stacks is shown in Fig 4c-f. At lower temperatures the reduced inversion response qualitatively translates into a steeper depletion slope. As explained above Dit data extraction is restricted to a range of energies shifted close to the band edge over which conductance data can be obtained. At 80K the conductance methods provides minimum values for Dit of $4.1\text{-}6 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$ for HfO₂ on strained Ge under 1.1% strain as well as a very low Dit of $2.9\text{-}4 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$ for strained GeSn MOS capacitors. For the determination of Dit the capture cross sections and thermal velocities of unstrained Ge were used. In order to estimate Dit at 300K the low frequency method²⁹ was

applied. A minimum D_{it} of $2 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ for Ge and \sim of $5 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ for strained Ge under 1.1% and 1.4% was found. The semiconductor bandgap increases with decreasing temperature. The direct bandgap energy of Ge is about 0.8 eV. When the temperature drops from 300 to 80 K, the bandgap energy of bulk Ge increases by about 0.07 eV. Applying the Ge temperature dependence of the bandgap to strained Ge, we obtain the same C-V characteristics for the 1.1% strained Ge (Fig. 4c) and strained GeSn (Fig. 4e) at 80 K close to the Ge at RT. Correspondingly, for 1.4% biaxial tensile strained Ge the bandgap energy increases from 0.54 eV to 0.63 eV from 300 to 80 K. As a consequence, the inversion response should be less pronounced than the one shown in Fig. 4f. In order to gain understanding of the inversion response we have performed numerical C-V simulations including a diffusion model^{22,30} of the MOS structures (details in SI). The modeling indicates that at constant bandgap but different carrier mobilities the inversion response increases with higher electron (minority carriers) mobility, while the hole (majority carriers) mobility has no effect. Consequently, the differences in the inversion response are an indication of enhanced electron mobility under tensile strain, in addition to the bandgap narrowing effect. This is also supported by the effective mass calculation presented in Fig. 1f,h, indicating a lower electron effective mass (here minority carriers) in strained Ge as compared with the strained GeSn, for the strain values discussed here. The lowest electron effective mass is calculated for 1.4% strained Ge which shows also experimentally the highest inversion response (see also Table S2 from SI.). Strained GeSn with very low hole effective masses may be exploited in p-type GeSn channel MOSFETs or Tunnel-FETs by forming a strained Ge/strained GeSn source-channel tunneling junction as suggested in Fig. 1a.

In summary, epitaxial growth of device-grade Ge and GeSn layers with high tensile biaxial strain up to 1.4% have been achieved by employing high Sn content GeSn buffer layers. Smooth and steep MOS C-V characteristics for Al₂O₃/HfO₂ high-k gate stacks have been demonstrated for the temperature range of 80 K to 300 K. Strain induced bandgap narrowing in these low band gap materials results in a strong inversion response of the minority carrier as further substantiated by simulation. Further investigations are needed to elucidate experimentally the carrier transport in these novel materials. The dielectric/ strained Ge(Sn) characterization presented here represents an essential step towards realization of Ge(Sn)-MOSFETs. In addition, these new semiconductors will inspire novel developments, such as strained Ge(Sn) Tunnel-FETs⁸ and optoelectronic applications.

ASSOCIATED CONTENT

Supporting Information. Details about the characterization of strained Ge(Sn)/GeSn are given, including RSM images and SIMS profiles. The methods used for band structure calculations and simulation of the CV characteristics are also included. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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REFERENCES

- (1) Pillarisetty, R. Academic and Industry Research Progress in Germanium Nanodevices. *Nature* **2011**, *479*, 324–328.
- (2) Dobbie, A.; Myronov, M.; Morris, R. J. H.; Hassan, A. H. A.; Prest, M. J.; Shah, V. a.; Parker, E. H. C.; Whall, T. E.; Leadley, D. R. Ultra-High Hole Mobility Exceeding One Million in a Strained Germanium Quantum Well. *Appl. Phys. Lett.* **2012**, *101*, 172108.
- (3) Zhao, M.; Liang, R.; Wang, J.; Xu, J. Improved Electrical Properties of Ge Metal-Oxide-Semiconductor Devices with HfO₂ Gate Dielectrics Using an Ultrathin GeSnO_x Film as the Surface Passivation Layer. *Appl. Phys. Lett.* **2013**, *102*, 142906.
- (4) Gupta, S.; Chen, R.; Harris, J. S.; Saraswat, K. C. Atomic Layer Deposition of Al₂O₃ on Germanium-Tin (GeSn) and Impact of Wet Chemical Surface Pre-Treatment. *Appl. Phys. Lett.* **2013**, *103*, 241601.
- (5) Hudait, M. K.; Zhu, Y. Energy Band Alignment of Atomic Layer Deposited HfO₂ Oxide Film on Epitaxial (100)Ge, (110)Ge, and (111)Ge Layers. *J. Appl. Phys.* **2013**, *113*, 114303.
- (6) Gusev, E. P.; Shang, H.; Copel, M.; Gribelyuk, M.; D’Emic, C.; Kozlowski, P.; Zabel, T. Microstructure and Thermal Stability of HfO₂ Gate Dielectric Deposited on Ge(100). *Appl. Phys. Lett.* **2004**, *85*, 2334.
- (7) Yang, Y.; Guo, P.; Han, G.; Lu Low, K.; Zhan, C.; Yeo, Y.-C. Simulation of Tunneling Field-Effect Transistors with Extended Source Structures. *J. Appl. Phys.* **2012**, *111*, 114514.
- (8) Kao, K.-H.; Verhulst, A. S.; Van de Put, M.; Vandenberghe, W. G.; Soree, B.; Magnus, W.; De Meyer, K. Tensile Strained Ge Tunnel Field-Effect Transistors: K · P Material Modeling and Numerical Device Simulation. *J. Appl. Phys.* **2014**, *115*, 044505.
- (9) Sánchez-Pérez, J. R.; Boztug, C.; Chen, F.; Sudradjat, F. F.; Paskiewicz, D. M.; Jacobson, R. B.; Lagally, M. G.; Paiella, R. Direct-Bandgap Light-Emitting Germanium in Tensilely Strained Nanomembranes. *Proc. Natl. Acad. Sci. U. S. A.* **2011**, *108*, 18893–18898.

- (10) Gupta, S.; Chen, R.; Huang, Y.; Kim, Y.; Sanchez, E.; Harris, J. S.; Saraswat, K. C. Highly Selective Dry Etching of Germanium over Germanium-Tin (Ge_{1-x}Sn_x): A Novel Route for Ge_{1-x}Sn_x Nanostructure Fabrication. *Nano Lett.* **2013**, *13*, 3783–3790.
- (11) Wirths, S.; Tiedemann, A. T.; Ikonc, Z.; Harrison, P.; Holländer, B.; Stoica, T.; Mussler, G.; Myronov, M.; Hartmann, J. M.; Grützmacher, D.; Buca, D.; Mantl, S. Band Engineering and Growth of Tensile Strained Ge/(Si)GeSn Heterostructures for Tunnel Field Effect Transistors. *Appl. Phys. Lett.* **2013**, *102*, 192103.
- (12) Kotlyar, R.; Avci, U. E.; Cea, S.; Rios, R.; Linton, T. D.; Kuhn, K. J.; Young, I. A. Bandgap Engineering of Group IV Materials for Complementary N and P Tunneling Field Effect Transistors. *Appl. Phys. Lett.* **2013**, *102*, 113106.
- (13) Zhu, Y.; Maurya, D.; Priya, S.; Hudait, M. K. Tensile-Strained Nanoscale Ge/In 0.16 Ga 0.84 As Heterostructure for Tunnel Field-E Ff Ect Transistor. *ACS Appl. Mater. Interfaces* **2014**, *6*, 4947–4953.
- (14) Lu Low, K.; Yang, Y.; Han, G.; Fan, W.; Yeo, Y. Electronic Band Structure and Effective Mass Parameters of Ge_{1-x}Sn_x Alloys. *J. Appl. Phys.* **2012**, *112*, 103715.
- (15) Wirths, S.; Ikonc, Z.; Tiedemann, A. T.; Holla□nder, B.; Stoica, T.; Mussler, G.; Breuer, U.; Hartmann, J. M.; Benedetti, A.; Chiussi, S.; Gru□tzmacher, D.; Mantl, S.; Buca, D. Tensely Strained GeSn Alloys as Optical Gain Media. *Appl. Phys. Lett.* **2013**, *103*, 192110.
- (16) Vincent, B.; Gencarelli, F.; Bender, H.; Merckling, C.; Douhard, B.; Petersen, D. H.; Hansen, O.; Henrichsen, H. H.; Meersschaut, J.; Vandervorst, W.; Heyns, M.; Loo, R.; Caymax, M. Undoped and in-Situ B Doped GeSn Epitaxial Growth on Ge by Atmospheric Pressure-Chemical Vapor Deposition. *Appl. Phys. Lett.* **2011**, *99*, 152103.
- (17) D’Costa, V. R.; Fang, Y. Y.; Tolle, J.; Kouvetakis, J.; Menéndez, J. Ternary GeSiSn Alloys: New Opportunities for Strain and Band Gap Engineering Using Group-IV Semiconductors. *Thin Solid Films* **2010**, *518*, 2531–2537.
- (18) Wirths, S.; Buca, D.; Ikonc, Z.; Harrison, P.; Tiedemann, A. T.; Holländer, B.; Stoica, T.; Mussler, G.; Breuer, U.; Hartmann, J. M.; Grützmacher, D.; Mantl, S. SiGeSn Growth Studies Using Reduced Pressure Chemical Vapor Deposition towards Optoelectronic Applications. *Thin Solid Films* **2013**, *557*, 183–187.
- (19) Bahder, T. Eight-Band K□p Model of Strained Zinc-Blende Crystals. *Phys. Rev. B* **1990**, *41*, 11992–12001.
- (20) Gupta, S.; Vincent, B.; Yang, B.; Lin, D.; Gencarelli, F.; Lin, J.-Y. J.; Chen, R.; Richard, O.; Bender, H.; Magyari-Kope, B.; Caymax, M.; Dekoster, J.; Nishi, Y.; Saraswat, K. C. Towards High Mobility GeSn Channel nMOSFETs: Improved Surface Passivation Using

- Novel Ozone Oxidation Method. In *2012 International Electron Devices Meeting*; IEEE, 2012; pp. 16.2.1–16.2.4.
- (21) Wirths, S.; Buca, D.; Mussler, G.; Tiedemann, A. T.; Hollander, B.; Bernardy, P.; Stoica, T.; Grutmacher, D.; Mantl, S. Reduced Pressure CVD Growth of Ge and Ge_{1-x}Sn_x Alloys. *ECS J. Solid State Sci. Technol.* **2013**, 2, N99–N102.
 - (22) Baert, B.; Schmeits, M.; Nguyen, N. D. Study of the Energy Distribution of the Interface Trap Density in a GeSn MOS Structure by Numerical Simulation of the Electrical Characteristics. *Appl. Surf. Sci.* **2014**, 291, 25–30.
 - (23) Engel-Herbert, R.; Hwang, Y.; Stemmer, S. Comparison of Methods to Quantify Interface Trap Densities at dielectric/III-V Semiconductor Interfaces. *J. Appl. Phys.* **2010**, 108, 124101.
 - (24) Brammertz, G.; Martens, K.; Sioncke, S.; Delabie, A.; Caymax, M.; Meuris, M.; Heyns, M. Characteristic Trapping Lifetime and Capacitance-Voltage Measurements of GaAs Metal-Oxide-Semiconductor Structures. *Appl. Phys. Lett.* **2007**, 91, 133510.
 - (25) Electronic archive- New Semiconductor Materials. Characteristics and Properties <http://www.ioffe.ru/SVA/NSM/Semicond/Ge/index.html>.
 - (26) Nicollian, E.; Brews, J. *MOS/metal Oxide Semiconductor/physics and Technology*; Wiley-Interscience: New York, 1982.
 - (27) Deen, D. A.; Champlain, J. G. High Frequency Capacitance-Voltage Technique for the Extraction of Interface Trap Density of the Heterojunction Capacitor: Terman's Method Revised. *Appl. Phys. Lett.* **2011**, 99, 053501.
 - (28) Martens, K.; Chui, C. O.; Brammertz, G.; De Jaeger, B.; Kuzum, D.; Meuris, M.; Heyns, M.; Krishnamohan, T.; Saraswat, K.; Maes, H. E.; Groeseneken, G. On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates. *IEEE Trans. Electron Devices* **2008**, 55, 547–556.
 - (29) Schroder, D. K. *Semiconductor Material and Device Characterization*; Third Edit.; John Wiley & Sons, Inc., Hoboken, New Jersey, 2006.
 - (30) Nguyen, N. D.; Schmeits, M. Numerical Simulation of Impedance and Admittance of OLEDs. *Phys. Status Solidi* **2006**, 203, 1901–1914.

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