Single Event Upsets under 14-MeV Neutrons in a 28-nm SRAM-based FPGA in Static Mode

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Abstract

A sensitivity characterization of a Xilinx Artix-7 FPGA against 14.2 MeV neutrons is presented. The content of the internal SRAMs and flip-flops were downloaded in a PC and compared with a golden version of it. Flipped cells were identified and classified as cells of the configuration RAM, BRAM, or flip-flops. SBUs and MCUs with multiplicities ranging from 2 to 8 were identified using a statistical method. Possible shapes of multiple events are also investigated, showing a trend to follow wordlines. Finally, MUSCA SEP3 was used to make assesment for actual environments and an improvement of SEU injection test is proposed.

Index Terms

FPGA, neutron tests, radiation hardness, reliability, soft error.

I. Introduction

RECONFIGURABLE devices, and in particular Field Programmable Gate Arrays (FPGAs) based on Static Random Access Memory (SRAM-FPGAs) have gained popularity in various fields such as nuclear research, aviation and spatial missions, to mention some. The main reasons are their high density of reconfigurable resources, as well as the ability to change their functionality "on the fly", which is also known as *dynamic reconfiguration*. On the other hand, applications running in aircrafts must deal with hard real-time constraints, whereas outer-space devices usually process enormous amounts of data before sending them to the station placed on Earth due to the reduced bandwidth in the downlink.

However, a major concern existing in these fields, especially in the space sector, is the high amount of radiation to which these devices are exposed. These radiations, naturally present in such hazardous environments, may cause soft errors known as Single Event Upsets (SEUs), which may alter the operation of the microelectronic components embedded in on-board systems. SEUs can be classified in several subtypes. Thus, if only one memory cell is affected by the particle, it is called Single Bit Upset (SBU). If more than one bit is flipped by the same particle, but in different logical address, it is called Multiple Cell Upset (MCU). Multiple Bit Upsets (MBUs) occur if the errors involve bitcells located in the same word. In SRAM-based FPGAs, these errors may affect the configuration memory, therefore changing the functionality of the system. Hence, in order to guarantee the correct operation of an autonomous system under such extreme conditions, tackling this problem becomes of critical importance.

State-of-the-art SRAM-based FPGAs have been tested under radiation multiple times in order to assess their reliability. In this article, a Xilinx Artix-7 FPGA (manufactured with 28-nm bulk CMOS process) has been examined against neutrons. The discussion below summarizes the literature concerning other radiation tests on 28-nm FPGAs.

In [1] results from heavy ions testing for Zynq-7000 are presented, with LETs (Linear Energy Transfers) varying from 2.6 to 17 MeV/mg/cm^2. Cross-section values versus LET for configuration memory are provided, both for Block RAM and for SRAM on-chip memory. In [2] it is presented a study of the influence of the angles of incidence and rotation on events induced by low-LET heavy ions in a Xilinx Artix-7 FPGA. The relevant conclusion is that there are significant differences in the MBU cross section depending on the angles of incidence and rotation of the device. Also in [3] a similar study is presented for Kintex-7 using heavy ions, the conclusion of which is that the number and size of MCUs is higher when ions strike along the columns.

It can be proved that high-energy electrons and the secondary particles created by them are also capable of producing soft errors. In [4] the energy dependence of electron-induced soft errors in a 28-nm bulk CMOS Xilinx Kintex-7 SRAM-based

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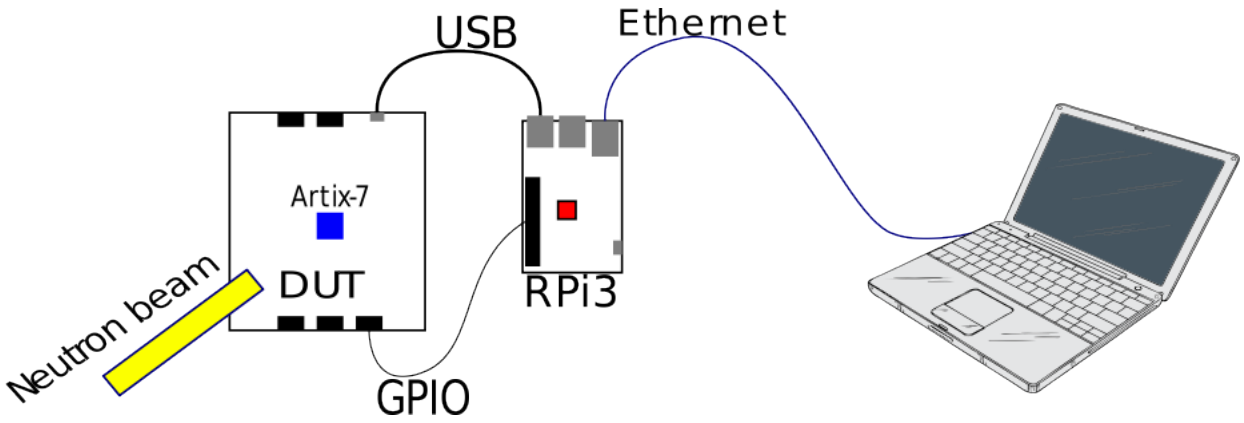


Fig. 1. Device Under Test and control system

FPGA is analyzed. The measured cross section ranges between 10^{-20} and $10^{-17}\mathrm{cm}^2/\mathrm{bit}$ using electrons with energy above 9 MeV. Similar experiments are presented in [5] for an Artix-7 and a Spartan-6.

Regarding neutrons, there are three excellent works presented in [6]–[8]. In [6] a study of power dissipation effects on a 28-nm Xilinx Zynq 7000 FPGA-based System-on-Chip and its neutron sensitivity is presented, demonstrating that the temperature variation caused by a higher operating frequency affects the cross section of the device. In [7] the dynamic SEU sensitivity of designs on Kintex-7 and Stratix V, both of them 28-nm SRAM-based FPGAs, is presented. Also the sensitivities of the design with and without Triple Modular Redundancy (TMR) are compared. Finally, [8] discusses the effects of thermal neutrons and high-energy hadrons issued from tests performed at three facilities: Institute Laue-Langevin (ILL), Laboratory of Subatomic Physics & Cosmology (LPSC), and CERN. MCUs are not studied in these works.

This paper discusses the sensitivity of a 28-nm SRAM-based FPGA under 14.2-MeV neutron radiation and classifies errors in SBUs and MCUs by using a variation of the statistical method presented in [9] and [10]. Issued cross sections are used to make predictions for typical environments and to propose an improvement of fault injection tests. The methodology and the experimental setup are described in Section II. Results are presented and discussed in Sections III and IV. Finally, conclusions and clues of future work are summaryzed in Section V.

II. Test Setup

The experiments were performed with 14-MeV neutrons at the GENEPI2 (GEnérateur à NEutrons Pulsés Intenses) neutron source at the LPSC (CNRS/UGA) [11]. The Device Under Test (DUT) is an Artix-7 FPGA (XC7A100T) embedded into a Nexys-4 DDR board. It has a 25,611,008-bit (N_{CF}) configuration memory, 126,800 (N_{FF}) flip-flops and 4,860 Kb (N_{BR}) of Block RAM, from which 540 Kb are devoted to implement Error Correction Codes (ECC).

During the irradiation, a Raspberry Pi 3 was connected to the board through the Universal Serial Bus (USB) and GPIO (General Purpose Input Output), as depicted in Fig. 1. As it must be close to the DUT to allow efficient communication, it was placed inside the irradiation room and heavily protected to avoid the neutrons affecting its behavior. This device was in charge of controlling the operations performed by the Artix-7. It was running Raspbian as operating system, and a modified version of the OpenOCD software [12], extended to provide the routines needed to issue the correct commands to the Artix-7: GCapture, GRestore, and readback operations. The software can be downloaded from a repository that was put in place by the authors [13]. With the modified code it is possible not only to read back the whole memory, but also frame by frame.

Any word of the configuration memory and BRAM contents could be obtained by reading-back the appropriate frames. However, flip-flop values must be captured by means of GCapture command prior to readback. This command saves the actual content of the flip-flops into specific bits of the configuration memory. Therefore, it was essential to identify the addresses of flip-flops and BRAM cells in the bitstream. In this way, before the tests, all the addresses of both flip-flop and BRAM cells were inferred by using the logic allocation files generated by Xilinx synthesis tools during the "generate bitstream" step. This file is created with extension `.ll`. By using this information it is easy to distinguish among errors occurred in flip-flops, BRAM or configuration memory.

The GPIO of the Nexys4 board was used to provide the clock signal and I/O data to the FPGA. The USB was used to drive the JTAG chain, so the bitstream could be loaded. It is also used to issue GCapture commands and to read-back the configuration memory.

For each experiment, the following steps were made. First, the target design (a simple counter using 80,000 flip-flops and BRAM cells in the FPGA) was loaded into the configuration memory. Every byte of the BRAM was initialized to a known pattern of 0x55; and 50% of the flip-flops were initialized to 1s and 50%, to 0s. Then, the device was irradiated for a given time. Finally, a GCapture operation was made in order to capture the current state of the flip-flops (as discussed before, such

TABLE I
TECHNICAL DETAILS ABOUT RADIATION TESTS AND NUMBER OF OBSERVED BITFLIPS

			Bitflips			
Test	Campaign	Fluence	Flux	Conf.	BRAM	F-F
TN1	November 2017	0.43	1.43	56	0	0
TN2		0.48	1.62	76	0	0
TN3		1.89	2.10	278	0	2
TN4		1.26	2.10	186	0	1
TN5		2.82	2.35	383	0	2
TM1	May 2018	0.63	2.10	140	0	2
TM2		0.64	2.14	128	0	1
TM3		0.64	2.14	131	0	1
TM4		1.85	2.06	370	0	0
TM5		3.37	1.87	681	0	3
	Total	14.01		2429	0	12
		$\times 10^9$ cm^{-2}	$\times 10^6$ cm^{-2}/s			

information can be read from the configuration memory), and then, read it back for the sake of comparison with the golden values.

Radiation tests involved a single FPGA sample, but two different campaigns were made, in November 2017 and in May 2018. In each one of these, there were five different tests, which only differed in the memory contents and the radiation exposure time.

III. RESULTS

A. Identification of cell types in the FPGA

The content inside an FPGA is read by means of a bitstream with the following characteristics. First of all, GCapture forces the FPGA to copy the last state of the flip-flops in specific cells in the configuration memory, erasing whichever value was previously present. Thus, possible bitflips in those bitstream locations will go unnoticed although the fraction is negligible ($\sim N_{FF}/N_{CF} = 0.5$ %). This means that the effective size of the configuration memory to calculate the cross sections in these radiation tests is $N'_{CF} = N_{CF} - N_{FF}$ (25,484,208 bits). If GCapture had not been used to obtain the flip-flop content, the value would have been N_{CF}. The configuration memory content is merged to that of the BRAM to create the bitstream sent to the Raspberry Pi. Therefore, the total size of the bitstream is $N_{BS} = N_{CF} + N_{BR}$, 30,587,648 bits.

After every irradiation, the raw bitstream was saved on a PC for later analysis. This consisted in comparing the bit values in the bitstream before and after the irradiation. If a cell had been flipped, its position in the bitstream was saved in a text file bearing in mind that the position of the first one was 0 and that of the last one, $N_{BS} - 1$. This position will be used as address, a_i, in later analysis. Finally, addresses were sought in two files containing the full set of addresses of the BRAM and flip-flops and categorized in independent sets according to the kind of cell (flip-flops, BRAM or configuration memory).

Table I shows the neutron fluence received by the DUT in the different tests as well as the total number of bitflips observed in each type of resources of the FPGA. At the end of Nov. 2017 campaign, dynamic tests, not shown in this manuscript, were performed in the FPGA, which received $1.03{\cdot}10^{12}$ n/cm^2. The number of bitflips was higher in the second campaign leading to an increase of $\sim$20% in the SEU cross-sections. There is not a clear reason to explain this: beam flux uncertainty, aging [14] or displacement damage [15].

B. Extraction of multiple events: MBUs

As indicated in Table I, most of the errors were observed in the configuration memory, very few in the flip-flops and none on the BRAM, probably due to the presence of ECC. Initially, it was difficult to determine the multiplicity of the events that provoked the bitflips.

A first analysis that can be done is to investigate the occurrence of multiple bit upsets in the configuration memory, easily detected as two or more bitflips in the same 32-bit word. The exact number of MBUs of different multiplicities is shown

TABLE II
CHARACTERISTICS OF MBUS OBSERVED IN THE CONF. RAM

		Experimental MBUs			False MBUs		
	N_{BF}	2-bit	3-bit	>3-bit	2-bit	3-bit	Prob.
TN1	56	2	0	0	0.002	$4.0 \cdot 10^{-8}$	0.2%
TN2	76	9	0	0	0.003	$1.0 \cdot 10^{-7}$	0.3%
TN3	278	18	3	0	0.047	$5.1 \cdot 10^{-6}$	4.6%
TN4	186	16	0	0	0.021	$1.5 \cdot 10^{-6}$	2.1%
TN5	383	8	4	0	0.089	$1.3 \cdot 10^{-5}$	8.5%
TM1	140	16	1	0	0.012	$6.4 \cdot 10^{-7}$	1.2%
TM2	128	6	0	0	0.010	$4.9 \cdot 10^{-7}$	1.0%
TM3	131	10	2	0	0.010	$5.2 \cdot 10^{-7}$	1.0%
TM4	370	7	0	1	0.083	$1.2 \cdot 10^{-5}$	8.0%
TM5	681	17	8	4	0.282	$7.5 \cdot 10^{-5}$	24.5%

in Table II. However, it is advisable to rule out the accidental occurrence of several independent SBUs in the same word. According to Tausch's approach [16], the probability of observing one or more false MBUs in an FPGA is:

$$1 - \exp\left(-\frac{N_{BF} \cdot (N_{BF} - 1) \cdot (W - 1)}{2 \cdot L_N}\right), \tag{1}$$

N_{BF} being the number of bitflips, W the data wordwidth, and L_N the memory size in bits. The inner term inside the exponential function is just the expected number of false 2-bit MBUs and a similar expression can be used to determine the number of false 3-bit ones [17], [18]. The rightwards columns in Table II show the expected number of false MBUs as well as the probability of occurring at least a false MBU of any multiplicity with $W = 32$, $L_N = N'_{CF}$. The immediate conclusion is that observed MBUs cannot be explained by the simple accumulation of SBUs, so multiple events must have occurred during the experiments.

C. Extraction of multiple events: MCUs

It is possible to go beyond this approach to get a more appropriate depiction of the multiple events, namely in the configuration memory of the FPGA. In 2014, Wirthlin *et al.* discovered that some measurable statistical properties of an experiment with SBUs and MCUs are different from those observed in a theoretical only-SBU system [19]. Thus, the discrepancies can be used to group the addresses of the flipped cells in multiple events allowing a quite accurate depiction of the typology of events even without any information about the physical layout of the device. This idea was extended by the authors in other works to systematize the procedure [9], [10]. In this case, the following scheme was implemented:

1) As previously said, every flipped cell in the configuration memory was given an address, a_i, related to its position in the bitstream ranging from 0 to $N_{BS} - 1$. Flipped cells were located and their addresses, a_i, saved to create a new set, A, with integer values in increasing order. The size of A is, obviously, N_{BF}, the number of bitflips observed in the experiment.
2) The elements in A were combined in pairs to build a new set, DV, such that $DV = \{|a_j - a_i|\,,\ a_i < a_j \in A\}$. This set has $N_{DV} = N_{BF} \cdot (N_{BF} - 1)/2$ elements with values between 1 and $N_{BS} - 1$.
3) A histogram showing the number of repetitions of each element in DV was made.
4) In this histogram, some values are expected to occur more times than the rest, although repetitions can be attributed just to random fluctuations. According to the theoretical only-SBU model, the expected number of elements repeated k times can be calculated using the expression shown in the Appendix.
5) Then, a threshold value, k_M, is calculated, such that the probability of an element being repeated k_M times is lower than 0.001. Thus, values appearing k_N times, with $k_N > k_M$, are attributed to the existence of MCUs, since they are not compatible with an only-SBU scenario.
6) Elements of the DV set appearing k_M times or more are extracted. In the remainder of the paper, these values will be referred to as *"critical distances"*. It is possible that different values show up in every test so the critical distances issued from each round are merged in the final set and used to identify the multiple events.

Let us illustrate this technique with an example. In the $TM5$ test of Table I, 681 cells were flipped, from which a DV set with 231,540 elements was built[1]. According to (2), in the Appendix, most of possible values should appear once or zero

[1]All the mathematical calculations shown in this paper, either simulations or data analysis, were done using Julia 1.1.1 [20].

TABLE III
ANOMALOUSLY REPEATED ELEMENTS IN THE DV SETS

Round	DV-value (Number of repetitions)				
TN1	3233 (6)	3231 (4)			
TN2	3233 (18)	1 (9)	3232 (7)		
TN3	3233 (45)	1 (24)	3231 (19)	3232 (16)	3234 (9)
TN4	3233 (28)	1 (10)	3232 (9)	3231 (5)	
TN5	3233 (5)	3232 (18)	1 (15)	3231 (12)	
TM1	3233 (31)	1 (18)	3232 (11)	3231 (6)	3234 (5)
TM2	3233 (21)	1 (6)	3231 (5)		
TM3	3233 (22)	1 (14)	3232 (12)	3231 (7)	
TM4	3233 (50)	3231 (13)	3232 (11)	1 (7)	
TM5	3233 (86)	1 (45)	3232 (44)	3231 (41)	2 (15) 3230 (11)

times, but the expected number of elements repeated twice is 1383.2, three times 6.28, four times 0.023 and, finally, 5 times $6.9{\cdot}10^{-5}$ so the occurrence of DV-elements 5 times or more is unlikely. However, it was found in actual results that 3233 appears 86 times, 1 does 45 times, etc. (Table III). These are the critical distances to relate pairs of cells and to start to group bitflips.

Once we know the DV-elements appearing in excess, the *"self-consistence technique"* [10] was applied on each set of data to reject false positives due to the interaction of MCUs. Table III shows the anomalously repeated DV-elements that passed this test in each round. These results suggest that pairs with addresses differing in 1, 2, 3230, 3231, 3232, 3233 & 3234 should be associated with MCUs so they must be adjacent cells. It is worth to indicate that all of these values appeared in almost every round but were initially rejected by the self-consistence test, apparently very conservative, which confirms the importance of repeating a test several times in order to improve the analysis of the results.

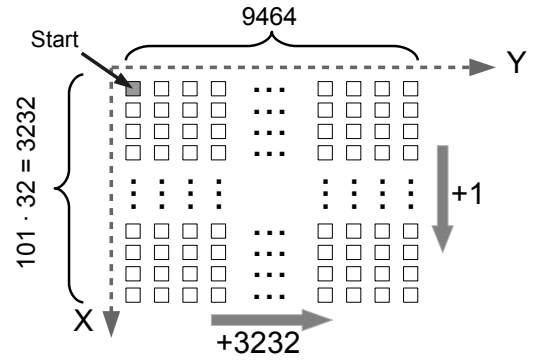
Since elements in DV were obtained by calculating the operation $|a_j - a_i|$ (a_j and a_i being addresses affected by bitflips), it is reasonable to think that flipped cells with addresses differing in 1 or 2 are associated with the MBUs listed in Table II since they are probably in the same 32-bit word. On the contrary, values (3230-3234) were quite more surprising. However, it was found out that they can be obtained as $(32 \times 101) \pm \{0, 1, 2\}$. These values have a clear correspondence with the internal memory organization of the FPGA, since the size of a frame, which is the minimal reconfiguration unit of Xilinx FPGAs, is 101 32-bit words [21]. Fig. 2(a) shows a simplified schematic of the internal organization of the configuration memory according to the information provided by the manufacturer. In a FPGA region, memory words of the same frame span vertically through a column and, as indicated in the figure, columns are transferred to the FPGA from left to right. Thus, this can be attributed to events that occurred in the same row (or in 2 nearby rows) and with a lateral distance of 0, 1 or 2 columns (Fig. 2(b)). No other anomalous values around integer multiples of 3232, such as 6464 or 9696, were observed.

Table IV summarizes the number of events of different size observed after the experiments. It is important, in any case, to determine if these events are actual or false, due to the random occurrence of bitflips in neighbor cells. In [18], it has been proposed that the average number of false 2-bit MCUs for this technique is $m_R \cdot N_{BF} \cdot (N_{BF} - 1) / L_N$, m_R being the number of critical DV distances used to relate pairs of addresses. In the worst case (TM5), this number is only 0.13, much lower than the actual value for this test (105). Therefore, false multiple events are scarce, probably absent, in these experiments.

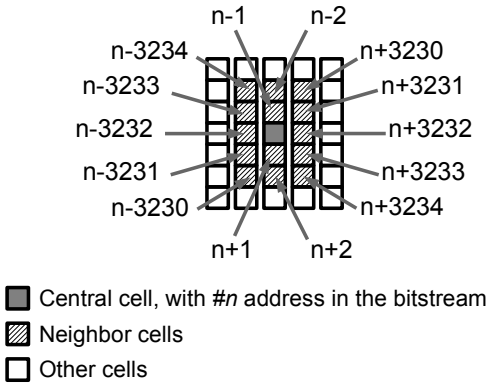
In previous works [9], [10], the statistical strategy for MCU extraction proposed the use of two different, yet complementary, mathematical operations to obtain the DV: The positive subtraction ($|a_j - a_i|$, used in this paper) and the bitwise XOR ($a_j \oplus a_i$). The latter proved to be very effective for SRAMs, such as the ones that were analyzed in those works. However, in this case the XOR operation was unsuccessful. Issued results were nonsense and they have not been included in this paper.

D. Cross sections for different events

From dividing raw results shown in Table IV and the uncertainty, derived from [22], by the fluence value and by the number of bitcells of each type (configuration memory, flip-flops), the single-event cross sections with error margins were got for all the possible multiplicities in each test. In Fig. 3, the weighted average value for each event multiplicity is shown. The absence of errors in the BRAM yields that the expected number of bitflips is lower than 3.69 with a 95% confidence [22] so the cross section for any event size is below $5.3 \cdot 10^{-17}\mathrm{cm}^2/\mathrm{bit}$, attributed to the use of ECC. In [8], a similar FPGA, probably the XC7A25T, was irradiated in different facilities with disabled ECC. The cross section for the BRAM was similar to that of the configuration memory for all the environments so the actual BRAM cross sections for 14-MeV neutrons should be similar to those shown in Fig. 3, which provide clear evidence that the embedded ECC is efficient enough to remove errors in this environment.



(a)



(b)

Fig. 2. Details about how the content in the configuration memory of the FPGA is converted into a bitstream. (a) Simplified XY-structure of the FPGA as indicated by the manufacturer. Bitstream is created concatenating columns from left to right. (b) Position of a cell with address n in the bitstream and the addresses of some of its neighbors.

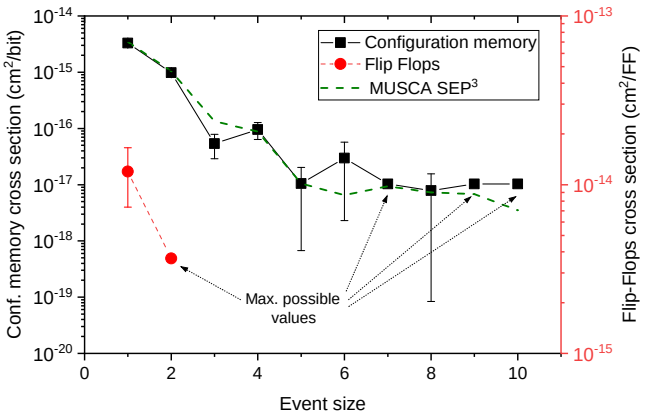


Fig. 3. Cross sections for 14-MeV neutrons according to the event size. Note that lines are related to different vertical axis. Displayed values are the weighed average of the values of all the tests. Note that there are 4 dots that are related to unobserved events in which we can only provide a maximum possible value. Finally, in dash green, the cross sections issued from MUSCA SEP3 up to 6-bit events.

TABLE IV
NUMBER OF MCUS THAT WERE EXTRACTED BY USING THE STATISTICAL APPROACH DISCUSSED IN SECTION III-C

Test	Event Size							
	1	2	3	4	5	6	7	8
TN1	35	9	1	0	0	0	0	0
TN2	31	13	1	4	0	0	0	0
TN3	142	45	1	8	1	1	0	0
TN4	108	30	2	3	0	0	0	0
TN5	230	63	1	3	0	2	0	0
TM1	57	22	5	6	0	0	0	0
TM2	74	20	2	2	0	0	0	0
TM3	63	20	1	5	1	0	0	0
TM4	231	62	1	3	0	0	0	0
TM5	390	105	9	4	0	5	0	1
TOTAL	1361	389	24	38	2	8	0	1

An interesting fact is that, for this kind of radiation, SBUs and 2-bit MCUs cross sections are on the same order of magnitude. Data indicate that about 54% of bitflips are caused by SBUs and around 32% by 2-bit MCUs. Events with higher multiplicity occur much less often. Also, it seems that the cross sections for larger events decrease with the multiplicity, but remain on the same order. There are hints as well of a higher cross section for events affecting an even number (4, 6, 8) of cells . This can be just a random statistical fluctuation due to the low number of observed events but a similar behavior has been found in other memories [23]. Finally, the SBU cross section for flip-flops is higher ($1.20 \cdot 10^{-14} \pm 4.60 \cdot 10^{-15} \mathrm{cm}^2/\mathrm{bit}$) than the one of the configuration memory (Fig. 3). No multiple events were observed involving the memory cells with the captured value of the flip-flops.

Fig. 3 also depicts the predictions issued from the tool MUlti-Scales Single Event Phenomena Predictive Platform (MUSCA-SEP3) [24], developed at the French Aerospace Lab (ONERA), in Toulouse (France). The calculations of this tool consider a dynamic neutron spectrum issued from a spectrometer (in this case, it was used for 14.2-MeV neutrons) and a technological model (i.e. elementary cell topology), determined through a technical analysis and technological parameters, based to the ITRS [25] (in this case, 28-nm bulk CMOS). One can see that the tool accurately predicts the cross sections for most multiplicities.

E. Hypothetical shape of MCUs

Accepting that Fig. 2 is accurate enough to depict the physical organization of cells in the configuration memory of the FPGA, it is possible to associate the index in the bitstream of cells in multiple events with the possible position in the XY-plane and, thus, try to study the shape of the multiple events. Tables V-VII show the observed shapes, the experimental probability of occurrence and the signature, which is the distance from the MCU cells to the reference cell, marked in dark orange in the figures, which is the cell in the MCU with the lowest index in the bitstream. Table VIII shows the shape of rare larger events, as well as their signatures.

Apparently, multiple events tend to occur along the wordline. Indeed, only events affecting one or two adjacent columns were observed but up to five rows were affected in Z8 (Table VIII). Directionality in very large events is common and it can be related to the physical structure of the arrays of cells [23], [26]. MCUs seem to be more likely if they flip pairs of cells in diagonal orientation making purely horizontal or vertical events extremely rare. Another interesting fact is that, setting the leftmost column in the FPGA as #0, corresponding to the first 101 words, if the event affected two columns, the reference cell is in an odd column for almost all of the MCUs. The only observed exception is 1 out of 391 2-bit MCUs, V2-shaped and integrally occurring along an even column. This fact points out to the existence of some physical barrier separating pairs of columns and avoiding the propagation of the events along the X-axis. On the contrary, SBUs are equally distributed showing no preference for even or odd columns.

Shapes shown in Tables V-VIII are very similar to those observed by other authors after irradiating a 28-nm Xilinx Kintex-7 SRAM-based FPGA under ultrahigh energy heavy ions [27]. This is not surprising since both devices belong to the same generation of 28-nm Xilinx's SRAM-based FPGAs. In this work, multiple events are detected with a geometric method (Euclidean distance between cells lower than $\sqrt{2}$) and occur along adjacent pairs of columns. Unfortunately, no information was provided about the probability of every shape so it is impossible to know if some event signatures are more probable

TABLE V
OBSERVED SHAPES FOR 2-BIT MCUS, SIGNATURE IN THE BITSTREAM AND PROBABILITY OF OCCURRENCE.

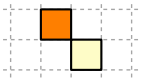
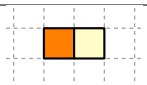
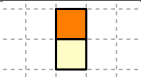
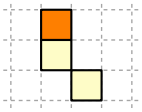
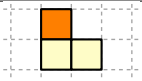
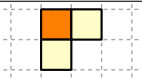
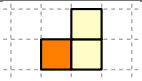
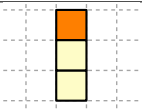
Name	Signature	Shape	Occurrence	Perc.
D2A	3231		70	18.0%
D2B	3233		265	68.1%
H2	3232		49	12.6%
V2	1		5	1.3%

TABLE VI
OBSERVED SHAPES FOR 3-BIT MCUS, SIGNATURE IN THE BITSTREAM AND PROBABILITY OF OCCURRENCE.

Name	Signature	Shape	Occurrence	Perc.
K3	1 3234		1	4.2%
L3A	1 3233		6	25.0%
L3B	1 3232		3	12.5%
L3C	3232 3233		7	29.2%
L3D	3231 3232		6	25.0%
V3	1 2		1	4.2%

than others. Finally, the authors also report that no event across three different columns was observed in concordance with the experimental results presented here.

IV. DISCUSSION

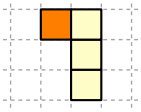
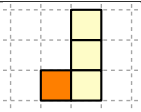
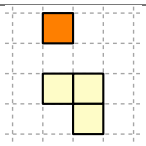
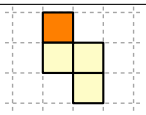
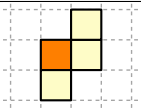
First of all, it is necessary to pinpoint the fact that the statistical method presented by Wirhtlin *et al*. for the detection of multiple events has worked in this FPGA, albeit with some changes such as the incorporation of the self-consistency principle (described in [10]), backing up this strategy. Finally, the suitability of statistical methods for different families of FPGAs has also been independently shown by Pérez-Celis and Wirthlin in a very recent paper [28].

A. MUSCA SEP3 Predictions

The MUSCA SEP3 methodology was developed by one of the authors for sequentially modelling all physical mechanisms involved in the SEE occurrence, from the system down to the semiconductor target [24], [29], [30], using results from SRIM [31], GEANT4 [32], [33] and physical models derived from Technology Computer-Aided Design (TCAD) simulations in different technology nodes. The critical charge criteria of the 28-nm SRAM-based FPGA is optimized from 14 MeV neutron experiments and its value is set to 0.5 fC.

As demonstrated in Fig. 3 by using MUSCA SEP3 it is possible to make estimations for known environments. For example, it has been predicted that the expected soft error rate due to α-particles coming from radioactive impurities is 46,800 FIT/Mbit

TABLE VII
OBSERVED SHAPES FOR 4-BIT MCUS, SIGNATURE IN THE BITSTREAM AND PROBABILITY OF OCCURRENCE.

Name	Signature	Shape	Occurrence	Perc.
L4A	3232 3233 3234		1	2.6%
L4B	3230 3231 3232		1	2.6%
S4	1 3232 3233		1	2.6%
X4 [a]	1 3233 3234		1	2.6%
Z4A	1 3233 3234		28	73.7%
Z4B	1 3231 3232		6	15.8%

[a] It could be an SBU+L3C

in standard technologies[2]. However, it is likely that the silicon used for the wafer had been purified. If so, the expected FIT decreases to 3720 FIT/Mbit in Low Alpha (LA) wafers and even to 318 in Ultra Low Alpha (ULA) ones. Concerning cosmic rays, Table IX shows the expected FIT for events of different size in Madrid (Spain), 40.41 °N, 3.70 °W, 650 m above sea level, a place with an average relative flux of 1.35 with respect to that in New York city, a classical location chosen as reference for estimating the neutron abundance on the Earth surface [34]. Atmospheric radiation fields composed by neutron, proton and muon spectra were calculated by using ATMORAD [35]. Spectra are associated with angular properties for energy sampling (neutron, proton) or from analytical functions (muon). The SER calculation combines the occurrence model validated by the 14-MeV measurements and a particle generator (Monte-Carlo) which considers the spectrum and the angular properties of each particle. Neutrons are expected to provoke 66.2% of the events, protons 27.6%, and muons 6.2%.

The contribution of the Boron concentration interacting with thermal neutrons was not considered in the calculation because it depends on the surrounding device material and this information is not available. Nevertheless, recent works have discovered that the contribution of the terrestrial thermal neutrons cannot be neglected since it can be equivalent to that from the high-energy neutron part [36]. Future works based on thermal neutrons tests and simulations are being currently conducted. In the case of a standard or LA hypothesis, the main contribution is induced by the alpha emitters. Only the increase in proton and muon contributions is likely to modify this trend.

B. Applications on SEU Injection tests

These results allow sketching an improvement of fault injection tests in FPGAs. Such tests constitute a very popular technique to verify designs running in FPGAs. However, an actual environment should be emulated in such a way that bitflips must be injected in random cells following a temporal pattern compatible with a Poisson distribution with a specific mean time between failures (MTBF) [37]. Unfortunately, to the authors' knowledge, errors are typically just injected as SBUs since it is unusual to know the relation between logic and physical addresses to flip adjacent bits. Nevertheless, the results shown in this paper allow dodging this drawback.

Fig. 3, or Table IV from which it was obtained, provides experimental data to determine the expected number of events of each type, as well as their expected abundance. Restricting the study to up to 4-bit events, the last value for which there are significant experimental data, it is possible to deduce that the ratio among 1-, 2-, 3-, and 4-bit events is 61.1:18.2:1:1.8. In

[2] 1 FIT: 1 failure per 10^9 hours

TABLE VIII
SIGNATURE AND PROPOSED SHAPE FOR LARGER EVENTS

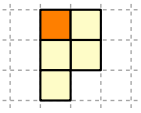
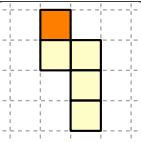
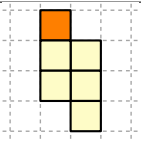
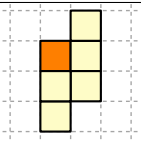
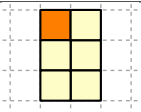
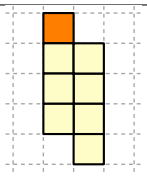
Name	Signature	Shape	Occurrences
P5	1 2 3232 3233		1
Z5	1 3233 3234 3235		1
Z6A	1 2 3233 3234 3235		4
Z6B	1 2 3231 3232 3233		3
R6	1 , 2 3232 3233 3234		1
Z8	1, 2, 3 3233 3234 3235 3236		1

TABLE IX
EXPECTED FIT FOR COSMIC RAYS, FOR THE XILINX ARTIX-7 FPGA AT MADRID (SPAIN)

Event Size	FIT	Event Size	FIT
1	1651	4	315
2	768	5	112
3	523	6	61

other words, when the system decides to inject a failure, 74.4% of injections must be an SBU; 22.2%, a 2-bit MCU; 1.2%, a 3-bit one; and 2.2%, a 4-bit event.

If the system decides to inject an SBU, a cell is randomly selected, the containing frame is read, its value flipped, and the new frame written in the FPGA.

On the contrary, if an MCU is chosen, the injection system must proceed as follows. First of all, the multiplicity of the new event is decided taking into account the probability of each, deduced from the cross section values shown in Fig. 3. Next, the shape of the event is determined according to the probabilities shown in Tables V-VII. A random cell in an odd column must be chosen to play the role of reference cell and, afterwards, the rest of cells in the emulated MCU are flipped according to the signature displayed in the tables. For this purpose, the involved frames must be read, modified and finally reloaded in the FPGA.

Obviously, experimental results are only valid for this FPGA model and for 14-MeV neutrons impinging the device with normal incidence. Thus, for instance, for other situations, such as atmospheric environments with a plethora of impinging particles, energies and angular effects, the cross section values and MCU proportions can change. However, even though this strategy does not perfectly mimic the error generation inside an FPGA, it is closer to reality than simulated experiments in which only SBUs are considered.

V. Conclusions

An Artix-7 FPGA was exposed to 14.2-MeV neutron radiation and SBUs/MCUs were extracted and discussed. In particular, MCUs involving some critical distances of 1, 2 and [3230–3234] were observed in the configuration memory. These offsets are related to this device addressing mode.

The calculated cross sections and error distribution probability will allow tuning the injection error tool developed by the authors [38] for emulating MBUs and MCUs in an accurate manner. Also, they are appropriate for use in prediction tools such as MUSCA SEP^3.

Appendix

If N_{SB} SBUs occur in a L-size memory at addresses $A = \{a_i,\ 1 \leq i \leq N_{SB}\}$, it is possible to create a new set such that:

$$DAV = \{a_i - a_j,\ a_i > a_j\}$$

In [9] & [10], it was demonstrated that:

1) The size of DAV is $N_{DV} = \frac{1}{2} \cdot N_{SB} \cdot (N_{SB} - 1)$.
2) The mean number of elements repeated m times in DAV is, with with $p_k \approx 2 \cdot L^{-2} \cdot (L - k)$:

$$N_R\left(m\right) = \left(\begin{array}{c} N_{DV} \\ m \end{array} \right) \cdot \sum_{k=1}^{L} p_k^m \cdot \left(1 - p_k\right)^{N_{DV} - m}.$$

In the previous work, the binomial expressions were replaced with the expression $(1+x)^n \approx 1 + nx$ to allow computing that expression as $N_R\left(m\right) \approx \left(\begin{array}{c} N_{DV} \\ m \end{array} \right) \cdot \frac{2^m}{m+1} \cdot L^{1-m}$. However, if we use another approach, $\sum_{k=1}^{L} a(k) \approx \int_1^L a(x) \cdot dx$, valid for slightly changing functions, the final expression would be:

$$N_R(m) \approx \left(\begin{array}{c} N_{DV} \\ m \end{array} \right) \cdot \cdot \sum_{k=0}^{N_{DV}-m} \frac{(-1)^k}{k+m+1} \cdot \left(\begin{array}{c} N_{DV} - m \\ k \end{array} \right) \cdot \frac{2^{m+k}}{L^{m+k-1}} \tag{2}$$

Unlike old expressions, this is not restricted to $N_{DV} \ll L$.

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