Evaluation of a COTS 65-nm SRAM under 15 MeV Protons and 14 MeV Neutrons at Low VDD

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***Abstract*—This paper presents an experimental study on the sensitivity of a Commercial-Off-The-Shelf (COTS) bulk 65-nm SRAM under 15.6 MeV proton irradiation when powered up at ultra-low bias voltage. Tests were run on stand-by and while reading the memory. Results show obvious evidence indicating that decreasing the bias voltage below 1 V exponentially increases the number of observed errors. SBUs and MCUs (mostly with vertical shapes according to the manufacturers' layout) are reported and their behavior is analyzed in this paper. Predictions on the SEU sensitivity obtained with the MUSCA-SEP3 modeling tool are also provided, and compared with the experimental results. These are also compared with 14.2 MeV neutrons, showing a significant difference in the cross-sections for both irradiation sources. TID tests and GEANT4 simulations were also run to check for the reason behind the difference in the cross-section between these two particles.**

***Index Terms*—COTS, SRAM, proton tests, radiation hardness, low bias voltage, reliability, soft error, TID synergistic effect.**

I. Introduction

MINIMIZING power consumption is one of the main goals in the design of modern electronic devices. On a critical system, it is not necessary to keep all the parts working full-time. Hence, some non-critical devices such as non-volatile SRAMs, are allowed to be switched off while the main parts of the system remain connected to the power supply. For the volatile memories, in order to prevent the data loss, they should be powered on at the bias voltage indicated by the manufacturer (also known as the nominal voltage). However, SRAMs can retain information even if the power supply drops down to 15-20% of the nominal value [1], minimizing the power demand. This technique is known as Dynamic Voltage Scaling (DVS), and it is commonly used in systems when low power consumption is a critical issue [2].

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It is well-known that, when the bias voltage of a memory is lowered, a new problem comes up: the critical charge to trigger Single Event Upsets (SEUs) decreases [3]. In fact, recently, the authors made a characterization of the SEU sensitivity of various COTS bulk SRAMs (with 130-nm, 90-nm and 65-nm manufacturing processes) at ultra-low bias voltages under neutron irradiation that supports this point [4], [5]. SEUs fall into two classes: Single Bit Upsets (SBUs) and Multiple Bit/Cell Upsets (MBUs, MCUs). If a part of the device that is critical for its correct operation is affected, a more serious event (a Single Event Functional Interrupt or SEFI) arises. Many other experiments have been done in the literature investigating the effect of such bias voltage variation on the behavior of academic custom D Flip-Flops, SRAM cells and manufacturing materials [6]–[11]. Proton irradiation can cause SEUs through Proton Direct Ionization (PDI) and/or by secondary particles [12]. The dependence of the SRAM sensitivity on energy levels of protons has been investigated in various studies [13]–[15]. The effect of low-energy protons on SRAMs has been also examined on various SRAM technologies mostly at nominal bias voltage [16], [17]. These studies show that SRAMs are especially sensitive to low-energy protons in comparison with high-energy ones. In [18] the effect of low-energy protons on a 32-nm SOI SRAM at low voltage is investigated.

Standard error detection and correction techniques are usually implemented in modern COTS memories, but they are sensitive to the type of bitflips: indeed they are not as efficient in dealing with multiple events as with SBUs.

Other studies in the literature have demonstrated that there is another point that should be taken into consideration while working at low voltages. In [19] it is shown that the Total Ionizing Dose (TID) can affect power consumption and threshold working voltage of the SRAM cells. It has also been shown that some memories can suffer from TID-SEE synergistic effects, which increases the sensitivity to neutrons or protons [20].

This paper explores the behavior of the CY62167GE30-4 5ZXI COTS bulk 65-nm SRAM, manufactured by Cypress Semiconductor, when powered up slightly above the minimum threshold voltage that guarantees data retention. Static and dynamic tests were made under 15.6 MeV protons. This allowed the authors not only validate the effects of DVS on this COTS SRAM, but also to establish a comparison with results obtained with 14.2 MeV neutrons in a previous work [4]. The parts were not delidded, and it was estimated that the encapsulation layer reduced the energy of protons on

the surface of the memory to something within the range 13.4−14.2 MeV.

The rest of the paper is structured as follows. First, in Section II, some information about the facility used for testing the memories and how tests have been run is included. Then the results of the experiments are reported in Section III. Section IV presents a discussion of the TID tests and the rationale behind the differences observed in the sensitivity between protons and neutrons. Finally, the conclusions are proposed in Section V.

II. Experimental Setup

The Device Under Test (DUT) was controlled by an Arduino Due, which was connected to a computer system in order to provide power and store the results. The DUT supply voltage was controlled by means of a variable voltage generator. It can provide a tunable voltage ranging from 0.05 to 3.5 V.

In order to guarantee that the observed errors were due to irradiation and not consequences of a problem in the experimental setup, the system was tested before and after the irradiation and the memory retained information at bias voltages above 0.72 V. The microcontroller is connected to the memory through a dedicated connection, whereas the data transmission to the computer was made with a USB port that virtualized the serial communication through the Universal Asynchronous Receiver/Transmitter (UART) of the microcontroller. To prevent any influence during the tests, everything in the irradiation chamber except the DUT itself was shielded with thick aluminum plates, whereas the computer was in another room for controlling and monitoring the process.

The tests were run in static and dynamic mode. The static tests consisted of five successive steps:

1) In order to observe all the SEUs that actually occurred in the memory cells, by using proprietary information provided by the manufacturer, the Error Correction Code (ECC) provided by the SRAM hardware was turned off.
2) The data are written on the memory with a specific pattern. In this case, the checkerboard patterns (0x55 and 0xAA) were used for logistic reasons.
3) The bias voltage of the memory is reduced and the device stays on stand-by.
4) The memory is exposed to radiation.
5) After irradiation, the bias voltage is restored to nominal and the memory is checked for errors.

When performing the tests on Step 3), in order not to activate over-voltage protection structures present in the memories, all the address and data buses, as well as the enable pins were set to 0. This was done only when it was necessary to change the supply voltage of the memory from nominal to low. In consequence, the data of the first address of the memory was always written to 0x00 (consequently lost for performing the experiments), whichever the pattern was. Considering the size of the memory and the fact that only 8 bits were lost, it is totally bearable to sacrifice these data to adjust the voltage.

Due to the time constraints, the dynamic mode was run only with 0x55 pattern. At first, the pattern was written on the memory in the absence of radiation. Read cycles were done for 32 minutes of irradiation and to avoid losing any event, a final read cycle was made without irradiation. Eq. (1) shows the scheme of the dynamic stress test algorithm which is similar to the March-C approach [21]. The up arrow indicates that write and read cycles were performed from the lowest address to the highest one. A deeper analysis of the dynamic mode results is provided in Section III-B.

$$\begin{aligned}\{\uparrow (W(0x55), R(0x55), R(0x55)\\ , R(0x55), R(0x55), R(0x55))\}\end{aligned} \tag{1}$$

The proton irradiation campaign took place in May 2019 at CNA (Centro Nacional de Aceleradores), Spain [22]. The experiments were performed using the external beam line installed in the 18/9 IBA compact cyclotron laboratory. The DUTs were placed at 56 cm from the exit nozzle with $100\,\mu\text{m}$ aluminum foil as window, so that the final energy at the surface was 15.6 MeV protons, whose estimated spread was on the order of 400 KeV. Irradiation was done at normal incidence to the front side of the memory. Given the thickness of the DUT packaging ($\sim$362 μm), it was estimated that the energy received by the metal memory cells of the SRAM is in the range of 13.4−14.2 MeV. The final energy of the incident beam was obtained using the energy loss data calculated with the SRIM2013 code [23]. The uniformity of the flux was better than 90% in the exposed area of interest, maintaining the flux stability within 5% during each experimental run. The medium flux used for performing the tests never surpassed $2.5 \times 10^8 (\text{p}/\text{cm}^2/\text{s})$.

The proton flux monitoring was performed measuring the beam current into an electrically isolated graphite collimator (1 cm of diameter) behind the exit window. A medium flux value was calculated in the base of the pulses registered by the counter. Finally, the fluence at the device under test was calculated depending on the exposure time for every run with an accuracy of 10%. Despite the low proton energy, the different device technologies were sensitive enough without delidding them. Previous tests also conducted by the CNA group [24] with similar devices showed that the covering (epoxy or similar) thickness on the order of 900 μm as maximum, allows working with incident proton energies on the order of 15 MeV to study single event effects in technologies below 130 nm.

The TID test was carried out in the CNA-RadLab facility, also at the CNA [25]. The irradiation system contains a Cobalt-60 gamma source with associated photon energies of 1.17 and 1.33 MeV (mean value: 1.25 MeV). One irradiation step was carried out during the campaign, achieving a total dose of 276.48 krad(Si). The dose rate was 194.2 rad(Si)/h, which is within the "low rate" window (36-360 rad(Si)/h) of the ESA standard, according to the TID Test Method [26]. The dose rate was obtained by measuring the charge with two Farmer ionization chambers (PTW-Freiburg, TM30013 model, Germany) and one multichannel electrometer, (PTW-Freiburg, T10004 model, Germany), and also considering the environmental correction factor.

The DUT was mounted on a printed circuit board which was placed into a 12×17 cm^2 filter box to be exposed to

TABLE I
RUN SEQUENCE OF THE IRRADIATION CAMPAIGN INCLUDING THE NUMBER OF SBUS AND N-BIT MCUS

Voltage (V)	Pattern	Fluence (p/cm^2) $\times 10^9$	SBUs	2-bit MCUs	3-bit MCUs	>3-bit MCUs	Affected addresses
3.00	0x55	7.4	155	35	4	0	237
2.00		9.3	229	49	7	1	353
1.50		7.4	170	32	0	0	234
1.00		9.3	296	76	2	1	457
0.95		9.3	264	58	4	0	392
0.90		9.3	345	56	2	1	467
0.85		9.3	418	71	7	1	585
0.80		9.3	508	91	7	0	711
0.75		9.3	560	60	7	3	713
3.00	0xAA	10.6	212	45	4	0	314
2.00		12.2	260	72	12	0	440
1.50		12.0	290	60	10	0	440
1.00		11.2	345	70	6	1	506
0.95		12.2	468	107	7	1	707
0.90		12.8	523	118	11	3	798
0.85		12.6	601	116	18	0	895
0.80		12.8	626	112	9	1	880
0.75		13.0	719	121	14	0	1003

radiation, in compliance with the ESCC Basic Specification No. 22900 [26]. This container had 2 mm of aluminum, and 1.5 mm of lead in the outer layer and a 5 mm front cover of polymethyl methacrylate (PMMA) to achieve the charged-particle equilibrium. The dose rate uniformity in the filter box was greater than 90%, so the uniformity throughout the memory (DUT), considering its size, was significantly larger.

III. Experimental Results

A. Static tests

Table I shows the experimental rounds and the number of SBUs and N-bit MCUs observed in each round. To estimate the sensitivity of the device it was needed to extract the number of SBUs/MBUs from the whole set of errors. Proprietary unscrambling information from Cypress was used for this purpose, which allowed relating addresses involved in the same multiple events. Any isolated bitflip observed in the memory is presented as an SBU. Affected addresses located at a Manhattan distance equal or lower than 3 were grouped in the same MCU.

Concerning the false 2-bit events derived from the combination of two independent SBUs, in [27], the authors presented a set of equations that estimate the number of such false 2-bit MCUs, as a simple function of the total number of bitflips per round, the memory size and the metric used to identify such MCUs (Manhattan distance, etc...). According to it, in the worst case, namely 0xAA at 0.75 V, the number of expected false 2-bit events was only 0.71, more than two orders of magnitude below the number of observed 2-bit events. Therefore, the occurrence of false events is negligible.

As mentioned before, two different patterns were tested and results do not show any significant dependence on them. However, due to the time constraints the two most extreme cases for patterns (namely 0x00 and 0xFF) were not tested and there might be a slight difference in the cross-sections in comparison with all these patterns [17]. At first, the 0x55 pattern was tested from 3 V down to 0.75 V. After that, the same sequence was tested with the 0xAA pattern. All types of events were more prone to occur as the bias voltage decreased.

The largest event observed in this memory was one 5-bit MCU for the 0x55 pattern and one 7-bit MCU for 0xAA. For both patterns, the multiplicity of the rest of MCUs was equal or less than 4. It has to be mentioned that no MBUs were found in the results. This is undoubtedly the result of interleaving the physical addresses by design. Also, based on [27] the probability of observing any false MBUs with this number of bitflips is very low, which is in agreement with the results.

Fig. 1 shows the relationship between the bias voltage and SBUs/2-bit MCUs sensitivity for 15.6 MeV proton and 14.2 MeV neutron irradiation. The latter were obtained only with 0x55 pattern and previously presented and discussed in [4] by the authors. These were obtained in the GENEPI2 accelerator, available in Grenoble (France) [28]. The uncertainty margins of the cross-section for larger MCU sizes with proton irradiation were so wide that it was impractical to include them. This graph also includes error bars for the experimental cross-section calculations. Said error bars were calculated counting in the beam profile (±10%), fluence accuracy (±10%) and with 95% of confidence intervals as discussed in [29].

One can clearly spot the dependency of the cross-section on the bias voltages. Both of the tested patterns with the proton irradiation showed almost identical behaviors. It is important to notice that lowering the bias voltage down to 1 V does not lead to a significant raise in memory sensitivity. However, it seems to increase drastically for the 0.75 V - 1 V range for both irradiation sources. It is shown that the SRAM sensitivity triples by lowering the voltage from nominal to slightly above threshold voltage. This is a good hint to control the limits of the DVS technique.

It can be easily deduced that the device is more sensitive to neutrons, as SBU and MCU cross-sections are one order of magnitude larger than their respective proton results.

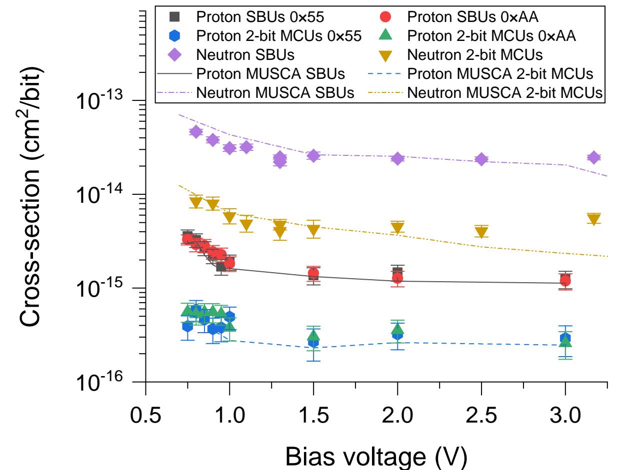

Fig. 1. SBU/2-bit MCU sensitivity against 15.6 MeV protons and 14.2 MeV neutrons [4] at various bias voltages.

TABLE II
THE NUMBER OF N-BIT MCUS OBSERVED IN DYNAMIC TESTS AT VARIOUS VOLTAGES

Voltage (V)	Total bitflips	SBUs	MCUs									Fluence $(p/cm^2)\times 10^{11}$
			2-bit	3-bit	4-bit	5-bit	6-bit	7-bit	8-bit	9-bit	>9-bit	
2.25	10940	6884	1614	182	24	8	0	0	1	0	0	3.8
2.50	4352	2760	670	61	9	1	2	0	0	0	1	2.0
2.75	6031	3829	897	103	12	0	2	2	0	1	1	2.4
3.00	7477	4688	1155	116	24	2	3	0	0	1	0	2.6
3.20	7718	4965	1149	100	10	1	2	1	1	0	0	2.7

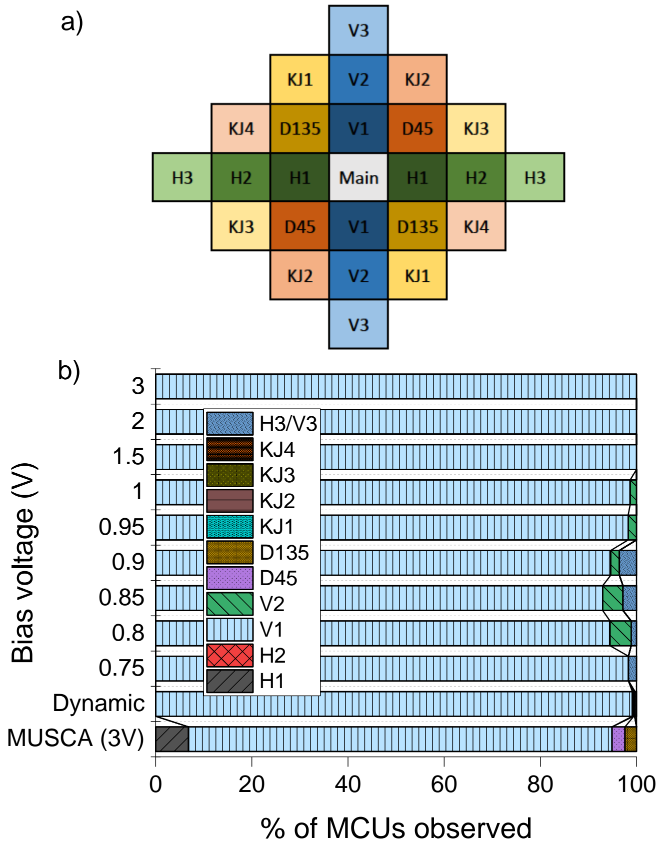

Fig. 2. (a) Possible shapes for a 2-bit MCU (Vertical, Horizontal, Diagonal, Knight Jump) and (b) 2-bit MCU shapes for 0x55 at various bias voltage

$3.57 \times 10^{-15}\mathrm{cm}^2/\mathrm{bit}$ is the highest SBU cross-section for proton irradiation which is observed at 0.75 V and with the 0x55 pattern. For neutrons the value is $4.63 \times 10^{-14}\mathrm{cm}^2/\mathrm{bit}$ at 0.8 V. There are several reasons that can explain why proton and neutron cross-sections have almost one order of magnitude in difference, to be discussed in greater detail in Section IV.

Fig. 1 also compares the results with theoretical cross-section predictions issued by the MUlti-SCAles Single Event Phenomena Predictive Platform (MUSCA-SEP3), a modeling tool developed at the French Aerospace Lab (ONERA) [15], [30]. MUSCA-SEP3 is used to predict cross-section at various VDDs showing similar behavior with the actual results, especially for protons. The difference between cross-sections of proton and neutron irradiations is clear also in the predictions.

Investigating the origin of the 2-bit MCUs led the authors to analyze the shape of this kind of event. Fig. 2 (a) shows all the possibilities for 2-bit MCUs with a Manhattan distance equal to or less than 3. There can be vertical (V), horizontal (H), diagonal (D) and knight jump (KJ) shapes with variations. These shapes can be technology-dependent and vary from device to device.

Fig. 2 (b) shows the percentage of such 2-bit MCU shapes for the static and dynamic tests and the 0x55 pattern (the 0xAA one depicted a similar behavior). At the first look, it is obvious that most of the 2-bit MCUs have vertical shapes. MUSCA predictions match the experimental observations, with some small disagreements in the prediction of horizontal-shaped events. Lowering the bias voltage increased the chance of diagonal MCUs to occur. However, the vertical shapes are the dominant kind of 2-bit MCUs in all the tests. This point has been confirmed with the manufacturer, since the well stripes of the CY62167GE-4 SRAM are organized in columns, and it is very difficult to cross them since the well doping is very high. It is, in fact, considerably stronger in the 65-nm technology than in the preceding 90-nm one, thereby leading to an almost null probability of horizontal-shaped events to occur in this technology.

B. Dynamic tests

It is reported by the manufacturer of the DUT that this memory is functional over a wide range of 2.2−3.6 V. The authors' tests showed that data can be read and written successfully within this range. 5 rounds of dynamic tests making the device working at different voltages were done. For each round the DUT supply voltage was set to a new value within the mentioned working voltage range of the memory (Table II) following the scheme described in (1), and with event rewrite: after observing any event, it was noted and the original data were restored with the correct value. In this way, error pile up from one read cycle to the next one is prevented.

Table II shows the total number of SBUs and MCUs for each supply voltage in dynamic mode. For the dynamic tests, the DUT is read and irradiated at the same time, to do so, the I/O ports need to be fed by, at least, 2.2 V to work properly. This voltage level is much higher than the minimum

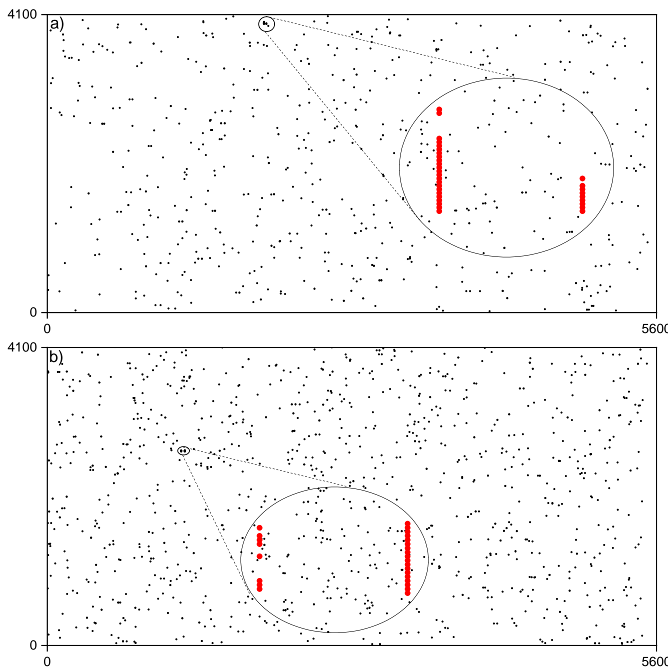

Fig. 3. (a) Observed type-A events [31] at 2.75 V and (b) at 2.5 V for the dynamic test (>9-bit in Table II). Each point is the physical position of a bitflip in the DUT, indicating the axes as X and Y in the ranges of 0-5600 and 0-4100 respectively. Expanded regions include the type-A events with dimensions of 30 × 25 (a) and 30 × 35 (b).

one that guarantees data retention. It can be observed that a) the relation of the SBUs to total bitflips is almost 79% for every voltage and b) the 2-bit MCUs have a 19% rule in total bitflips collectivity. To compare this table with Table I, two points should be taken into account. First, the total irradiation time for each row of Table II was almost 32 times higher than each static test. Second, the results of 5 read cycles added up to generate the final result for each voltage.

Since both static and dynamic tests were run under the same range of fluxes, the difference between the static and dynamic fluences (2 orders of magnitude higher for the dynamic tests) shows the contrast in the irradiation times. This can explain the higher abundance for the larger MCUs during the dynamic tests. Bitflips might be piled up within a given read cycle, which can be justified by comparing the read speed of the memory with the irradiation time. Therefore, it is postulated that many of the larger size MCUs are not originated from one single particle. Thus several SBUs or even smaller MCUs with different occurrence time would be seen as a larger MCU.

According to the estimations based on [27], the number of false 2-bit MCUs for each row in Table II comparing to the total number is negligible. In the worst case, namely at 2.25 V, the number of expected false 2-bit events was 20, for the other voltages this number is always below 10. The estimation of false events of large multiplicities is much more complex and it still remains an open problem.

There is a difference for the 2 events labeled as ">9 bit" in Table II (at 2.50 V and 2.75 V), which are events with 18 and 20 bitflips, respectively. In order to investigate this in greater detail, a bitmap plot for the read cycle containing the largest MCU sizes was created. Fig. 3 shows this bitmap for the dynamic tests at 2.75 V and 2.5 V. It can be seen that the two largest MCUs observed at the dynamic tests are vertical lines of bitflips. These are similar to type-A MCUs that were introduced in [31].

It is important to note that this type of error did not appear on the static tests. The authors also investigated the distribution of the events on the device. These were randomly scattered all over the SRAM at different bias voltages with different patterns. Therefore, plots of the events occurred at other voltages are similar to the plots in Fig. 3, with the exception of the large-scale ones.

Finally, Fig. 4 shows the SEU cross-section of the DUT for dynamic tests. In this case, it is evident that the cross-section for each SEU type is independent of the working voltage of the memory. Cross-sections for SBU and 2-bit MCU are comparable with the results of the static tests at nominal bias voltage (also shown in the figure).

Again, the shapes of 2-bit MCUs for dynamic mode results are mostly vertical with a few diagonal ones. These vertical shapes prevent the flipped bits from occurring in the same word, which would keep the memory safe from MBUs even without interleaving. Analyzing the MCU shapes with the 0xAA pattern on the memory showed almost the same behavior as 0x55.

IV. Discussion

In this section, the authors try to investigate the reason behind the difference between cross-sections of the neutrons and protons with similar energies. Loss of proton energies from 15.6 MeV to almost 14.2 MeV reaching the silicon layer of the memory might be one possible explanation. However, previous studies show that SRAM sensitivity to proton irradiation does not differ by changing the proton energy in the range of $2-100$ MeV [12], [13], [16]. Hence, even if the energy that is reaching the memory cell is around 14.2 MeV, the cross-section for protons should be the same, therefore the authors believe that this is not the main reason for the gap between both sensitivities. Another reason that can

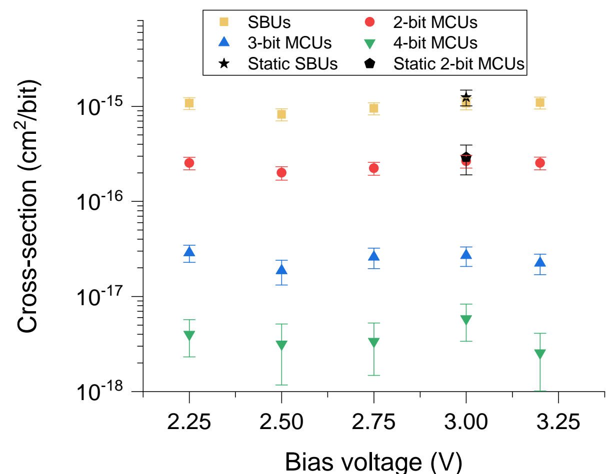

Fig. 4. Cross-section of the dynamic results at various voltages

be postulated is the existence of background particles affecting the sensitivity of the memory. In order to verify this, a TID test was run to check for gamma particle contribution to these results.

A. TID test

As mentioned before, TID can affect SRAM sensitivity to SEUs or even directly cause errors on some devices [32]–[34]. To study this phenomenon in more detail, the DUT was tested with gamma irradiation. The process took 60 days and the total accumulated dose reached 276.48 krad(Si) before dismounting the DUT. During this time, the SRAM was tested periodically and no bitflips were observed.

The same SRAM was tested before and after the dose accumulation and the results can be seen in Fig. 5. It is worth mentioning that the after-TID tests were done less than 2 hours after dismounting the memory from the gamma radiation source. It can be seen in this figure that, although the SBU cross-section for after-TID results are, in most of the cases, higher than the before-TID ones, they all fall within the 95-% confidence interval of each other. Also, it can be seen that for 2-bit MCUs and 3-bit MCUs there is almost no difference before and after the TID test. Thus, there may be hints of larger influence of TID on SBUs than on MBUs, specially at lower voltages, but further tests are necessary.

To have a deeper insight into the reason of why this is happening, the authors compared the number of each SEU type before and after the TID test, which is shown in the plots of Fig. 6. Comparing both plots shows a slightly higher contribution of SBUs in the total number of events for the after-TID test. On average, said contribution rises from 77.8% (before) to 81.5% (after), which is a 3.7% increase. For each plot, the maximum difference for SBU and 2-bit MCU contributions are about ± 10. In general, it is hard to conclude from Figs. 5 and 6 whether or not TID had some effects in the SBU/MCU distribution of events. However, it can be concluded that the one order of magnitude difference in the cross-sections is not coming from the TID effects.

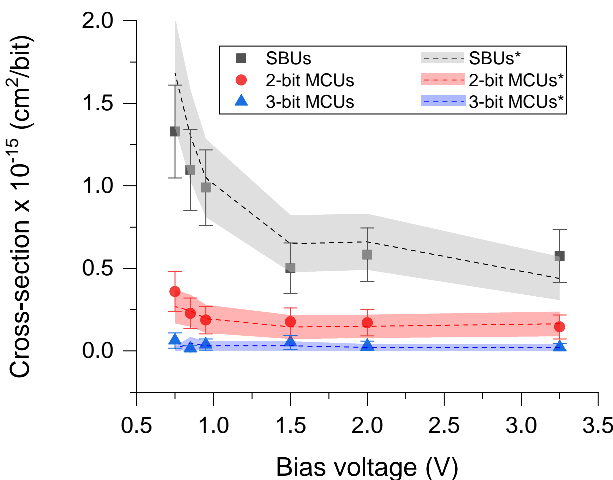

Fig. 5. Cross-section of the memory before and after TID on various voltages. * The tests after the TID test

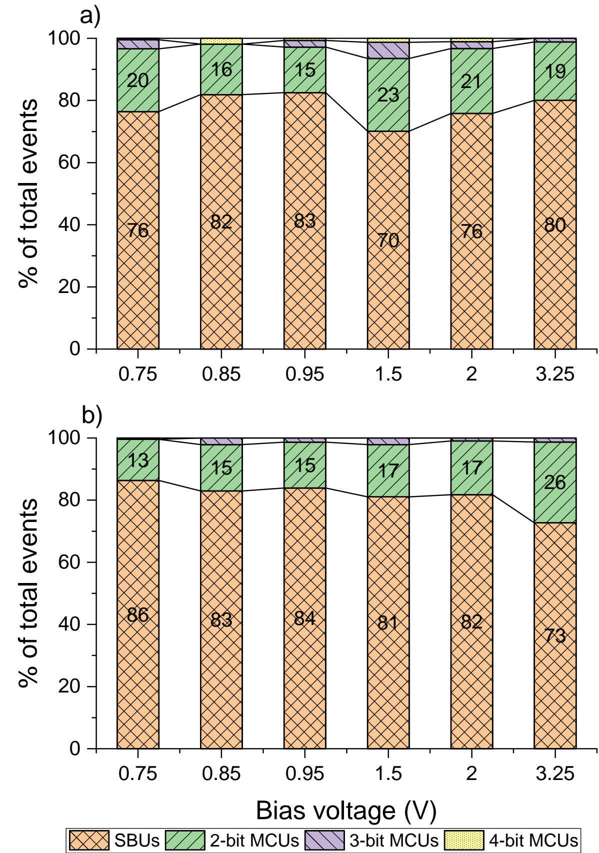

Fig. 6. Contribution of each SEU type in total number of events before (a) and after (b) the TID test

B. Difference in cross-sections between protons and neutrons

The above subsection allowed concluding that gamma irradiation could not explain the significant sensitivity difference between protons and neutrons observed in Fig. 1. This subsection gives more insight into this phenomenon. In a recent study, Han et al. [35] compared the memory sensitivities against these particles in the range of $1-1000$ MeV using GEANT4 simulations. This study can be used to extract some conclusions for the proton/neutron energies that are object of study in this paper in a qualitative way.

According to [35], the SEU cross-section of protons above and at 30 MeV can be considered equivalent to neutrons. However, below 30 MeV the cross-section of protons is lower than neutrons and the difference increases for lower energies. Several reasons are mentioned to explain this difference. First, a higher cross-section for neutron nonelastic reactions in silicon compared to the proton one. Second, neutron nonelastic events can deposit more energy than the proton ones on the whole. Finally, neutron SEUs have a smaller threshold energy than the proton ones do at this lower range of energies. Another interesting phenomena was observed in [35] that is more relevant for the results presented in this paper: there exists a bump in the neutron SEU cross-section at 14 MeV. Similar to previous observations, this can be related to the relatively large neutron nonelastic cross section around that energy. Thus, the equivalent LET dramatically increases for

neutrons whose energy is close to 14 MeV.

In order to investigate the reason for the difference in the proton and neutron cross-sections in a quantitative way, the authors also performed simulations using GEANT4. The probability of interaction of 14 MeV protons and neutrons with Silicon nuclei is $1.01 \times 10^{-5}\mu\mathrm{m}^{-1}$ and $8.69 \times 10^{-6}\mu\mathrm{m}^{-1}$, respectively. Therefore, the difference observed in the SEU sensitivities between both particles cannot implicate these interaction probabilities.

Conversely, the angular and energy properties of the secondary ions (SIs) generated by these nuclear reactions are very different depending on whether neutrons or protons are involved. Thus, characteristics of SIs from the 14 MeV neutrons and protons induced elastic and nonelastic reactions in silicon were investigated by using GEANT4 simulations. SIs created by such nuclear interactions can range from H to P, including several isotopes. 10^4 interactions were considered with normal p/n incidence and simulations provided the secondary ion count, atomic and mass numbers, their energies and directions. For the latter, a Cartesian coordinate system was considered, and the output direction of each particle interaction is a unit vector whose projections over the axes X, Y and Z are V_x, V_y and V_z, respectively. It is assumed that the direction of the incident particle is (V_x=0, V_y=0, V_z=1).

Fig. 7 presents in (a) the cumulative relative frequency of V_z and in (b) the relative frequency of SI energy restricted to atomic number higher than 11. V_z values in the range $(0-1]$ correspond to SIs emitted in the direction of the incidence angle, while angles less than 0 imply SIs emitted in an opposite direction. A 0-value would therefore indicate that the SI is emitted perpendicular to the incident particle. Results presented in Fig. 7(a) show that, for neutron interactions, SIs are emitted in all directions while proton ones induced exclusively SIs in the direction of the incidence angle. This shows a first difference between neutrons and protons, which one can imagine that the consequence on the SEU sensitivity is significant. However, this difference is not sufficient to explain the order of magnitude observed experimentally in Fig. 1 (and also confirmed by MUSCA-SEP3).

To complete the analysis, Fig. 7(b) shows that SIs induced by neutrons have a higher energy than protons. This difference is significant too, on the order of a factor of 2.5 for the highest energies. Thus, once a SEU sensitivity threshold is considered (i.e. for the MUSCA SEP3 simulations), it has an important impact in the neutron cross section. Considering the same particle fluence, while few protons will be likely to induce SEUs, many neutrons will be possible to do so.

Albedo neutrons were also considered as they also significantly increase the neutron cross section, as shown in recent works [36], [37]. Indeed, neutrons are attenuated as they interact with nuclei in the matter, and they can induce the re-emission of particles able to reinforce the local spectra. Cascade neutrons (i.e., with energy higher than 20 MeV) colliding with nuclei produce fast neutrons (on the order of 1 MeV) which are moderated to epithermal and thermal ones as they travel and interact with the elements of the room. One of them is concrete, which is used to build the walls of facility test rooms. Another one is polyethylene, typically

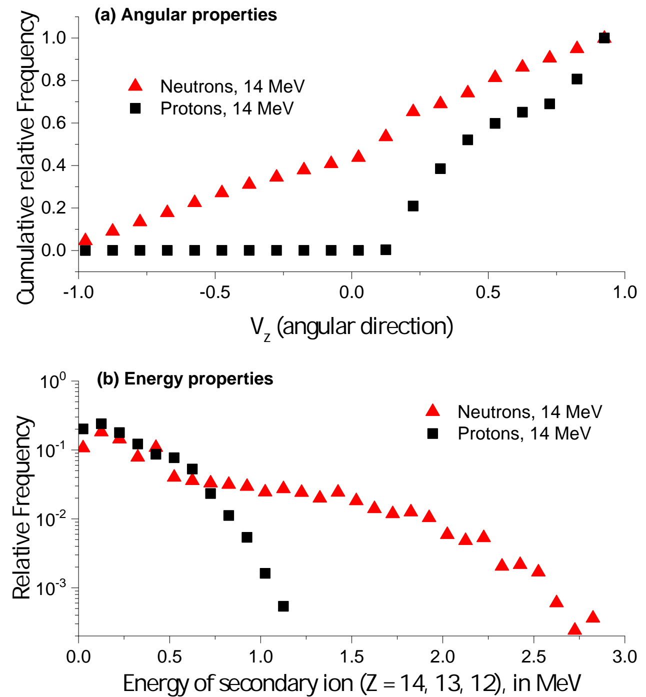

Fig. 7. (a) Cumulative relative frequency of V_z and (b) relative frequency of secondary ion energies, restricted to atomic numbers higher than 11

used to protect some parts of the SEE test boards. The latter was used for the neutron experiments of [4], fairly close to the DUT (∼40-50 cm.), which was not the case for the proton tests. A first study, made in [37], revealed that the neutron spectra ranging from 0.1 MeV to a few MeV are reinforced because of the albedo neutrons issued from collisions with concrete and polyethylene. These low-energy neutrons have a high impact in the device SEE sensitivity, as recent studies have pointed out [38]. Another preliminary analysis of the SEU contribution of 14 MeV neutrons made with MUSCA-SEP3 on this COTS SRAM showed a 1.9X increase if albedo is taken into account. This study is out of the scope of this work, but it is clear that it should be investigated in depth.

Therefore, the difference in cross-sections between protons and neutrons observed experimentally can be attributed firstly to nuclear reaction properties and secondly by the scattering/albedo neutrons induced by polyethylene shielding and concrete chamber walls. Thermal neutrons were not considered in these investigations. Nevertheless, if the device contains a borophosphosilicate glass (BPSG) passivation layer, it is likely that thermal neutrons induced by material environments (facility, protection of SEU tester board, etc.) further increases the SEU sensitivity under the neutron beam.

The existence of a bump for 14 MeV neutrons was predicted in [35]. Even if the neutron tests were not performed over a wide range of energies, a comparison between cross-sections of 14 MeV neutrons and 14 MeV protons will surely reveal a very similar phenomena. According to [35], this can lead to important mispredictions in the assumption that the SEU cross-sections vary with energy following the Weibull fit (or the Bendel model).

V. Conclusions

Experimental proof of sensitivity of the CY62167GE30-4 5ZXI bulk 65-nm COTS SRAM, when powered up at low bias voltages at static and dynamic modes against 15.6 MeV protons is presented in this paper. Under natural conditions, the memory is fully functional with bias voltages above 0.72 V and up to the nominal voltage established by the manufacturer. SBUs and MCUs were detected at all the bias voltages. Vertical shapes are shown to be the dominant 2-bit MCUs and no MBUs were observed with this memory.

An interesting result was the 15.6 MeV proton/14.2 MeV neutron SEU sensitivities being 1 order of magnitude apart, for particles with almost the same energies. Comparisons with MUSCA-SEP3 show a very good agreement between experimental results and predictions. The difference observed between both particles was explained by higher energies of secondary ions produced by neutrons and their direction (studied with GEANT4), as well as a bump found and analyzed at about 14 MeV neutrons in a previous work [35].

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