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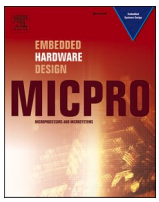

SEE sensitivity of a COTS 28-nm SRAM-based FPGA under thermal neutrons and different incident angles

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ABSTRACT

This paper provides an experimental study of the single-event upset (SEU) susceptibility against thermal neutron radiation of a 28-nm bulk Commercial-Off-The-Shelf (COTS) Xilinx Artix-7 FPGA under different angles of incidence. Experimental results indicating SEUs on configuration RAM (CRAM) cells, Flip-Flops (FFs), and Block RAMs (BRAMs) are presented and discussed. Shapes of multiple events (ranging from 2 to 12-bit) are also analyzed, and their dependency on the incident angle of the particle beam against the device's surface. Possible shapes of 128 and 384-bit multiple events are also investigated, revealing a trend to follow word lines. The results of the front incident angle are compared with 14.2-MeV neutrons, demonstrating a considerable difference in the device's sensitivity against both irradiation sources. Finally, a modeling tool called MUSCA-SEP3 is used to predict the device's sensitivity under the same environmental conditions. The obtained experimental results will show a good agreement with the predicted ones in a very accurate way.

1. Introduction

In recent years, a state-of-the-art trend has emerged in space activities to present a new essence to the space ecosystem by developing used technologies and approaches in the traditional space industry; it refers to "New Space." Hence, new companies pursue flexibility, economical, and high-performance devices as they play a significant role in space missions. Among these, Commercial-Off-The-Shelf (COTS) devices are growingly used in critical demands due to satisfying these criteria [1]. These factors make COTS Field Programmable Gate Arrays (FPGA) suitable for space applications. Some FPGAs based on Static Random Access Memory (SRAM) is widely deployed in satellites and other spacecraft.

On the other side, the effects caused by space radiation are a growing issue that poses a threat to the proper function of COTS SRAM-based FPGAs. Indeed, particles such as protons and neutrons existing in aerospace environments can induce Single Event Effects (SEEs). If a single ionizing particle changes the state of one or several bitcells, Single Event Upsets (SEUs) happen. They can be classified according to their multiplicity. If the impinging particle impacts only one memory cell, a Single Bit Upset (SBU) occurs. In contrast, a Multiple Cell Upset (MCU) appears if several physically adjacent bitcells are altered. If bitcells in the same word are affected, a Multiple Bit Upset (MBU) occurs. Therefore, it is worth researching such SRAM-based devices' behavior under radiation effects.

Various research works have studied SRAM-based FPGAs under radiation to evaluate their reliability. Authors in [2] performed tests on a Xilinx 28-nm bulk Zynq-7000 to measure its SEE sensitivity vs. Linear Energy Transfer (LET) of heavy-ions for its Configuration RAM (CRAM) and Block RAM (BRAM). Results reveal that, for LET values higher than 12 MeV/mg/cm^2, MCUs and MBUs were observed. Researchers in [3] performed experiments also on a the Xilinx Zynq-7000 under very-high energy heavy-ion radiation and provided an analysis of the SEE vulnerability. The research demonstrated various SEE phenomena. In [4], the main contribution was the investigation of the angular effects with low-LET heavy-ions on the SRAM cells of a 28-nm bulk SRAM-based Artix-7 FPGA, which is the same device that is used in this work. Notable differences were also reported in the MBU cross-sections

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of CRAM and BRAM memory cells under particles striking the device with different incident angles. Lee et al. [5] presented Soft Error Rate (SER) predictions for a Xilinx Kintex-7 XC7V325T FPGA with emphasis on the importance of angular testing, and proposed a method to extend existing error estimation tools. Du et al. [6] also made tests on the same device by employing an ultrahigh energy heavy-ion beam at CERN. Clusters of multiple large-scale events were observed with different multiplicities happening in the CRAM.

Experiments using high-energy electrons have also been conducted on FPGAs. In [7], authors investigated the electron-induced soft errors in a 28-nm bulk SRAM-based FPGA with energies above 9 MeV. The single event upset rate for the memory cells in the FPGAs was between 10^{-20} and 10^{-17} cm^2/bit. The same authors also considered the sensitivity under 20-MeV electrons of different FPGAs (a Xilinx 45-nm Spartan-6 XC6SLX16 and a 28-nm Artix-7 XC7A100T) at the LINAC facility [8]. The electron-induced SEU cross-section for the memory cells in the FPGAs was found to be between 10^{-18} and 10^{-17} cm^2/bit.

Neutron-induced SEEs on this kind of FPGAs have also been studied. For instance, Bruni et al. [9] have studied the effect of power dissipation on a Xilinx 28-nm Zynq-7000 XC7Z020-CLG484-1. The experiments show that the temperature variation induced by a higher operating frequency impacts the CRAM cross-section. In [10], Fabero et al. researched the response of a 28-nm SRAM-based Artix-7 FPGA against 14.2-MeV neutrons and analyzed the observed events using a statistical method. Researchers in [11] examined a Kintex-7 FPGA in the ATLAS Liquid Argon (LAr) Calorimeter at CERN against a broad spectrum of neutrons, protons, heavy-ions, and high-energy hadrons. The obtained results demonstrate that upsets occur at a rate of 1.1×10^{-10} upsets/-bit/s in the CRAM and 9.6×10^{-11} upsets/bit/s in the BRAM. Rezzak et al. considered the SEE response of a 28-nm SONOS Polarfire MPF300TS FPGA, under neutrons and protons [12]. The response of this device against neutrons and protons showed immunity against SELs and no configuration upsets.

Finally, another significant contribution to the total SER is associated with interactions between Boron-10 (^{10}B) isotopes (present as a p-donor in silicon used to manufacture modern nanoscale devices) and thermal neutrons (also known as slow neutrons). Thermal neutrons are a distinct source of soft errors since they can interact with the ^{10}B. When ^{10}B reacts with these, an alpha particle and a lithium-ion are formed, thereby provoking SEEs. All memories and logic devices below 65-nm contain ^{10}B [13, 14], which makes them sensitive to thermal neutrons.

A few works have investigated SEEs induced by thermal neutrons on state-of-that-art FPGAs. Tsiligiannis et al. [15] carried out tests on a 28-nm FPGA under a mixed particle field at CERN. They showed a significant influence of thermal neutrons on CRAM and BRAM cells. Recently, Scialdone et al. [16] revealed that the PolarFire FPGA exhibits a high sensitivity against thermal neutrons due to existing the ^{10}B in the device. Another recent work [17] evaluated the sensitivity of a 28-nm Xilinx Zynq-7000 FPGA against a mixed particle beam composed of thermal, epithermal and fast neutrons. However, this beam could not categorize the SEE sensitivity of that device against these 3 types of neutrons separately.

The first contribution of the present work with respect to the state of the art is to explore the sensitivity of a Xilinx 28-nm SRAM-based Artix-7 FPGA under thermal neutrons impinging at different incident angles. For this purpose, the statistical method presented in [18] was used to classify simple and multiple events observed in the CRAM, BRAM and Flip-Flops (FFs). The second contribution is a comparison of this device's sensitivity between thermal neutrons and 14.2-MeV neutrons. Finally, the third contribution of this article is a validation of the experimental data with predictions issued from a prediction tool called Multi-Scales Single Event Phenomena Predictive Platform (MUSCA SEP3), which has been developed by researchers at the ONERA research center.

Also, this work is an extended version of the Latin-American Test Symposium (LATS) conference paper [19]. The extra contributions of this work with respect to [19] are:

- A discussion of the sensitivity of the studied device against 3-bit MCUs and MBUs.
- The discussion of the shapes of the MCUs, including 2 to 12-bit multiple events, as well as 128- and 384-bit ones, which are presented in Section 0.
- A comparison between the sensitivities of this device against thermal neutrons and 14.2-MeV neutrons that is made in Section 0 (thermal neutrons were only discussed in [19]).
- The Monte-Carlo simulations obtained with with MUSCA-SEP3 and the related discussion provided in Section 0.

This work is organized as follows: Section 0 presents the experimental setup. Section 0 demonstrates the experimental results. Single and multiple event extraction, the shapes of the observed MCUs, comparison of obtained results with 14.2-MeV neutrons, and obtained results by MUSCA are reported in Section 0 . Concluding observations are finally provided in Section 0.

2. Experimental setup

Experimental tests were carried out in March 2021 on an Artix-7 XC7A100T FPGA embedded into a Nexys-4 DDR board. The device organizes 15,850 logic slices, each with four 6-input Look-Up Tables (LUTs), 8 FFs, and 4,860 Kbits of fast BRAM, from which 540 Kb to execute Error Correction Code (ECC) and six clock management tiles.

The experiments were conducted at the new Thermal and Epithermal Neutron Irradiation Station (TENIS) located at Institut Laue-Langevin (ILL). Thermal neutron experiments were performed at the Platform for Advanced Characterisation of Grenoble (PAC-G) [13, 20]. The Monte-Carlo N-Particle (MCNP) calculated neutron energy spectrum TENIS beamline with a high flux reactor is shown in Fig. 1.

A captured flux of 2.86 × 109 n/cm2/s employing gold foil activation at the beam exit was measured. An estimated captured flux of 2.1 × 109 n/cm2/s gained since the sample position was 49.4 cm away.

A control computer is connected to the DUT through a USB-to-JTAG connection to run the tests. Authors modified a version of OpenOCD software [21] to implement the GCapture instruction and the readback operation [22] to communicate with the FPGA. These modifications allow to read back the whole FPGA's configuration memory and even frame by frame. By performing a GCapture operation before the readback procedure, reading the actual state of the FFs in the design is

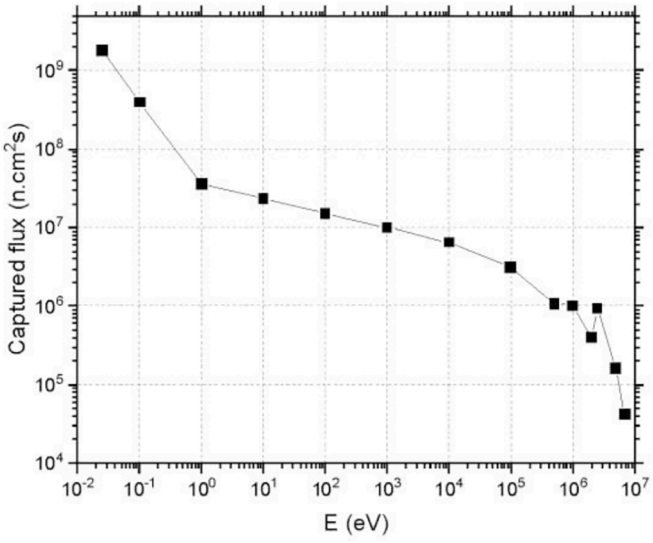

Fig. 1. MCNP calculated neutron energy spectrum on TENIS beamline with high flux reactor.

possible.

The FPGA was irradiated with four incident angles. These are depicted in Fig. 2: Normal front and back incidences, grazing angles in two directions (East-West (EW) and North-South (NS)), 45°, and 135°. The following stages were used for each test:

1 The target design is firstly loaded. This bitstream will be later referred to as "golden" since it contains the information that has not been corrupted by radiation. This design was a large shift counter using 126,800 FFs, which is 63% of the total FFs of the FPGA. No more than this amount of FFs could be used in the design, since the Xilinx Vivado tool [23] could not synthesize and implement it otherwise. In the HDL code itself, 50% of these FFs were initialized to 1′s and the rest, to 0′s.
2 To initialize each byte of the BRAM with a 0 × 55 pattern. This was done by manually, again by modifying the HDL code itself of the design.
3 To irradiate the device at fluences ranging from 0.87 × 1011 to 6.30 × 1011 n/cm2 in rounds of 1, 2, and 5 min.
4 To perform a readback of the whole CRAM and save it in the control computer, in a binary file.
5 To get the actual status of the FFs in the design. For this purpose, a GCapture command followed by another readback of the CRAM is executed. The GCapture copies the bits from the FFs of the FPGA architecture into some specific bits of the CRAM. Subsequently, it was possible to locate these specific bits by using the .ll file generated during synthesis (this is explained in Section 0).
6 Finally, the two files that were obtained in Steps 4 and 5 are compared with the "golden"' CRAM values. On the one hand, the differences between the first readback (Step 4) and the "golden"' give the bitflips occurred in the CRAM. On the other hand, the differences between some specific bits from the second readback (which are extracted with the .ll file as explained in Step 5) and those of the "golden" show the bitflips occurred in the architectural FFs of the FPGA.

3. Experimental results

This section explains the extraction methods of information retrieval from the FPGA, as well as the experimental rounds of irradiation that were carried out.

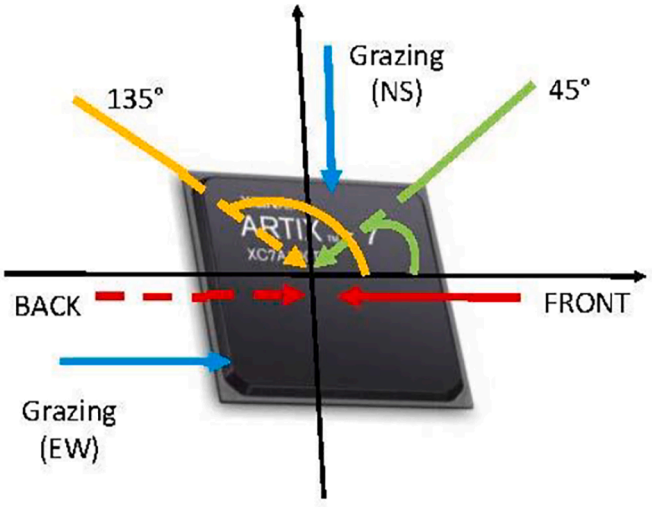

Fig. 2. Beam incident angles that were tested.

3.1. Extraction of the bitflips occurred on the FPGA

When carrying out the first *readback* (Step 5) in Section 0, the whole contents of the CRAM of the FPGA are retrieved, which can be saved in a binary file. Hence, by comparing this file with the "golden" bitstream (Step 1 in Section 0) one can obtain the bitflips that occurred in the FPGA's CRAM.

Then, when a *GCapture* + *readback* are carried out, another binary file can be generated, this time containing, in some specific locations, the values of the FFs of the FPGA's architecture at the moment of carrying out the *GCapture* (i.e., after radiation). The specific locations of the values of the FFs can be retrieved by using a *logic location* (.ll) file, which is generated by Vivado through the synthesis and implementation of the design.

Said .ll file is a flat text file containing one line per physical latch or BRAM bit existing in the FPGA architecture that is used in the design. Each of these lines provides the following information:

1 The bit offset of the current latch/BRAM bit with respect to the beginning of the data payload of the FPGA's programming file (i.e., . bit file) that is written on its CRAM.
2 The frame number (F) + bit offset with respect to F, which is used to access the content of that same latch/BRAM bit in the FPGA architecture.
3 The name of the involved latch/BRAM bit, which is the same as the name given by the HDL programmer for that bit of information.

By using the information in items 1) and 3) from the previous list, it is possible to extract the data stored in all latches from the whole information that is retrieved through this second *readback*. This information is then compared with the initial values that were written on the FFs in Step 3) of Section 0 in order to check if there were bitflips on them.

3.2. Rounds of irradiation

Table 1 shows 17 rounds of irradiation that are categorized into six types depending on the incident angle. The number of observed bitflips in CRAM and FFs is approximately proportional to the particle fluence. Most bitflips appeared in the CRAM, a few in the FFs. The authors observed no bitflips in the BRAM due to the embedded ECC in memory modules, which could not be disabled.

In these tests, many bitflips, several thousand in some cases, were observed, although the exposure times were short (5 min maximum). In this situation, two or more independent bitflips can be misled with multiple events if they randomly occur in close cells. Therefore, a correct understanding of these results is critical to extracting single and multiple

Table 1
Irradiation rounds and number of observed bitflips.

				Bitflips	
N	Beam Angle	Fluence	Flux	CRAM	FFs
1	Normal incidence (Front)	1.26	2.1	7,360	25
2		2.52	2.1	14,275	47
3		6.30	2.1	29,829	98
4	Normal incidence (Back)	1.26	2.1	5,040	14
5		2.52	2.1	10,077	32
6		6.30	2.1	25,356	97
7	45	0.921	2.17	5,439	27
8		1.84	2.17	11,181	46
9		4.60	2.17	26,888	83
10	135	0.87	2.05	4,791	16
11		1.74	2.05	9,565	29
12	90°-EW	1.26	2.1	900	3
13		2.52	2.1	2,089	11
14		6.30	2.1	8,178	22
15	90°-NS	1.26	2.1	1,395	2
16		2.52	2.1	2,652	8
17		6.30	2.1	6,598	20

events from the bulk set of bitflips. The following sections discuss the so-called "false MBU" extraction and MCU/SBU category.

4. Discussion

4.1. Extraction of MBUs

Table 2 reports the observed MBUs in the same 32-bit word (as per the Artix-7 addressing mode). Experimental MBUs in the table are displayed according to their multiplicity. As noted earlier, due to a large number of detected bitflips (N_{BF}), the probability of two or more independent bitflips randomly involving the same word is not negligible. The number of these "false MBUs" was assessed by using the mathematical expressions presented by the authors in a previous work [18].

The false MBUs are also declared in Table 2. It can be concluded that all observed experimental MBUs are not false ones. As an example, in round 1, 314 2-bit MBUs were seen; only 32.78 of them are considered to be false ones employing the mathematical method in [18].

The per-bit cross-section plots of 2 and 3-bit MBUs at different incident angles in the CRAM are presented in Fig. 3. Error margins with 95% confidence are also included in the figure, as explained in [24]. More details about how these cross sections are calculated, as well as how they are proportional to the SER are provided in the.

The relevant finding in Fig. 3 is that there are notable differences in the MBU cross-section depending on the incidence angle. Thus, the highest 2-bit MBU cross-section is obtained for the front direction and 135°, the lowest one being for 90°. The 3-bit MBUs follow a similar trend, with the possible exception of the 135° and 45° cases. This might be due to the low number of such events not being high enough to extract statistically strong conclusions.

4.2. Extraction of SBUs and MCUs

In most cases, researchers are unaware of the physical structure of memory or FPGAs; due to being protected by the manufacturers. In this study, the authors utilized a statistical method to classify SBUs and MCUs with various multiplicities from the set of bitflips. Wirthlin et al. in [25] firstly introduced an analytical technique to extract MCUs from SEUs. Authors in [26, 27] further expanded that method to determine multiple events by operating all addresses affected by radiation with a binary operator (XOR or positive subtraction) and, on such obtained elements, extract those that are anomalously over-represented with respect to a theoretical environment where only SBUs can occur. In the case of these experiments, it was remarked an irregular abundance of pairs of addresses varying in 1, 2, 3230-3234, and 6462-6466.

Values 3230-3234 can be obtained as $(32 \times 101) \pm \{0, 1, 2\}$; and

Table 2
Characteristics of MBUs observed in the CRAM.

	Experimental MBUs			False MBUs	
N°	2-bit	3-bit	> 3-bit	2-bit	3-bit
1	314	57	20	32.78	0.069
2	674	124	55	123.32	0.47
3	1,076	292	122	538.48	3.94
4	230	41	14	15.38	0.021
5	465	69	29	61.45	0.172
6	1,338	235	96	389.09	2.53
7	257	37	20	17.9	0.027
8	515	226	32	76	0.206
9	1,459	235	79	437.53	3.039
10	227	35	3	13.89	0.019
11	494	57	36	55.36	0.14
12	26	5	3	0.49	0.00014
13	73	8	10	2.64	0.0017
14	369	59	19	40.56	0.094
15	47	12	0	1.18	0.0005
16	135	27	10	4.25	0.003
17	296	61	20	26.34	0.048

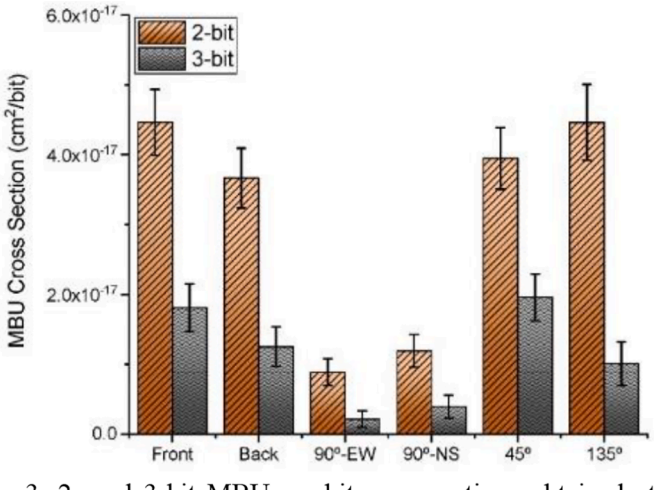

Fig. 3. 2- and 3-bit MBU per-bit cross-sections obtained at different incident angles in the CRAM.

6461-6466, as $(2 \times 32 \times 101) \pm \{0, 1, 2, 3\}$. This is related to the fact that, in Xilinx FPGAs, a frame has 101 32-bit words [28]. Thus, the large-scale events suggest MCUs affecting physically close bits, but belonging to different frames. For illustrative purposes, Fig. 4 shows a scheme of the inferred physical structure of Xilinx Artix-7 FPGAs, as the authors are not aware of the actual one. The 101 words existing in the same frame are organized vertically in the same column, in such a way that the same bit of a word in the following (or precedent) frame is 3232 bits away, and 6464 bits away if considering 2 frames apart. Therefore, if bits n, n+3232 and n+6464 were simultaneously affected by a particle, values 3232 and 6464 would be yielded if subtracting the addresses bound to those bits. A similar reasoning can be given for the rest of the values in the ranges of values 3230-3234 and 6461-6466.

MCUs with multiplicities ranging from 2 to 128 were identified in each test. Fig. 4: Location of a cell with address n in the bitstream and the addresses of some of its neighbours shows the observed MCUs in each case. It seems that different sizes in MCUs are generally seen in all directions, with the exception of the largest events. Events with higher multiplicities occur much less frequently, and it was particularly surprising that MCUs in the form of clusters of 128 and 384 (=128 × 3) bits

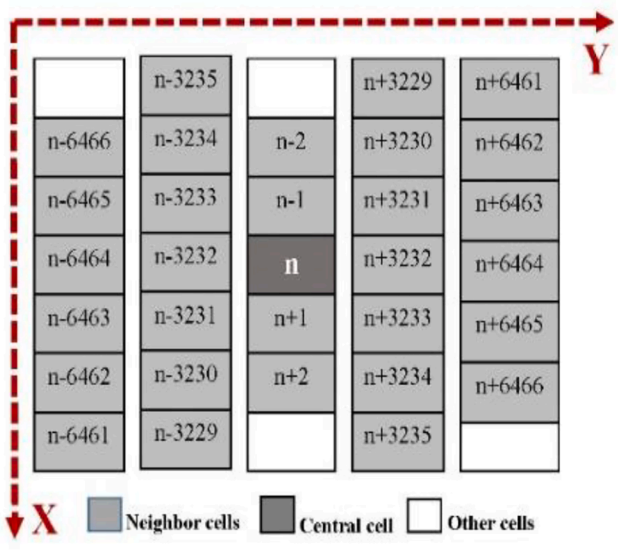

Fig. 4. Location of a cell with address n in the bitstream and the addresses of some of its neighbours.

were also detected. Authors suspect that these were Single Event Functional Interrupts (SEFIs) related to errors that emerged in the clock distribution elements or input/output buffers (IOBUFs) of the FPGA.

Fig. 5 shows the 2 and 3-bit MCU cross-sections of all the 6 possible types of experiments (classified by incident angle and direction), once the MCUs were deduced from the set of observed SEUs. Similarly as with the "false MBUs" discussed in 00, the methodology presented in [18] was used to estimate the number of 2- and 3-bit "false MCUs" expected to be in the experiments and to correct the results. Considering the results, it is concluded that the device had the highest MCU sensitivity at 45°, 135°, and the front direction, and the lowest at grazing angles. The back direction is in between them. This is in agreement with the results regarding MBUs presented in Fig. 3: 2- and 3-bit MBU per-bit cross--sections obtained at different incident angles in the CRAM, but at the same time it contradicts the results that the authors obtained in a previous work [29] with 14-MeV neutrons on a 130-nm bulk memory, where the highest MCU sensitivity was measured at grazing angles.

Fig. 6 shows the sensitivity of FFs. The figure only exhibits the SBU cross-section since FFs are not logically arranged into larger words because they are sparse. In addition, it demonstrates the comparison of the SBU cross-sections of CRAM cells with that of FFs. On the one hand, the sensitivity trend belonging to the incidence angle is similar to those detected in Fig. 4 and Fig. 5 (highest for 45°, 135°, and the front direction, lowest for grazing angles, and in between these, the back direction). Also, the FFs indicate the highest sensitivities of CRAM cells. It is worth mentioning that CRAM and FFs cross-sections are in the same order of magnitude

4.3. Shape of MCUs

The shapes of the MCUs are also presented in this investigation. The types of 2-bit MCUs were reported in Fig. 7. The shapes include a horizontal one (H2), two vertical ones (V2 and V2B), two diagonal ones (D2A and D2B), and two types of events in a chess-like knight-jump move (KJA and KJB). Fig. 8 displays an abundance of these for the six classes of tests. The most abundant type of 2-bit MCU in all the cases was the D2A, followed by D2B and H2. Verticals and the knight-jump ones occurred very few times.

This study also reports the 3-bit MCUs. 43 different types of such multiple events were detected, as displayed in Fig. 9. The authors suppose some of these possible shapes might actually be false events resulting from the interaction of 2-bit events (usually, D2A, the most abundant) with an isolated SBU.

Each event has a name on it ("XAB", "XBE", etc) and a couple of numbers, pointing to the distances between bitflips 1&2 and 1&3 of the

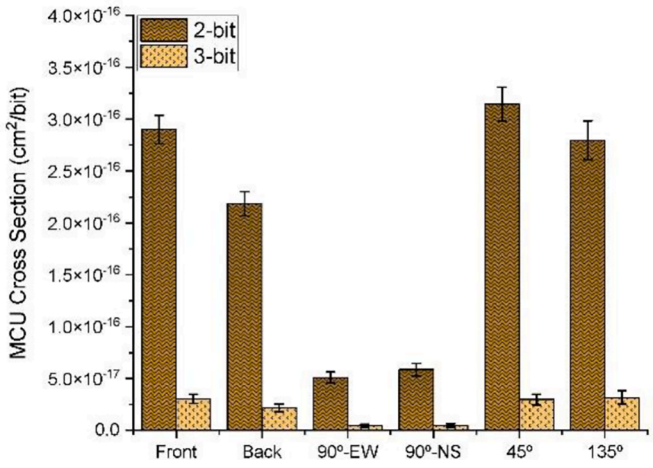

Fig. 5. 2- and 3-bit MCU cross-sections obtained at different incident angles in the CRAM.

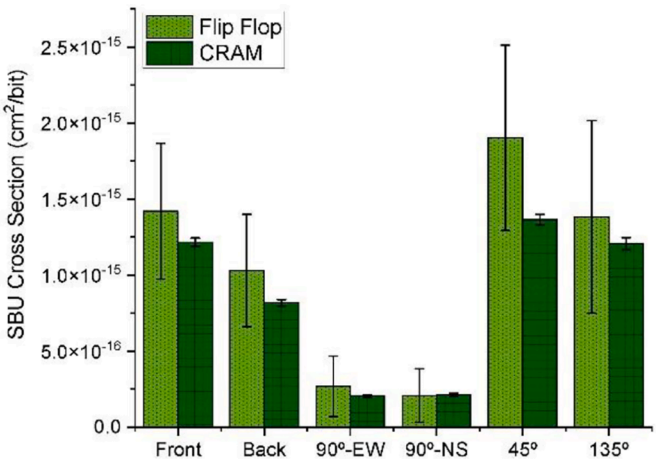

Fig. 6. SBU cross-sections obtained at different incident angles for FFs and CRAM.

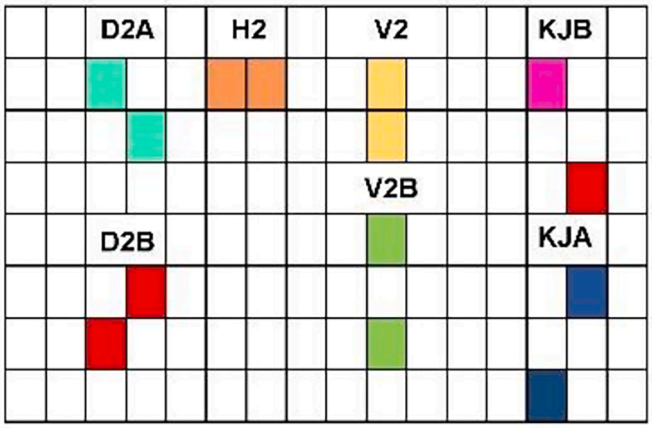

Fig. 7. Shape of the 2-bit MCUs.

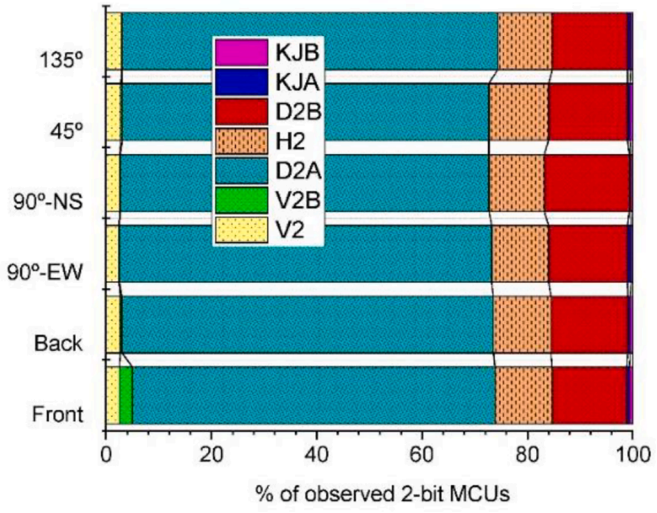

Fig. 8. Abundance and classification of the observed 2-bit MCUs according to their shapes.

3-bit MCU. Bitflip 1 of all types of 3-bit MCUs is marked in orange color in the figure to reach a better understanding. As explained in Section 00, distances in vertical increase by 1; and in horizontal by 3232 (as 101 ×

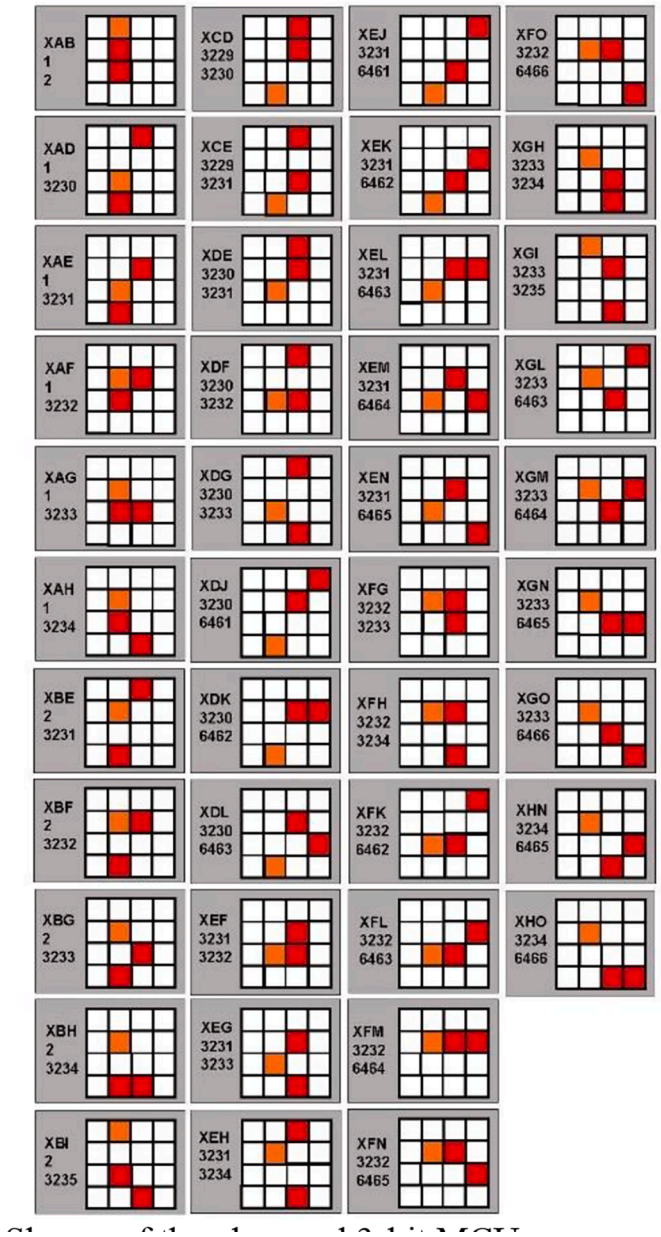

Fig. 9. Shapes of the observed 3-bit MCUs.

32), which corresponds to the structure of the CRAM in this FPGA. Fig. 10 depicts the percentages of seen events of each type. The most observed types of 3-bit MCUs are XAF and XEF, followed by XFG. Authors suppose the reading order of the CRAM can explain these differences about the actual physical position of the device concerning the neutron beam.

As reported in Table 3, MCUs of larger multiplicities were also observed. Fig. 11 displays the most observed shapes for each multiplicity, from 4-bit through 12-bit, For each multiplicity, shapes are displayed from more to less often, from left to right, and they are named XIA, XIB, and XIC. In general, it can be observed that these multiple events are mostly organized in columns, which, again, is consistent with the addressing mode of the Artix-7 FPGA. The abundance of such events depending on their shapes is depicted in Fig. 12.

In addition, Fig. 11 illustrates the shapes of the events with multiplicities 128 and 384. As indicated in the figure, all these events exhibited a horizontal shape, which points to the existence of some sort of SEFI. It is unexpected to observe horizontal events once most of the shapes in different multiplicities occur vertically.

4.4. Comparison between thermal and 14.2-MeV neutrons

This part makes a comparison between the radiation effects observed on the same Xilinx Artix-7 FPGA under thermal neutrons and under 14.2-MeV neutrons, the latter obtained in two radiation-ground campaigns carried out in 2017 and 2018 by the authors [18] at the GENEPI2 facility, hosted by the LPSC-CNRS laboratory [30]. Only normal incidence and front direction of the neutron beam were considered in this comparison.

Fig. 13 compares the cross-sections for 14.2-MeV and thermal neutrons according to the multiplicity of the events. It can be noted that thermal neutrons yielded MCUs with higher multiplicities than fast 14.2-MeV ones. On the other hand, it is recognized that higher cross-sections belong to fast neutrons. Although, it is observed that in the multiplicities of greater than four, the cross-section values are the same for both irradiation sources.

Comparative results show a considerable difference in FF cross-sections for both irradiation sources. FF cross-sections were 2.12×10^{-13} (cm^2/bit) and 6.75×10^{-15} (cm^2/bit), for thermal neutrons and 14.2-MeV ones, respectively.

4.5. MUSCA SEP3 predictions

As mentioned earlier, thermal neutron-induced SEU has been reported since the 1980s for devices containing ^{10}B in borophosphosilicate glass (BPSG) layers. Foundries left the BPSG from the 180-nm technological node and below; nevertheless, thermal neutron-induced SEU has continued to be reported for modern technologies. Boron doping in p-type silicon, using Diborane (B_2H_6) and boron trifluoride (BFl_3) in interconnect processing has been recognized as another source of ^{10}B contributing to thermal neutron-induced SEEs. The ^{10}B can increase SEE susceptibility because it has an unusually high nuclear cross-section of 3845 barns (where 1 barn = 10^{-24} cm^2 for thermal neutrons, while thermal neutron cross-sections with ^{11}B and Si are 5.3 and 2.2 barns, respectively. The isotopic abundance of natural boron is 20% ^{10}B and 80% ^{11}B. The risk of introducing ^{10}B is the high cross-section for ^{10}B thermal neutron capture and subsequent production of energetic charged particles that can cause SEEs. The ^{10}B cross-section for thermal neutrons is dominated by the (n,α) reaction inducing emission of an alpha particle and a Lithium-ion with energies of 1.47 MeV and 0.84 MeV, respectively. Moreover, the emission angle of the secondary is the opposite.

Simulations of the impact of a thermal neutron in the 28-nm bulk technology were performed using MUSCA SEP3 [31]. The platform is a Monte Carlo prediction tool that can simulate the radiation effects of protons, neutrons, muons, and heavy-ions on bulk CMOS, SOI, and Fin-FET technologies. In the framework of these investigations, the (n_{th}, α) nuclear reaction was introduced in the physic list, with the main consequence being the production of an alpha particle and Li-ion, whose energetic and angular properties have been described previously. Thus, ^{10}B is considered in three regions characterized by realistic concentration. Firstly, p-type sources and drains contain a boron concentration of 10^{20} cm^{-3} (whose 20% of ^{10}B). Secondly, the wells are characterized by a boron concentration of 10^{19} cm^{-3} and the tungsten plug (defined as a layer) by a concentration of 10^{16} cm^{-3}. A 12 × 12 SRAM array was considered for each simulation, and incident neutrons were uniformly distributed across the surface and the direction considered. The elementary SRAM cell surface is equal to 0.135 μm^2 (i.e. 0.57 μm × 0.24 μm). SBU and MCU-type event analyses can be extracted from simulations.

The first analysis concerns the relative contributions of ^{10}B in p-type sources and drains, p-wells, and tungsten plugs. Results show that the main contribution of thermal neutron-induced SEU results from boron present in p-type sources and drains. Moreover, alpha particles and Li-

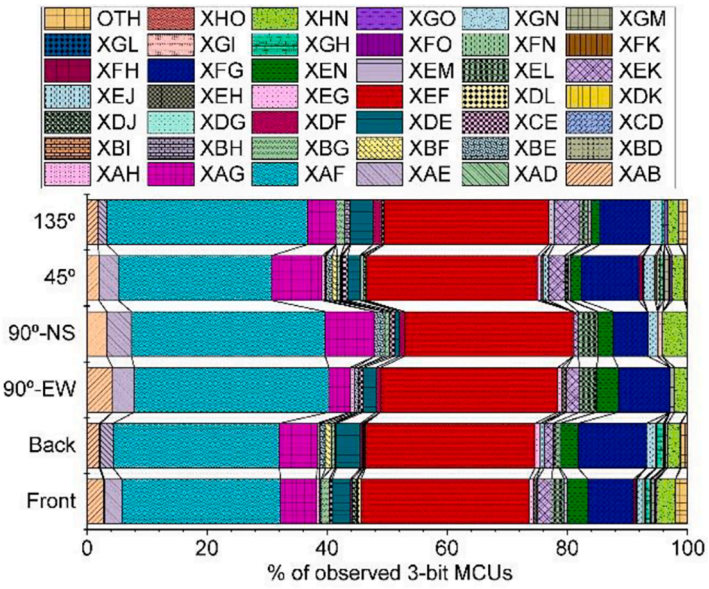

Fig. 10. Abundance and classification of the observed 3-bit MCUs according to their shapes.

Table 3
Different multiplicities in MCUs extracted by using the statistical method presented in [25], [26].

	Directions					
Size	Front	Back	45°	135°	90°-EW	90°-NS
2	✓	✓	✓	✓	✓	✓
3	✓	✓	✓	✓	✓	✓
4	✓	✓	✓	✓	✓	✓
5	✓	✓	✓	✓	✓	✓
6	✓	✓	✓	✓	✓	✓
7	✓	✓	✓	✓	✓	✓
8	✓	✓	✓	✓	✓	✓
9	✓	✓	✓	✓	✓	×
10	✓	✓	✓	✓	✓	×
11	✓	✓	✓	×	✓	✓
12	✓	✓	✓	×	×	×
128	✓	✓	✓	✓	✓	✓
384	×	×	✓	×	×	×

ions contribute to SEU occurrence.

Fig. 14 presents the 2 and 3-bit MCU cross-sections of the front, 90°, and 45° incident angles in the CRAM. Results cannot be compared quantitatively with the experimental results because the SRAM cell description and the critical charge are based on assumptions. Nevertheless, trends are very close to experimental results. The highest MCU

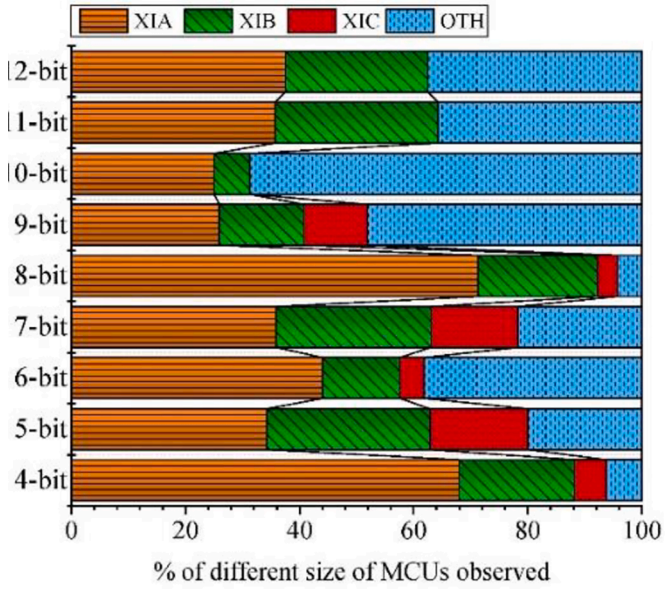

Fig. 12. Abundance and classification of the observed MCUs in different multiplicities.

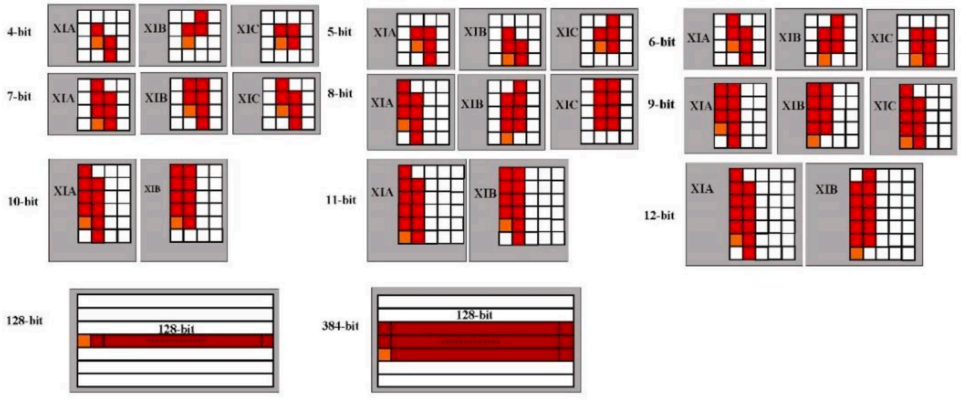

Fig. 11. Shapes of 4-bit to 12-bit, 128-bit and 384-bit MCUs.

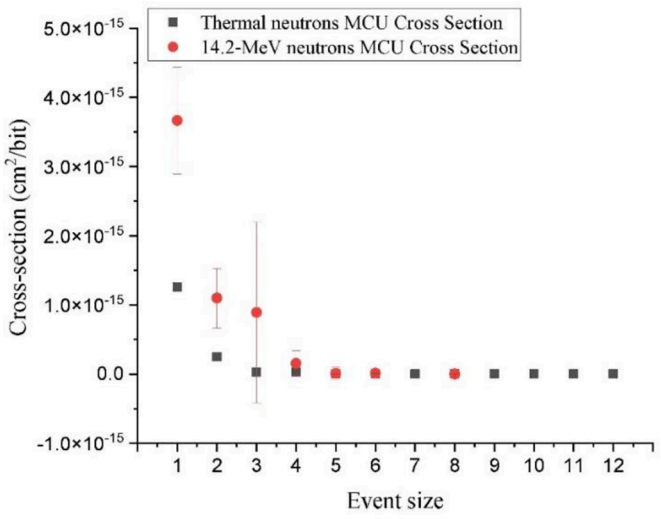

Fig. 13. Comparison of cross-sections of thermal neutrons and fast neutrons according to the multiplicity of the event.

sensitivity was obtained at 45° and the front direction, while the lowest was for grazing angles. The detailed analysis indicates two parameters that influence the occurrence level according to the direction; the ratio between the surface of drains/sources and the depth of dopant implantation and the distance travelled by the thermal neutron.

These results are very different from those observed experimentally, and by simulation, for 14-MeV neutrons [29]. Indeed, a lower sensitivity in 14-MeV neutron tests was obtained for the front of the device than the grazing condition, while an opposite behavior is observed with thermal neutrons. Concerning 14-MeV neutrons, physical analyses have shown that secondary ions are mainly emitted in the direction of the neutron incidence angle. In the case of front incidence, the MCU occurrence is due to the proximity of the carrier deposition on adjacent cells and/ or the carrier diffusion mechanism. In the case of lateral incidence, the particle's path may impact a larger number of cells, which strongly depends on the coupled secondary ion range and carrier density.

In the specific case of thermal neutrons, secondary ions (alpha and lithium) are isotopically emitted with an inverse angle between both particles; these properties do not favor either configuration. The ratio between drain/source surfaces and the dopant implantation depth has a higher influence on MCU occurrence. The global probability that a thermal neutron interacts with a ^{10}B atom is more important in the case of the front direction than the grazing direction.

4. Conclusion

This work has presented an experimental study of the radiation effects of thermal neutrons at different incident angles on a 28-nm bulk COTS SRAM-based FPGA. SBUs and multiple events (MBUs and MCUs) on CRAM cells, FFs, and BRAMs under diverse directions have been discussed. The study has revealed angular dependencies with the occurrence of SBUs and MCUs that were extracted from the experimental results. These dependencies are consistent for all types of events (MCUs and MBUs), but they differ from the trends that were observed in a previous work where the same device was exposed to 14.2-MeV neutrons [10]. Thus, in general, thermal neutrons provoke events more easily than 14.2-MeV ones, but the angular effects of these particles differ mainly due to the fact that thermal neutrons do not provoke as many multiple events as fast ones at grazing angles. Comparing the results of thermal neutrons and fast neutrons, it is observed that fast neutrons had a higher sensitivity to thermal neurons in multiplicities of 1 to 4. In events greater than 3, more various sizes happened in thermal ones.

Shapes of observed multiple events, including large-scale (128-bit and 384-bit) ones, were also discussed, revealing that they are more prone to affect cells in the same column. This is consistent with the addressing organization of the target Artix-7 FPGA, whose 32-bit words are organized in columns. Finally, a modelling tool called MUSCA-SEP3 was used to predict the device's sensitivity. The obtained experimental results matched with predicted ones in a very accurate way.

Availability of data and materials

The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

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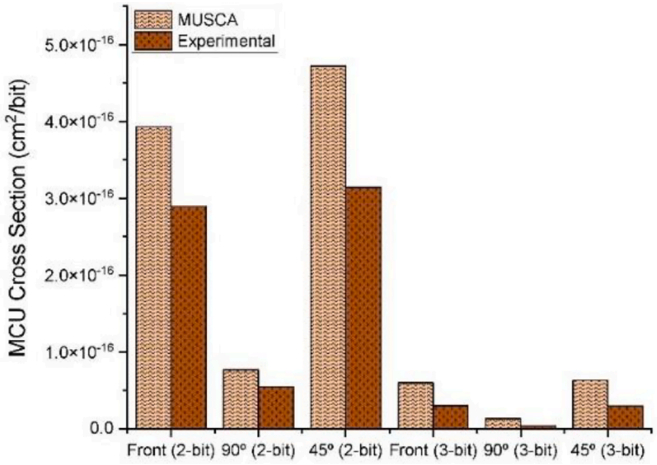

Fig. 14. Comparison of 2 and 3-bit MCU cross-sections issued from MUSCA SEP3 vs. experimental results for different incidence angles.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix A

Typically, cross-sections (σ) are calculated as follows:

$$\sigma = \frac{\text{N° of observed events}}{\text{Particle flux . Time . Memory size (bits)}} \tag{1}$$

Where "Particle flux" is the amount of particles per time unit that the device receives per cm^2 and "Time'" is the exposure time of the device against the radiation beam. The higher this value is, the higher the SER of the device is, since said SER is defined as follows:

$$SER = \frac{\text{N° of observed events}}{\text{Time}} \tag{2}$$

Thus, replacing the following term:

$$\frac{\text{N° of observed events}}{\text{Time}} = \sigma \text{ . Particle flux . Memory size}$$

from (1) in (2) we get:

$$\text{SER} = \sigma \text{ . Particle flux . Memory size (bits)} \tag{3}$$

which clearly indicates that the SER is directly proportional to σ.

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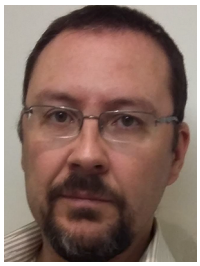

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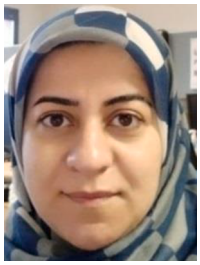

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