Neutron-Induced Upsets and Stuck Bits on COTS Pseudo-Static RAMs

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***Abstract*—This paper presents an experimental study on the SEE radiation effects of several pseudo-static RAMs (PSRAMs) under 14-MeV neutrons. SEFIs and stuck-at faults were observed while performing static and dynamic tests.**

***Index Terms*—COTS, PSRAM, radiation hardness, reliability, soft error.**

I. Introduction and Related Work

Commercial-Off-The-Shelf (COTS) Pseudo-Static RAMs (PSRAMs) combine the benefits of DRAMs' high density with SRAMs' ease of use, making them suitable for low-power and spatial applications. Hence, it is interesting to understand the radiation effects on these kind of devices.

Previous studies in the literature have reported Total Ionizing Dose (TID) effects on PSRAMs, such as a 52.5 TID threshold for bitflips [1], and a voltage drop due to a transistor leakage of 14.9% after a TID of 100 krad [2], both on the IS66WV25616BLL device (manufactured by ISSI).

Other studies have pointed out radiation effects under different types of particles on various types of dynamic RAMs. Thus, Söderström et al. studied 6-to-200 MeV electron-induced SEEs [3] and 50-230 MeV proton-induced SBUs and stuck faults [4] on several 63-nm, 72-nm and 110-nm Synchronous DRAMs (SDRAMs), manufactured by ISSI. Matana et al. observed SBUs, stuck-at bits and SEFIs on a self-refresh DRAM (commertially known as HyperRAM), manufactured by Infineon, under thermal+atmospheric neutrons and 70-230 MeV protons [5], [6]. Stuck bits have also been observed on DDR3 memories with 45-MeV protons [7]. Finally, the leakage current attributed to radiation-induced stuck-at errors in DRAM cells has been quantified and modeled [8], and the retention time and degradation of functionality under proton irradiation on SDRAMs have also been studied [9]. However, none of these papers discussed radiation-induced single events in PSRAMs.

This paper studies the SEE sensitivity of 3 PSRAMs to 14-MeV neutrons. The devices were tested in both dynamic and static modes to achieve a better understanding. SEFIs, stuck-at faults, and isolated SBUs were observed in these devices and are discussed in the rest of the paper.

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This work was supported in part by the Spanish MINECO project PID2020-112916GB-I00, "RESHYLIENCE". The work at the FNG was funded by the European Union's 2020 research and innovation program under grant agreement No 101008126, corresponding to the RADNEXT project.

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TABLE I
Tested memories

Device	Size (Mb)	Manufacturer	Referred as
APS1604L-3SQR	16	AP Memory	AP (a)
APS6404L-SQRH	64	AP Memory	AP (b)
IS66WVS4M8ALL	32	ISSI Inc.	ISSI

II. Experimental Setup

Three COTS PSRAMs, namely APS6404L-SQRH (64Mb) and APS1604L-3SQR (16Mb) (manufactured by AP Memory Technology) and the IS66WVS4M8ALL (32Mb, manufactured by ISSI Inc.) were used as Devices Under Test (DUTs). These memories use both SPI and Quad SPI (QPI) communication protocols, and during the tests, they operated at nominal voltage, room temperature, and the incidence angle of neutrons was normal with respect to the surface of the device.

Table I shows a brief summary of these DUTs. These were controlled by a microcontroller board based on the Atmel SAM3X8E ARM Cortex-M3 CPU running at up to 84 MHz. The microcontroller was connected to a computer system via a USB cable, which supplied power and enabled data storage. This computer system, located in a separate room, was used to control and monitor the experiment. All equipment in the radiation room, except the DUT itself, was shielded against radiation.

The test campaign was conducted in February 2024 at FNG (Frascati Neutron Generator, Italy) [10], where the samples were exposed to a constant flux of $2{\cdot}10^7$ 14-MeV n/cm^2/s produced from typical D-T reactions. The access to the FNG facilities was funded by the RADNEXT project [11]. Regarding potential displacement damage, the equivalence factor for 14-MeV neutrons is 1.79 1-MeV n/cm^2 [12].

The information to map the logical addresses to the physical position of each memory cell was not available to the authors. However, a tool called LELAPE that has recently been developed by the authors [13] was used to categorize the different types of events from the raw data. This tool performs a statistical analysis of all the possible "distances" between the events that were observed and classifies bitflips into the same event if the "distance" between them appeared more often than expected in a theoretical only-SBU scenario. The statistical foundations of this method are described in detail in previous works [14], [15].

III. Experimental Results and Discussion

A. Static Tests: Description and results

At first, the memories were tested in static mode to find a threshold flux for the radiation setup. The setup was tested using a data pattern of `0x55` gradually increasing the flux. None of the DUTs showed SEEs up to $2 \cdot 10^7$ n/cm^2/s of flux and a total fluence of $5 \cdot 10^{10}$ n/cm^2.

These results allow us to establish threshold levels for the cross-sections of the different devices. Using the procedure proposed by ESA [16], the upper threshold levels for the cross sections are as follows:

$$\sigma_{\mathrm{S,DEV}} \leq \frac{3.69}{5 \cdot 10^{10}} = 7.4 \cdot 10^{-11}\ \mathrm{cm}^2/\mathrm{device}$$

and

$$\sigma_{\mathrm{AP(a)}} \leq 4.4 \cdot 10^{-18}\ \mathrm{cm}^2/\mathrm{bit}$$

$$\sigma_{\mathrm{AP(b)}} \leq 1.1 \cdot 10^{-18}\ \mathrm{cm}^2/\mathrm{bit}$$

$$\sigma_{\mathrm{ISSI}} \leq 2.2 \cdot 10^{-18}\ \mathrm{cm}^2/\mathrm{bit}$$

It is nonsense to determine whether there is a dependence on the pattern associated with the Alpen effect [17].

Another important observation is that, despite working in static mode, the PSRAMs run internally since they continuously refresh their contents. Thus, since no errors were observed in these static tests, the authors suggest that the radiation-induced events observed in the dynamic tests (described in the following sections) are not related to this characteristic of the DUTs.

B. Dynamic Tests: Description

Dynamic tests are a type of test that involves irradiating a device as it works on a specific task. For a PSRAM, these tasks can consist of reading, writing, or a simple/complex combination of both. There are several dynamic test algorithms, and using each one of them might have a different impact on the device's cross-section. Two of the well-known dynamic test algorithms are called March-C [18] and March Dynamic Stress (DS) [19].

A specific type of notation is used to describe these algorithms. The symbol $\uparrow$ in this notation indicates that the addresses are accessed in increasing order. The $\downarrow$ address order must be the reverse order of $\uparrow$. If the order of the addresses can be chosen arbitrarily, then the symbol $\updownarrow$ is used. A complete test cycle is shown in the "{...}" bracket pair; while an element is shown in the "(...)" bracket pair. Each element can include a mix of read/write operations which are applied to a cell. These operations are 'w0', 'w1', 'r0', and 'r1'. The 'w' indicates a write operation, and the 'r' stands for a read operation. The following numbers after 'w' or 'r' show the expected value for the bit in that operation.

1) March-C Algorithm: In this type of dynamic test, there are six elements of single or double operations. Each element and its operations are applied to all SRAM addresses and then the algorithm progresses to the next cycle [18]. The scheme of the March-C algorithm is as follows:

$$\begin{aligned}\{ &\updownarrow (w0); \uparrow (r0, w1); \uparrow (r1, w0); \\ &\downarrow (r0, w1); \downarrow (r1, w0); \updownarrow (r0); \}\end{aligned} \tag{1}$$

2) March Dynamic Stress (DS) Algorithm: The main purpose of this algorithm is to put pressure on the read/write lines. Unlike the previous algorithm, the March DS does not transient from one bit to another [19]. However, it focuses on doing the same operation several times. The scheme of the March DS algorithm is as follows:

$$\begin{aligned}\{ &\uparrow (r0, w1, r1, r1, r1, r1, r1); \\ &\uparrow (r1, w0, r0, r0, r0, r0, r0); \\ &\uparrow (r0, w1, r1, r1, r1, r1, r1); \\ &\uparrow (r1, w0, r0, r0, r0, r0, r0); \\ &\downarrow (r0, w1, r1, r1, r1, r1, r1); \\ &\downarrow (r1, w0, r0, r0, r0, r0, r0); \}\end{aligned} \tag{2}$$

Considering that the DUTs are irradiated during every stage of the dynamic algorithms, it is possible to miss some bitflips in the final step. Hence, after each complete run of the algorithms, the devices were read one more round to check for these possible bitflips.

C. Dynamic Tests: Raw Results

The dynamic tests were continued at the maximum flux available in the FNG facility of $2{\cdot}10^7$ n/cm^2/s.

Each DUT was tested with the March-C and DS algorithms at various speeds. The raw data extracted from these tests are presented in Table II. It is worth mentioning that 4 groups of errors were distinguished during the tests:

- **Single Bit Upsets (SBUs)**: An isolated bit in a cell is flipped 0→1 or 1→0.
- **Stuck-At Faults (SAFs)**: Individual bitflips that did not disappear even after rewriting the DUT. The content of these cell were Stuck-At 0 (SA0) or 1 (SA1).
- **Single Event Functional Interrupts (SEFIs)**: Large number of consecutive addresses, after which the DUT remained functional.
- **System hangs**: Large number of consecutive addresses, but this time the DUT hung, so a hard reset was necessary to continue working with it.

Whenever the device hung, the data obtained so far were unusable and the experiment had to be repeated. Therefore, such hangs avoided to get results for some experiments, such as March-C at 3 and 6 MHz on the AP (a) device. This is marked with a "×" symbol in Table II. Anytime such hangs occurred, the involved memory was changed for safety measures.

At first glance, it is noticeable that during the March-C experiments on the AP devices, several hangs halted the

TABLE II
RUN SEQUENCE OF THE IRRADIATION CAMPAIGN FOR THE DUTS

Device	Algorithm	Speed (MHz)	Total fluence (n/cm^2) $\times 10^{11}$	Number of observed bitflips
AP (a)	March-C	3	10	×
		4	10	827
		6	10	×
		12	10	33
	March DS	4	19.1	6
AP (b)	March-C	3	1.15	×
		4	7.63	×
		4	1.09	235
		6	1.14	×
		12	1.11	6
	March DS	12	22.7	16539
		12	20.2	5585
ISSI	March-C	3	1.33	320
		4	1.33	303
		6	1.31	367
		12	1.08	357
	March DS	12	18	×

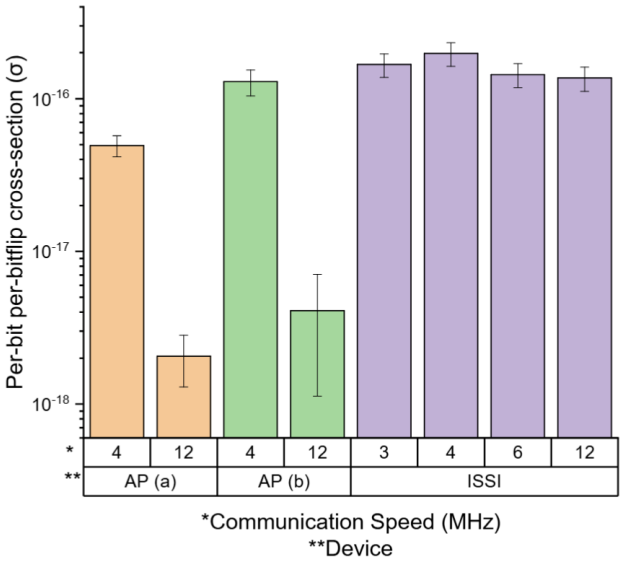

Fig. 1. Per-bit per-bitflip cross-sections of the tested devices while running the March-C algorithm at various speeds

algorithm. Comparing this with the ISSI device shows that the AP memories are more prone to this type of event. However, the ISSI device hung many times when running the March DS algorithm and it was not possible to record any bitflip during that experiment (i.e., the last row of Table II).

Using the data presented in Table II for the March-C algorithm, the sensitivity of the DUTs to 14-MeV neutrons was calculated as well. Fig. 1 shows the per-bit per-bitflip cross-section (in cm^2/bit) of the PSRAMs against radiation at various speeds, which was calculated as follows:

$$\sigma = \frac{N_{\text{bitflips}}}{\Phi \cdot N_{\text{bits}}} \tag{3}$$

Where N_{bitflips} is the number of bitflips that were observed in the experiment, Φ is the particle fluence (in n/cm^2) and N_{bits} is the DUT capacity in terms of bits.

TABLE III
CATEGORIZATION OF THE EVENTS OBSERVED FOR THE MARCH-C DYNAMIC ALGORITHM

Device	Number of observed bitflips	Speed (MHz)	SEFIs	SAFs		SBUs
				SA0	SA1	
AP (a)	827	4	1	1	0	8
	33	12	1	1	3	1
AP (b)	235	4	30	0	0	9
	6	12	0	0	0	6
ISSI	320	3	39	0	0	9
	303	4	35	0	0	22
	367	6	45	0	0	9
	357	12	44	0	0	8

The graphs incorporate error bars accounting for uncertainties in the beam profile (±10%), fluence accuracy (± 10%), and the 95% confidence intervals as described in [16].

Figure 1 shows a significant decrease in the cross-section for the AP memories at a higher speed (4 MHz vs. 12 MHz). For the ISSI device, no significant dependency between cross-section and communication speed can be observed. However, this figure represents the raw data on the sum of the observed bitflips after executing the March-C algorithm, which includes multiple write/read cycles. To gain a detailed understanding of the results, the output of each read cycle of the algorithm was analyzed separately.

D. Dynamic Tests: March-C, Categorization of events

A detailed categorization of the raw data with LELAPE revealed more information about the results. For this purpose, the data from each read cycle were analyzed individually.

Table III shows the detailed number of events that occurred during the March-C test and were reported in Table II. For the AP (a) device, most of the bitflips observed and presented in Table II belong to the same event. Thus, at 4 MHz, 102 consecutive addresses from `0x15C600` to `0x15C665` (both included) lost their data completely, hence they were classified as SEFIs in Table III. The authors had previously observed a similar phenomenon in other parallel SRAMs under 14-MeV neutrons and 15-MeV protons [20]–[22]. The occurrence of a micro-latchup, which results in a significant delay of control signals (such as word line selection) at the vertical edge of a memory array—distant from the address decoder—can account for this phenomenon. The presence of current limiters and separate power lines in these areas might explain these disruptions.

SAFs were also observed in this device more often compared to the other two: several SA0s and SA1s were identified when working at 4 and 12 MHz of frequency. Due to the change of the written pattern in the March-C algorithm (all 0's and all 1's, alternatively), SA0s and SA1s appeared repeatedly in odd or even cycles, respectively.

Table III also shows detailed event numbers for the AP (b) and ISSI devices. It can be observed that these behaved differently from the AP (a) one.

Thus, firstly, it can be seen that the number of detected SEFIs is higher for these (30-45 SEFIs per round). However,

TABLE IV
DETAIL OF THE LARGE EVENTS OBSERVED DURING THE TWO MARCH DS TESTS CARRIED OUT ON AP (B) DEVICE

Number of affected addresses	Start address	Final address	Expected data	Observed data
2048	0xAA000	0xAA7FF	0xFF	Random
2048	0x152000	0x1547FF	0xFF	Random
899	0x1B4400	0x1B4782	0xFF	0x00
2048	0x1FE000	0x1FE7FF	0xFF	Random
314	0xC2AC6	0xC2BFF	0x00	0xFF
2048	0xAC000	0xAC7FF	0xFF	Random
2048	0x1AA7FF	0x1AA000	0x00	0xFF
1024	0x141000	0x1413FF	0x00	Random
2049	0x1FF800	0x1FFFFF	0x00	0xFF
2049	0x1EC800	0x1ECBFF	0x00	Random

the multiplicity of these events was significantly smaller: Each of them corrupted the data only on one address (i.e., one byte). However, every bit of these bytes was flipped, which means converting 0x00 to 0xFF and vice-versa. It is important to mention that the single SEFI presented at 12 MHz on Table III for the AP (a) memory was also similar to this type.

On the other hand, no SAFs were observed for these two devices with the March-C algorithm. Finally, scarce SBUs were observed in all devices regardless of the communication speed. Even if the results vary at different speeds, this time no significant dependence between SEE sensitivity and communication speed could be found. This is mainly due to the overwhelming effect of SEFIs.

E. Dynamic Tests: March DS, categorization of events

Due to the frequent hangs occurred during the DS tests, not much could be concluded from these tests. For the AP (a) device, in total 6 individual bitflips were observed (Table II). For AP (b), the two experiments shown in Table II yielded a large number of errors (16539 and 5585 bitflips each). Table IV shows the details of the SEFIs observed during these two experiments.

As can be seen in Table IV, most of these events affected ∼2048 consecutive addresses. Events where the data observed were random can be categorized as SEFIs, whereas those where the data changed from 0xFF to 0x00 can be seen as massive SA0s (or SA1s if the data changed from 0x00 to 0xFF). The latter two have not been observed in previous studies carried out by the authors. Since the effect of these large events overshadows the other smaller events (e.g. isolated SAFs and SBUs), the authors recommend more experiments with this algorithm at various speeds for PSRAMs which have proved to be very sensitive to stuck-at faults and SEFIs.

IV. CONCLUSIONS

This paper has presented an experimental study of the SEE sensitivity of APS6404L-SQRH, APS6404L-SQRH (from AP Memory) and IS66WVS4M8ALL (from ISSI Inc.) PSRAMs to 14-MeV neutrons. Both static and dynamic March-C and Dynamic Stress (DS) tests were conducted at the FNG research center, demonstrating that these devices are susceptible to various types of events, including SBUs, stuck-at faults and SEFIs. March-C tests revealed that the AP Memory devices were more prone to errors at lower SPI frequencies; however, March DS experiments were less conclusive.

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