Impact of the Bitcell Topology on the Multiple Cell Upsets Observed in VLSI Nanoscale SRAMs

Juan A. Clemente, Guillaume Hubert, Mohammadreza Rezaei, Francisco J. Franco and Hortensia Mecha

***Abstract*—This paper presents an analysis of the multiple events (and more specifically, Multiple Cell Upsets or MCUs) that may occur at successive generations of bulk CMOS SRAMs operating under harsh conditions, such as in avionics or space. Such MCU distribution is greatly impacted by the bitcell topology, which, in the International Technology Roadmap for Semiconductors (ITRS) / International Roadmap for Devices and Systems (IRDS) history, experienced a drastic change in the transition between the 90-nm and the 65-nm nodes. Experimental results obtained from proton and neutron accelerators, along with predictions issued from the MUSCA-SEP3 modeling tool, are provided. Various COTS Static Random Access Memories (SRAMs) manufactured by Infineon in bulk CMOS 130-nm nodes down to the 65-nm one were used as targets for the experimental results. Finally, MUSCA-SEP3 was also used to analyze and discuss scaling trends on more modern nodes (45-nm down to 14-nm).**

***Index Terms*—Single Event Effects, Multiple Cell Upset, SRAM, IRDS roadmap.**

I. Introduction and Related Work

WHEN nanoscale devices, and particularly memories, are exposed to radiation, they might suffer from the effects of the so-called Single Event Effects (SEEs) [1]. This is especially of interest in environments such as avionics and space, where Commercial-Off-The-Shelf (COTS) devices have arisen as an interesting alternative to devices certified against radiation [2]. The reason is that, in spite of miniaturization, they implement techniques for error detection and correction [3].

Among these effects, Single Event Upsets (SEUs) are provoked by a single particle (such as protons, neutrons...) [4], [5] impacting the device and flipping the content of one or more memory cells. Thus, a Single Bit Upset (SBU) appears when the output logic state of only one cell is flipped, whereas Multiple Bit Upsets (MBUs) and Multiple Cell Upsets (MCUs) manifest when the state of several cells (belonging to the same memory word or not, respectively) are flipped instead. The latter classification is no more than a logical interpretation of a multiple event, in which a number of physically neighbouring cells are affected by the same particle. These are all soft errors, which do not permanently damage the memory cells. There is also a plethora of other types of destructive (and therefore, permanent) errors, such as Single-Event Lathups (SELs), Single Event Gate Ruptures (SEGRs), Single Event Burnouts (SEBs)... which are out of scope for this paper [6].

The constant miniaturization of Very Large Scale Integration (VLSI) devices has led to an increase in the probability of occurrence of MCUs. Indeed, the multiplicity of such events has also demonstrated to be higher in more miniaturized devices [7]. This is partly due to the reduction in the size of the transistors that compose the cells, which makes it easier for a particle to encounter several bitcells along its path. In 1994, Dodd et al. used mixed-mode device/circuit modeling to demonstrate that MCUs can result from charge collection in adjacent SRAM cells [8]. Nowadays the most widely considered mechanism for SRAM upset is the charge collection at an OFF transistor drain [9]. The mechanisms behind charge sharing between multiple close junctions have been described in other works in the literature [10], [11]. Benett et al. [12] state that such charge sharing depends on the amount of charge generated by the incident particle (heavy ions and laser) in the first micrometer of the active silicon. This is also true for protons as they are ionizing particles too [13], although other parameters such as the particle incident angle significantly affect the MCU/MBU occurrence and their multiplicity [14].

At certain points of the miniaturization roadmap, manufacturers have encountered a number of challenges to continue technology scaling in array designs for meeting both performance and density requirements for high performance [15]. These were solved thanks to a tight cooperation between process and design mitigation techniques. A well-known case study of a combined process-design mitigation strategy was to change the topology of the SRAM cell from a "tall" design to a "wide" one [16]. Thus, the "tall" cell was classically used until the 90-nm technological node, but the "wide" one was adopted to alleviate process difficulties [17], for the 65-nm technological node and subsequent ones [18] (see Fig. 1). The "wide" design improves critical dimension control and variation by aligning the polysilicon in a single direction, therefore eliminating diffusion corners and relaxing some patterning constraints on other critical layers. These changes are suspected to have a strong impact on the distribution of the multiple events that occur when a memory is exposed to radiation.

In a previous work [19], the authors examined several SRAMs with 130-nm, 90-nm and 65-nm bulk CMOS manufacturing processes under 14.2 MeV neutron radiation when dynamic voltage scaling (DVS) is applied for saving power.

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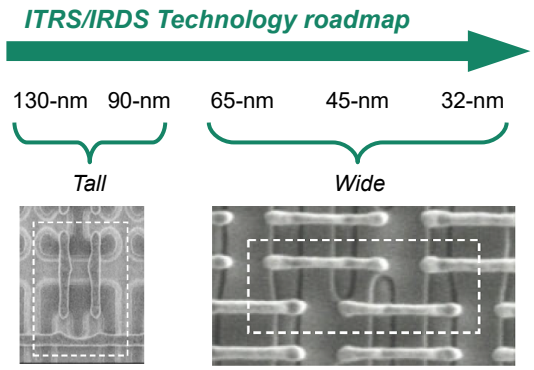

Fig. 1. Technology roadmap for several nodes, including the "tall" and "wide" bitcell designs.

In that work, a preliminary study of the 2-bit MCU shapes was done and, indeed, it was revealed a drastic change in the transition between the 90-nm and 65-nm nodes. This article further extends that analysis for more particles (protons and neutrons; heavy ions were excluded from this study for simplicity), more energies (from 10 MeV to 1 GeV), more nodes (down to 14-nm) and events of more multiplicity. For this purpose, the MUSCA-SEP3 modeling tool [20]–[22] will be used. It was developed at the ONERA research center (in Toulouse, France) for emulating the possible effects caused by the impact of an energetic particle (neutron, proton, heavy ion...) in the sensitive areas of a microelectronic device.

Results will reveal that MUSCA-SEP3 predicts well the drastic change observed experimentally between the 90-nm and 65-nm nodes. Then, this tool will be postulated for making predictions in other nodes for which experimental results are not available. Analyzing the MCU shapes can further point key issues for the design of an effective SEE mitigation approach.

The rest of the paper is organized as follows. First, Section II discusses the experimental results on the 130-nm, 90-nm and 65-nm nodes obtained with protons and neutrons, as well as the comparison with the MUSCA-SEP3 predictions. Then, Section III discusses the so-called "false multiple events" (as defined by the authors in previous works [23], [24]), which constituted a disagreement observed in Section II. Section IV presents scaling trends made with MUSCA-SEP3 simulations on more miniaturized nodes (65-nm down to 14-nm) and finally, Section V presents the conclusions.

II. Experimental vs. MUSCA-SEP3 predictions

A. Experimental setup

Table I shows the devices (3 COTS SRAMs manufactured by Infineon) [25]–[27], which were irradiated under 14.2-MeV neutrons and 14-MeV protons. Table II shows the experiments that were made.

The data regarding neutrons are those published in [19] when the devices operated at nominal V_{CC} (3.3 V). They were obtained in May 2015 and June 2017 at the GENEPI-2 facility, available at the Laboratoire de Physique Subatomique et Cosmologie (LPSC) in Grenoble, France [28], [29]. Additionally, new proton ones were carried out in May 2019 at the cyclotron existing at the Centro Nacional de Aceleradores (CNA) in Sevilla, Spain [30], [31]. Proton data on Device C were published in [32].

TABLE I
Devices that were examined experimentally

Device	Node	Part nº (Infineon)
A	130-nm	CY62167DV30LL-55ZXI [25]
B	90-nm	CY62167EV30LL-45ZXI [26]
C	65-nm	CY62167GE30-45ZXI [27]

TABLE II
Experiments that were carried out and events with different multiplicity. Neutron energy was 14.2 MeV and proton energy was 14 MeV

Device	Exp. Nº	Pattern	Fluence [a]	Events SBU	2-bit	3-bit	4-bit
A	1	0x55	1.79×10^{9} n/cm^2	439	34	3	0
	2	0x55	1.20×10^{10} p/cm^2	391	39	6	5
	3	0xAA	9.30×10^{10} p/cm^2	263	30	4	2
B	4	0x55	5.83×10^{8} n/cm^2	288	34	4	4
	5	0x55	1.10×10^{10} p/cm^2	335	56	7	1
	6	0xAA	1.00×10^{10} p/cm^2	269	28	6	1
C	7	0x55	2.79×10^{9} n/cm^2	1161	259	39	9
	8	0xAA	2.91×10^{9} n/cm^2	1088	200	35	5
	9	0x55	7.40×10^{9} p/cm^2	155	35	4	0
	10	0xAA	1.60×10^{10} p/cm^2	212	45	4	0

[a] p = protons; n = neutrons

In both cases, static tests were performed: the SRAM under test was firstly initialized to a known pattern (0x55 or 0xAA), then the beam was activated for a few minutes, and finally the SRAM was read back and existence of errors was checked. Table II shows the events observed, where those with different multiplicities (from SBUs to 4-bit MCUs) were extracted by using proprietary information of the manufacturer. Bitflips located at a Manhattan Distance (MD) lower or equal to 3 were grouped into the same MCU.

B. MUSCA-SEP3

MUSCA SEP3 is based on sequentially modelling all physical mechanisms involved in the SEE occurrence, from the system down to the semiconductor target. It allows calculating SEE cross sections for a given device, or analyzing the nature of the events triggered by the particles emulated with the tool.

MUSCA-SEP3 takes as input a low-level description of the bitcells' floorplan, with a size (X×Y) that is specified by the user. It includes the topology of the transistors' drains/sources extracted from the cell layout, and as well as a description of the passivation and metallization layers, which can also be simplified to assumptions deduced from the technological roadmap if no specific information is available (such as the thickness and specific materials, for instance). Then, the objective is to model a situation close to the irradiation by emulating the impact of particles on the target device by means of Monte-Carlo simulations. In each simulation, a particle is

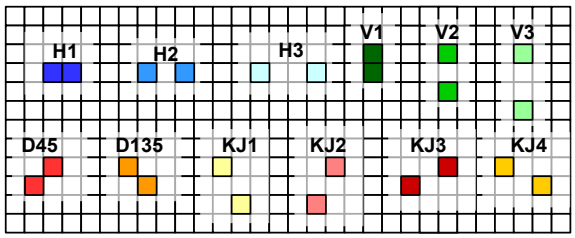

Fig. 2. Classification of the 2-bit MCUs that can be observed with Manhattan Distance (MD) ≤ 3, according to their shapes.

selected according to the input energy spectrum and angular properties. In this case, this is reduced to a normal incidence, although MUSCA-SEP3 is also capable of studying angular effects of incident particles, as demonstrated in another recent research [33]. Then, the starting point of the particle is selected as the central cell of the 11×11 grid of memory cells. This emulates the impact of a particle in a small memory, and makes it possible to analyze the SEEs occurring not only in the target cell, but also in the neighbouring ones.

Then, the particle is transported within the device and the primary or secondary ion energy loss along the path is simulated by using the stopping powers pre-calculated with the SRIM code [34]. The simulation of nuclear reactions induced by primary protons or neutrons is performed by inputting pre-calculated nuclear reactions for various incident energies and materials. Subsequently, primary and secondary ions are responsible for the production of electron-hole pairs in the device. The next step is to simulate the transport and the collection mechanisms inducing charge levels in each drain/source. The impact of the particle can be deduced by associating collected charges with some criteria (for instance, a given level of threshold critical charge). Finally, the cells that trapped enough charge to trigger a SEE are identified and the shape of the events can be analyzed. In this study, we have considered a double criterion to stop each simulation: either to obtain 10^3 events or to draw 10^5 nuclear events.

C. Studying the shape of experimental 2-bit MCUs

First, the topology of the experimental 2-bit MCUs was studied. Fig. 2 shows the 12 possible types of such events that can occur (horizontal (H1-H3), vertical (V1-V3), diagonal (D45, D135) and chess "Knight Jump" distributions (KJ1-KJ4)). A horizontal line was considered as the direction in which bits of the same word are distributed. The manufacturer calls them "rows".

Events of such distributions were extracted from the experiments and their relative abundances are depicted in Fig. 3. Experiments regarding neutrons and protons are displayed in Figs. 3(a) and 3(b), respectively. Each displayed experimental piece of data has been the result of averaging the data of Table II regarding the two possible *checkerboard* patterns (0x55 and 0xAA) concerning the same device. For each one of these, MUSCA-SEP3 predictions are also provided in the figure for the sake of comparison.

In both subfigures, it can be clearly observed the impact of the drastic change in the bitcell topology occurred between

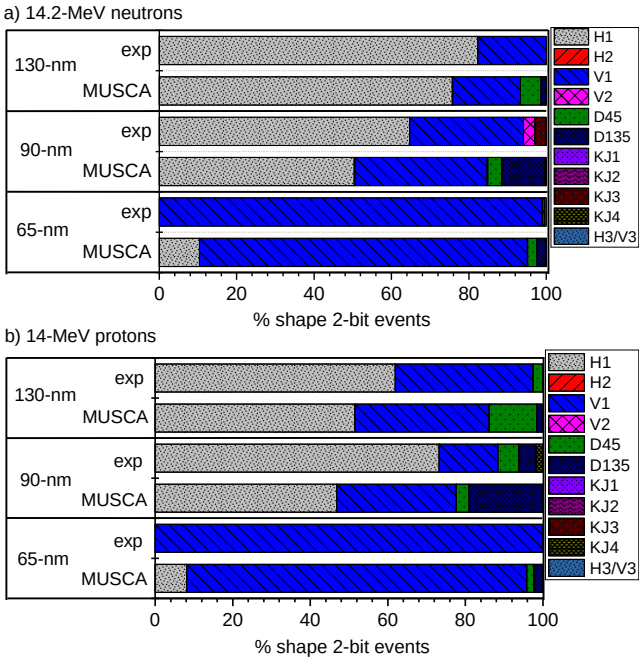

Fig. 3. Classification of 2-bit MCUs according to their shape. MUSCA-SEP3 predictions vs. experimental data concerning a) 14.2-MeV neutrons and b) 14-MeV protons.

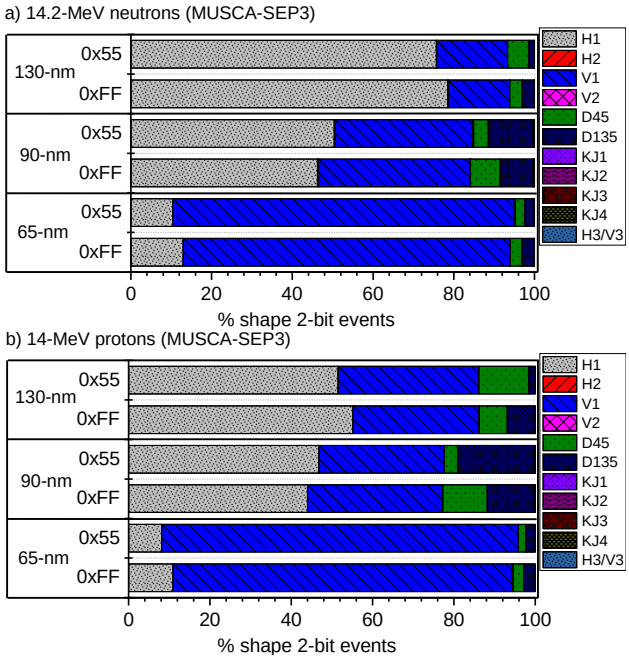

Fig. 4. Classification of 2-bit MCUs according to their shape. MUSCA-SEP3 predictions for different patterns (0x55 and 0xFF) and nodes, concerning a) 14.2-MeV neutrons and b) 14-MeV protons.

the 90-nm and the 65-nm nodes. Thus, whereas the horizontal "H1" type is dominant in the 130-nm and 90-nm nodes (with percentages that range from 62% to 82%), the vertical "V1" distribution is almost the only existing one for the 65-nm node ($\sim$98% for neutrons and 100% for protons). H1 and V1 are the most abundant 2-bit MCU shapes, followed by the diagonal ones (which are more abundant in the 90-nm node). Other

TABLE III
NUMBER OF EVENTS OF TYPE KJ1-KJ4, H2, H3, V2 AND V3 OBSERVED IN EXPERIMENTS 1-10 PRESENTED IN TABLE II

Exp. Nº	Total bitflips (N_{BF})	KJ1-KJ4	H2+V2	H3+V3
1	516	0	0	0
2	507	0	0	0
3	343	0	0	0
4	384	1	1	0
5	472	0	0	0
6	347	1	0	0
7	1850	0	3	1
8	1631	0	1	1
9	237	0	0	0
10	314	0	0	0

types of events (H2, V2 and KJ1-KJ4) are extremely rare, but surprisingly not predicted with the MUSCA-SEP3 model. Next section makes a deeper discussion of these undetected types of events by MUSCA-SEP3.

In all the cases, this simulation tool demonstrates to be a quite accurate model, since predictions match well the experimental data. Reverse engineering was performed on the 90-nm SRAM [35], allowing to access to the cell topology. Results confirm the use of a "tall" design, in contrast to the "wide" one. Note that this study cannot be extrapolated to heavy ions as primary impinging particles, even though the secondary heavy ion productions are emulated by MUSCA-SEP3 when nuclear interactions occur in the simulations.

In both cases (experimentally and simulations), a comparison between proton and neutron irradiation shows a slightly higher probability of protons to cause vertical events. The experimental case of the 90-nm SRAM (protons) seems to be an outlier since it does not match the MUSCA-SEP3 predictions, but it can be attributed to the number of double events being scarce (less than 100, see Table II). Finally, Fig. 4 breaks down the predictions for the two different patterns (0x55 vs. 0xFF). The pattern does not seem to have any significant impact in the event distribution either.

III. DISCUSSION OF FALSE MULTIPLE EVENTS

Fig. 3 showed that, in the experiments, the vast majority of the observed events were bitflips separated by a Manhattan distance not greater than 1, disposed of horizontal, vertical or diagonal distribution. Other kinds of events were very rare, although some of them were observed experimentally. Table III shows the number of such events observed in the experiments described in Table II. None of these events were predicted by MUSCA-SEP3, although a larger number of events were simulated with this tool (in the order of tens of thousands). For this reason, these rare events were also subject of study. The total number of bitflips (N_{BF}) is also added to the table.

It is noteworthy to observe that the majority of such events occurred in Experiments 7 and 8, where, in addition, the largest amount of bitflips were observed. As discussed above, each experiment involved a unique round of reading. Since there seems to be a correlation between the total number of bitflips in a round of reading and the appearance of these particular MCUs, it was suspected that some (or maybe all)

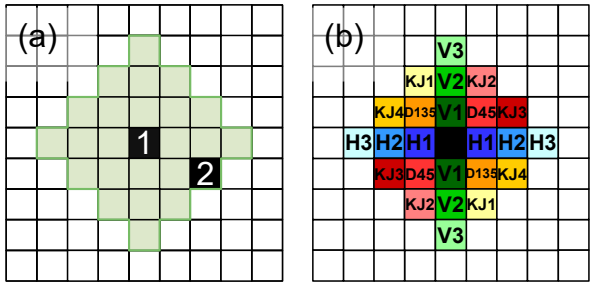

Fig. 5. a) Area of influence (colored cells) of a single bit upset (black cell "1") when MD=3. In this case, it is equal to $2 \cdot 3^2 + 4 \cdot 3 = 24$ cells. b) Relative abundance of each type of event. 2 possible events exist for each one of the 12 types displayed in Fig. 2.

of these events were a consequence of independent SBUs that coincidentally affected close SRAM bitcells and therefore, they were erroneously considered as part of the same multiple event. In previous works [23], [24], the authors studied that the probability of observing so-called "false" multiple events becomes non negligible if the number of bitflips that occurred in the same round of reading is high enough. In particular, if Manhattan distance is used as the metric to group bitflips into the same MCU, it was postulated that the expected number of false 2-bit MCUs is:

$$N_{F\_2bit\_MCU} = \frac{N_{BF} \cdot (N_{BF} - 1) \cdot MD \cdot (MD + 1)}{L_N} \quad (1)$$

Where N_{BF} is the number of bitflips occurred in the experiment, MD is the threshold value of the Manhattan distance used and L_N is the size of the memory in bits. This equation was developed by exploiting the idea that a given SBU has a so-called "area of influence" that is defined as the number of bitcells existing around it at a Manhattan distance lower or equal to MD. In [24], it was demonstrated that it can be obtained as: $2 \cdot MD^2 + 4 \cdot MD$. For instance (Fig. 5(a)), if MD=3, the area of influence of SBU "1" is 24 cells. If a second SBU "2" occurs within said area of influence, a false MCU will occur.

This idea can be used to answer the following question: How many false events of type KJ1-KJ4, H2, H3, V2 and V3 are expected to occur in an experiment where N_{BF} bitflips were observed in a memory with L_N bits, where a given Manhattan Distance MD is used to group bitflips into the same MCU?

For the expected number of false events of type KJ1-KJ4, looking at Fig. 5(b), one can note that there are 8 possible locations surrounding the black cell such that, if a second SBU affects one of them, a false "Knight Jump" event would appear. This can be understood as the area of influence of the black cell concerning KJ1-KJ4 events being 8 cells, which is ⅓ of the whole area of influence used to obtain $N_{F\_2bit\_MCU}$ in (1). Thus ($MD = 3$ is assumed):

$$N_{F\_2bit\_KJ} = \frac{N_{F\_2bit\_MCU}}{3} = \\ = \frac{N_{BF} \cdot (N_{BF} - 1) \cdot MD \cdot (MD + 1)}{3 \cdot L_N} = \\ = \frac{4 \cdot N_{BF} \cdot (N_{BF} - 1)}{L_N} \quad (2)$$

Similarly, the expected number of false events of types H2+V2 and H3+V3 would be the same, this time taking into account that the area of influence (4 cells) is ⅙ of the one used in (1) (or ½ of that of (2)). Therefore:

$$N_{F\_2bit\_H2+V2} = N_{F\_2bit\_H3+V3} = \\ = \frac{N_{BF} \cdot (N_{BF} - 1) \cdot MD \cdot (MD + 1)}{6 \cdot L_N} = \\ = \frac{2 \cdot N_{BF} \cdot (N_{BF} - 1)}{L_N} \quad (3)$$

The estimations given by these equations should be seen as "false event rates per experiment", which occur following a probability model given by a Poisson distribution. Thus, if the previous equations established that the event rate for a given experiment is μ_0, the probability of such false event occurring exactly k times is given by:

$$P_{false\_event}(\mu_0, k) = \frac{e^{-\mu_0} \cdot (\mu_0)^k}{k!} \quad (4)$$

Therefore, the probability of such false event occurring a number of times ranging from 0 to n is:

$$P^*_{false\_event}(\mu_0, n) = \sum_{k=0}^{n} \frac{e^{-\mu_0} \cdot (\mu_0)^k}{k!} \quad (5)$$

In the experiments, (5) was used to obtain the minimum value for n, n_{TH}, that makes the probability of observing false events a number of times ranging from 0 to n_{TH} above 99%. For that purpose, MD was set to 3 and L_N, to 16,777,216 (the 3 tested SRAMs had a size of 16 Mbits). As the expected number of false events is very low in all the experiments (between 0 and 1 in most of the cases), the accumulated probability for this Poisson distribution starts in 0 since $P_{false\_event}(\mu_0, 0)$ is not negligible.

Table IV shows the results for the experiments presented in Table III where these kinds of rare events showed up (Exp. Nº 4, 6, 7 and 8). In the table, n_{EXP} is the number of occurrences of each event type in the experiments.

The first observation that can be made is that all the events observed in Experiments Nº 4 and 6 are, most probably, false ones (whenever $n_{EXP} = 1$, $n_{TH} = 1$ too). For Experiments 7 and 8, two cases exist:

- If $n_{EXP} > 0$ and $n_{TH} \geq n_{EXP}$, it can be postulated that those events were all false with 99% probability. This happens in Exp. Nº 7 (H3+V3) and Exp. Nº 8 (H2+V2 and H3+V3).
- If $0 < n_{TH} < n_{EXP}$, maybe not all the observed events are false. In this case, there is 99% of probability that 2 of these H2+V2 events (Exp. Nº 7) are false ones and the other one is a true one. Therefore, it can be concluded that most of the 2-bit MCUs other than H1 and V1 are false and this explains the differences with MUSCA-SEP3.

TABLE IV
NUMBER OF "RARE" 2-BIT MCUS THAT WERE FOUND IN THE EXPERIMENTS AND COMPARISON WITH THE FALSE EVENT RATE PREDICTED BY (2) AND (3)

	Event type	Event rate	n_{TH}	n_{EXP}
Exp. Nº 4	KJ1-KJ4	0.063	1	1
	H2+V2	0.032	1	1
	H3+V3	0.032	1	0
Exp. Nº 6	KJ1-KJ4	0.029	1	1
	H2+V2	0.014	0	0
	H3+V3	0.014	0	0
Exp. Nº 7	KJ1-KJ4	0.816	3	0
	H2+V2	0.408	2	3
	H3+V3	0.408	2	1
Exp. Nº 8	KJ1-KJ4	0.634	2	0
	H2+V2	0.317	1	1
	H3+V3	0.317	1	1

The latter case will be the most common one in a situation where the discussed effects appear, such as in an accelerated experiment with a high particle fluence. The analysis provided in this section leaves the door open towards further discussions. Without loss of generality, and for MCUs of any multiplicity observed in the experiments, it can happen that: $0 < n_{TH} \ll n_{EXP}$. In that case, (1) can be used to correct the confidence intervals for the MCU rates that were extracted experimentally. A similar analysis can be made with equations predicting the number of false 3-bit events [24]. The estimation of false events with larger multiplicities still remains an open problem.

IV. SCALING TRENDS: TECHNOLOGY AND PARTICLE ENERGY

Results in the previous sections allowed postulating MUSCA-SEP3 as a good tool to estimate the shape of the 2-bit events. Thus, it has been used to study scaling trends for further technology nodes. More simulations have been made by emulating the impact of neutrons at different energies. These were obtained by shrinking the bulk CMOS technological floorplanning of the 65-nm that was used for the estimations of Figs. 3 and 4. In addition, since the type of particle did not seem to have a significant impact on the MCU contribution, the simulations in this section have focused only on a type of particle, in this case, neutrons.

In a first simulation, the neutron energy was set constant to 10 MeV and the {65-nm → 14-nm} nodes were analyzed. The heatmaps of Fig. 6 show the results, where the horizontal and vertical scales ("H offset" and "V offset") are the horizontal and vertical offsets between the two bitflips that belonged to the same event. Fig. 7 shows 3 examples of the value of these parameters for a horizontal, a vertical and a diagonal event. Squares with a darker color in Fig. 6 indicate the existence of more double events with the corresponding H and V offsets. Note that the square (0,0) is always blank (0 value) because no double event exists whose bitflips are 0 cells apart. Also, note that, since we are interested in the dispersion of the events,

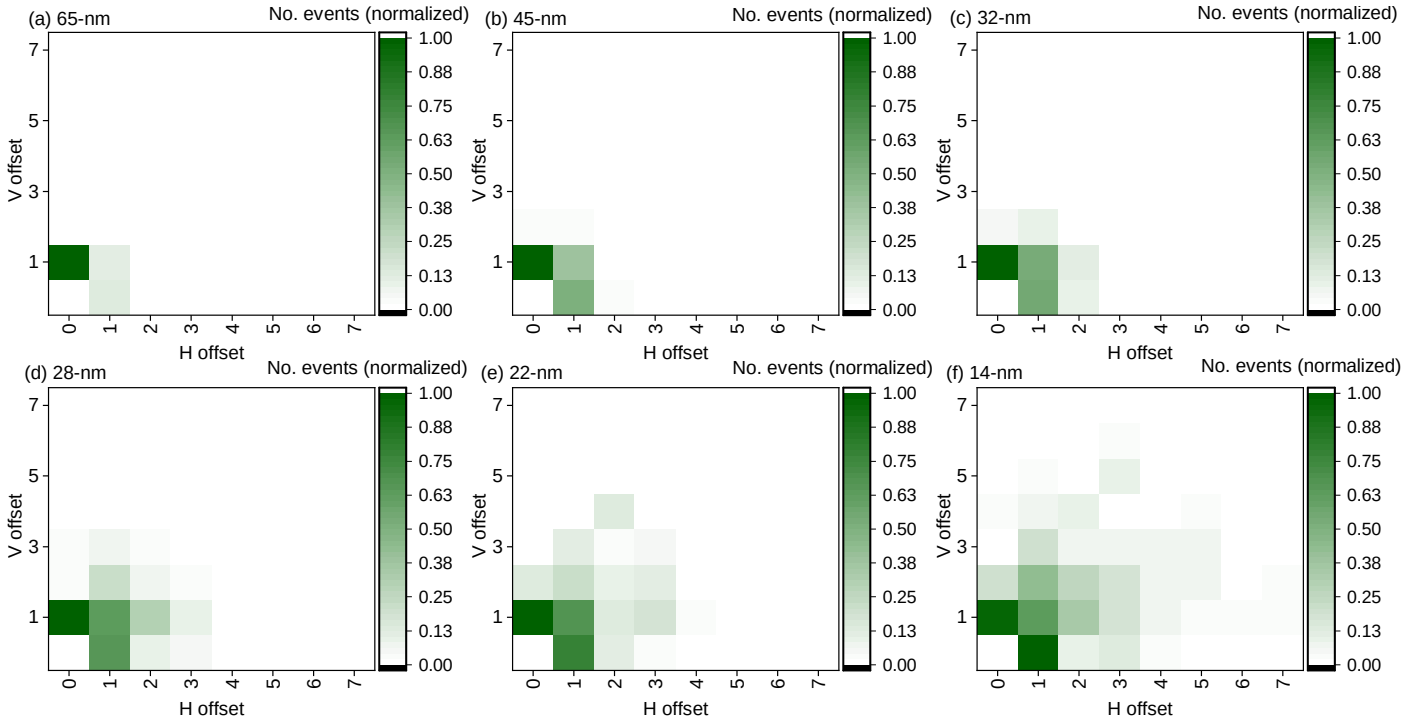

Fig. 6. Scaling trends for the shape of 2-bit events, for the nodes ranging from (a) 65-nm down to (f) 14-nm, for 10-MeV neutrons.

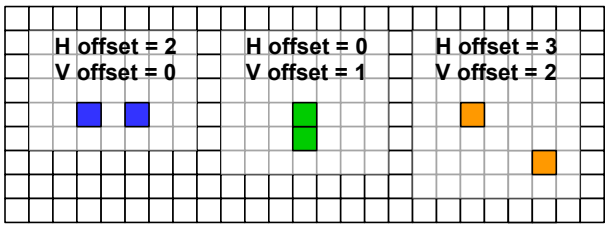

Fig. 7. Examples of 2-bit MCUs with various sizes and H/V offsets.

each heatmap displays normalized results with respect to the maximum number of events counted in each case.

In the figure it is clearly visible that, for the 65-nm node (top left subfigure), events have a clear preference for (H offset = 0; V offset = 1), which is precisely the V1 type of events displayed in Fig. 2. Indeed, this was the most numerous one in Figs. 3 and 4. However, starting from the 45-nm node, horizontal events are more prone to happen.

A conclusion that can be extracted in this figure is the need of using an increasingly high threshold distance (i.e., the value of Manhattan Distance parameter, MD, discussed in previous sections) in order to correctly identify all the double events as the technology scales down. For instance, with a value of $MD = 3$, 100% of the 2-bit events are captured for the 65-nm node (this also happens if $MD = 2$). However, for the 14-nm one, almost 16% of the events would not be accounted for if MD was 3 (in this case, a value of $MD = 7$ would be needed instead).

In order to verify if this trend is circumstantial to the neutron energy (10 MeV), more simulations with a spectrum of energies ranging from 10 MeV and 1 GeV in the same nodes as in Fig. 6 were carried out. All of them showed a very similar trend. Fig. 8 presents the results regarding neutron energy of 1 GeV. The differences between the heatmaps corresponding to the same technology node and various energies (10 MeV vs. 1 GeV) are visibly very minor. Nevertheless, it must be mentioned that, at a higher energy and with the same node, the H/V offsets tend to be higher too. This is not very visible in the subfigures due to the very high values displayed in the hottest squares of the heatmaps (for instance, up to 24,300 events in Fig. 8.a). This greater occurrence of events is clearly due to the sensitivity increase of the device against more energetic neutrons (10 MeV vs. 1 GeV), which is not surprising at all [7], [36]. In this case, the minimum values of MD to capture 100% of the events range from 2 to 12.

However, as pointed out in (1), increasing the value of MD in the researcher's criteria for extracting multiple events (while keeping the rest of the parameters constant) also increases the probability to observe false events by accumulation of simpler ones. Therefore, in a radiation-ground experiment, the total particle fluence should be adjusted accordingly in order to reduce the N_{BF} per round and therefore, to keep the probability of said event accumulation at a reasonably low value. Fig. 9 depicts this idea, by showing the expected number of false multiple events for different nodes, while keeping N_{BF} constant but increasing MD to correctly identify all the occurred multiple events. Results are normalized to the 65-nm case (10 MeV). The two discussed energies are displayed: 10 MeV and 1 GeV. In all the cases, L_N is also constant (hence, memories with the same size are assumed).

In both cases, the probability of false multiple event occurrence rapidly increases with the neutron energy if values of MD are selected such that 100% of the multiple events are

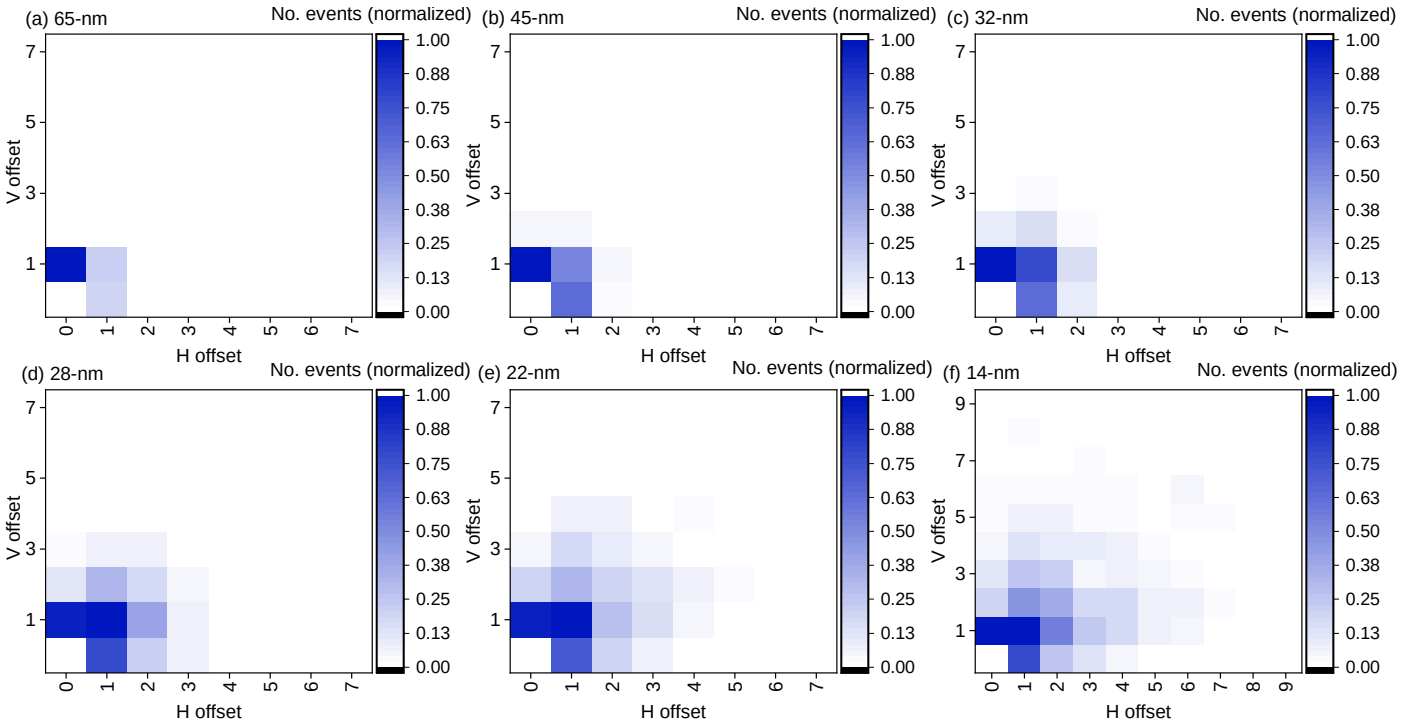

Fig. 8. Scaling trends for the shape of 2-bit events, for the nodes ranging from (a) 65-nm down to (f) 14-nm, for 1-GeV neutrons.

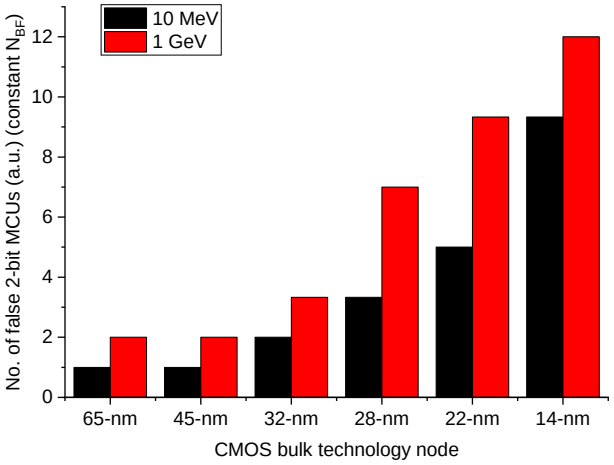

Fig. 9. Number of expected false 2-bit MCUs, for the values of MD needed to correctly identify all the multiple events. N_{BF} and L_N are assumed to be constant (parameters of (1)).

TABLE V
PER-BIT SENSITIVITY OF THE DEVICES OF TABLE I PREVIOUSLY OBSERVED BY THE AUTHORS IN [19]. RESULTS ARE NORMALIZED TO THE 90-NM NODE

Device	130-nm	90-nm	65-nm
SEU Sensitivity/bit	0.93	1	0.74

correctly identified. Indeed, the expected number of such false events is multiplied by 9.3 from the 65-nm node to the 14-nm one for 10 MeV; and by 12 in case of 1 GeV.

However, it is important to point out that this figure does not take into account the per-bit sensitivity change of bulk CMOS SRAMs as the technology scales down. Indeed, experimental results published in the literature [36] that studied the SER trends of various technology nodes have reported a sustained decrease in the SER/Mbit of the device. This was also observed by the authors in a recent work [19], where the 65-nm node per-bit sensitivity of the devices discussed in this paper (Table I) experienced a drop from the 90-nm to the 65-nm one (see Table V). MUSCA-SEP3 simulations were also carried out to confirm this trend, for nodes 65-nm down to 14-nm (Fig. 10). For these simulations, the SBU cross section, as well as the {2-bit $\rightarrow$ 8-bit} ones were firstly estimated, and finally weighed by the corresponding event multiplicity to obtain a realistic normalized number of expected bitflips depending on the node. These estimations are also consistent with Monte-Carlo simulations presented in other works [7].

Data discussed so far have shown that, as the technology scales down, for the same neutron fluence (at a constant energy), it is expected that, on the one hand, bitflips belonging to the same MCU are increasingly more distant, and on the other hand, the number of recorded bitflips (N_{BF}) decreases (considering memories with the same size). These two effects mutually cancel each other in (1), and it is interesting to evaluate the effect of both of them altogether. This is shown in Fig. 11, which depicts the expected number of false 2-bit MCUs when the neutron fluence is kept constant, for equally-sized memories with different technology nodes. In this figure, it is clear that the per-bit SEU sensitivity reduction shown in Fig. 10 is stronger than the effect of increasing MD (shown in Fig. 9) which leads to a sustained decrease in the per-bit number of false 2-bit events. However, there is an observation

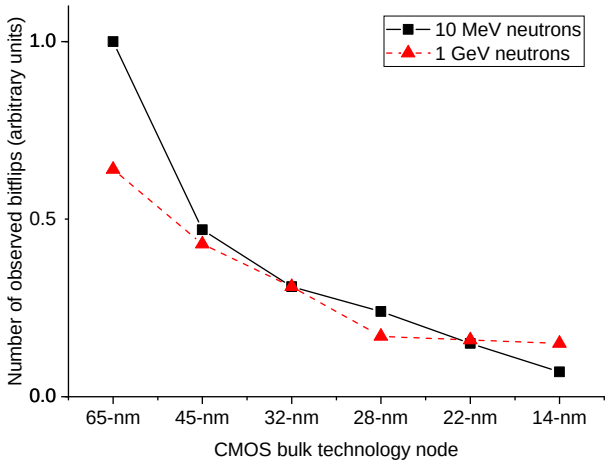

Fig. 10. SEU sensitivity trends, obtained with MUSCA-SEP3, for bulk CMOS technology nodes 65-nm down to 14-nm. 10-MeV and 1-GeV neutron energies are displayed. Results are normalized to the 10MeV&65-nm node.

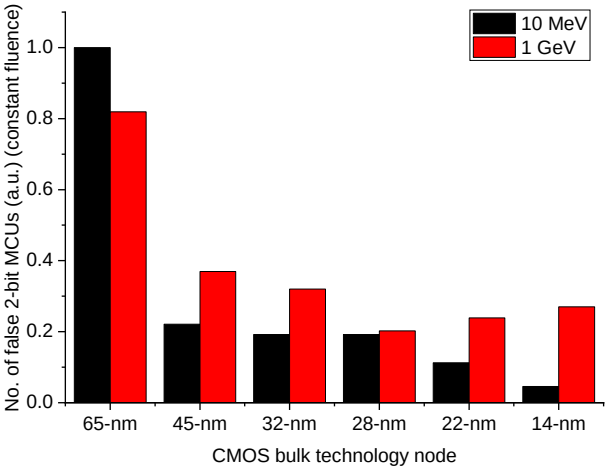

Fig. 11. Number of expected false 2-bit MCUs, for the values of MD needed to correctly identify all the multiple events. L_N and the total neutron fluence are assumed to be constant. Therefore N_{BF} changes according to the SEU sensitivity of the technology node (parameters of (1)).

to be made: for high-energy neutrons (1 GeV), the trend seems to invert from the 28-nm node. This is caused by the large dispersion of multiple events at higher energies. Since it is expected that technology miniaturization will continue in more modern SRAMs, this is an interesting hint of future work.

Finally, Fig. 12 reflects the effect of the neutron energy while keeping the technology node constant, thereby filling the gap of previous figures between 10 MeV and 1 GeV with the following intermediate energies: 30 MeV, 100 MeV and 300 MeV. In this case, the node was set to 14-nm. Results show that particle energy slowly impacts the H and V maximum offsets of the multiple events. Thus, for instance, the maximum (H or V) offset for 10 MeV is 7, whereas for 1 GeV, it would be 8. Similar trends were observed for the remaining nodes (not shown in the paper for simplicity).

V. Conclusions

This paper has studied the effect of technology scaling in the shape of 2-bit MCUs for bulk CMOS SRAM devices.

First, an experimental study made on 3 successive nodes (130-nm, 90-nm and 65-nm) has been presented. These results have been cross-checked with predictions issued from the MUSCA-SEP3 modeling tool. Predictions and experiments were in good concordance. A complementary analysis has also been made on these data, presenting the false multiple events that were found experimentally, however not predicted by MUSCA.

Then, the dispersion in the XY plane of these events has been studied as a function of neutron energy and miniaturization. Finally, its impact, together with the per-bit SEU decrease as technology scales down (previously reported in the literature and also estimated by the authors) has been analyzed and discussed.

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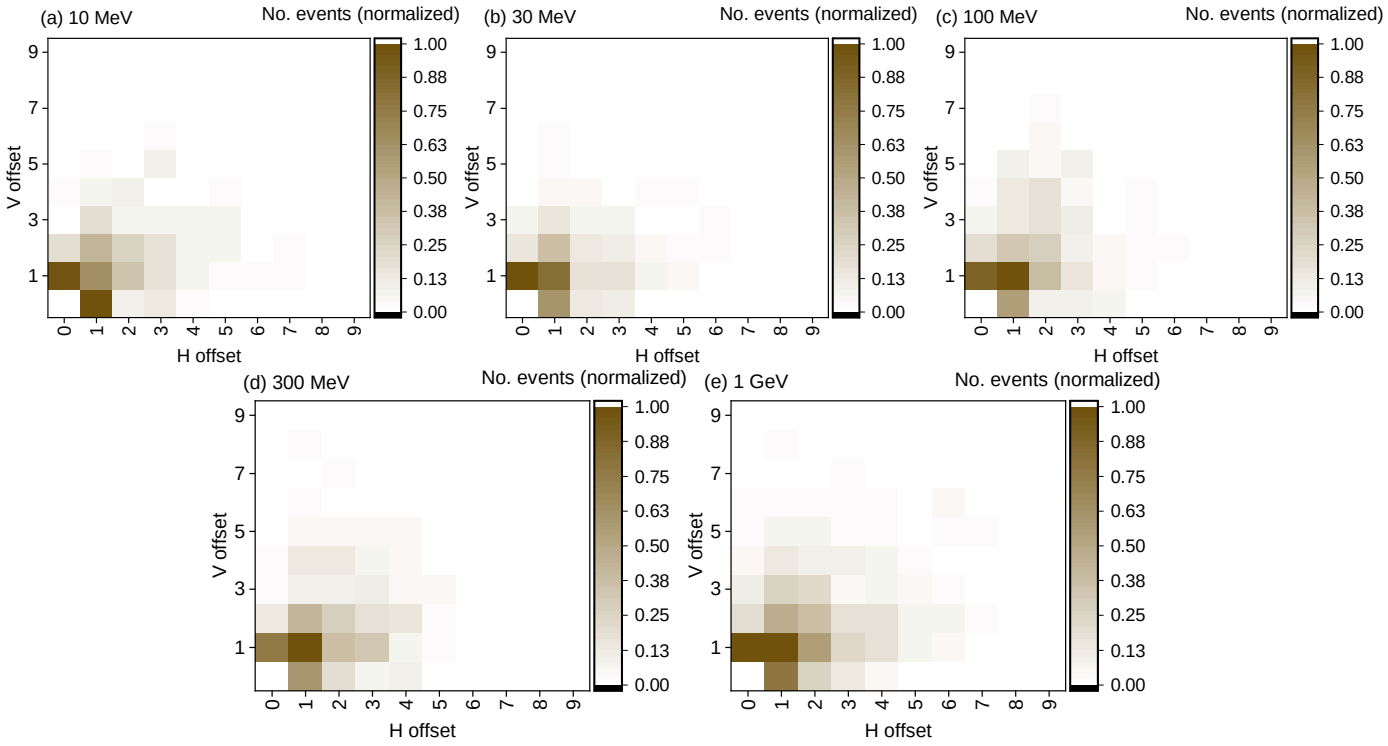

Fig. 12. Scaling trends for the shape of 2-bit events, for the 14-nm node, for neutron energies ranging from (a) 10 MeV down to (e) 1 GeV.

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