Evidence of the robustness of a COTS soft-error free SRAM to neutron radiation

R. Velazco, J. A. Clemente, G. Hubert, W. Mansour, C. Palomar, F. J. Franco,
M. Baylac, S. Rey, O. Rosetto, and F. Villa

***Abstract*—Radiation tests with 15-MeV neutrons were performed in a COTS SRAM including a new memory cell design combining SRAM cells and DRAM capacitors to determine if, as claimed, it is soft-error free and to estimate upper bounds for the cross-section. These tests led to cross-section values two orders of magnitude below those of typical CMOS SRAMs in the same technology node. MUSCA SEP3 simulations complement these results predicting that only high-energy neutrons (> 30 MeV) can provoke bit flips in the studied SRAMs. MUSCA SEP3 is also used to investigate the sensitivity of the studied SRAM to radioactive contamination and to compare it with the one of standard CMOS SRAMs. Results are useful to make predictions about the operation of this memory in environments such as avionics.**

***Index Terms*—COTS, LPSRAM, MUSCA SEP3, neutron tests, radiation hardness, reliability, soft error, SRAM**

I. Introduction

STATIC Random Access Memories (SRAMs) are widely used in electronic design for different purposes (e.g., to storage data in low-power systems, to extend the memory subsystem of a microprocessor through a Parallel Master Port (PMP) interface, etc.). The reliability of a system can be compromised if the information inside is corrupted by single or multiple upsets resulting from the impact of energetic particles (e. g., heavy ions, neutrons, alpha particles,...). In consequence, it is specially important to minimize the occurrence of soft errors. It is well known that this is relevant for applications devoted to operate in the Earth's atmosphere, even at the ground surface, where cosmic rays have decayed into a rain of particles, mainly neutrons in a wide range of energy: Thermal ($\lesssim$ 1 eV), spallation ($\sim$ 10 MeV), and high-energy neutrons ($\sim$ 100 MeV).

Several strategies have been proposed in last decades to deal with the potential increase of the sensitivity to radiation of advanced integrated circuits. Renesas Electronics, a Hitachi spin-off, redesigned the classical 6T-SRAM cell to minimize the occurrence of soft errors. The fundamental idea was to place the basic devices in several piled-up layers, creating a three-dimensional structure instead of distributing the devices on the wafer surface. This solution also allows creating additional capacitors. In planar technologies, the capacitive hardening technique induces associated area and speed penalties. Thus, despite an improvement in the single-event sensitivity, this technique is rarely selected as one of alternatives. Nevertheless, if somehow this hardening technique avoids the area penalty while keeping the time penalty small, the technique becomes an interesting option.

SRAM devices built from this technology, called Advanced Low Power SRAM (A-LPSRAM), are available in the market and can be used in common designs. Therefore, according to the potential market, it can be classified as a Commercial-Off-The-Shelf (COTS) device instead of typical rad-hard for space or military systems. In a compendium of experimental data done by NASA [1], the sensitivity of the A-LPSRAM to heavy-ions was studied putting in evidence that the device is not completely immune to soft errors. In the literature, only two references with scarce details have been published investigating its robustness with respect to neutrons [2], [3], which are the main particles present in the Earth atmosphere. In this paper, the behavior of this cell under 15-MeV neutrons is investigated and MUSCA SEP3 (MUlti-SCAles Single Event Phenomena Predictive Platform) [4] is used to extrapolate the obtained results for high energy neutrons. The α-emitter contamination is also discussed.

15-MeV neutron tests were performed in the GENEPI2 (GEnerator of NEutrons Pulsed and Intense) facility, which was used for the first time for performing radiation tests on integrated circuits.

II. Description of the cell

Keeping information in CMOS memory cells is, actually, equivalent to storing charge in specific capacitors. This fact is quite obvious in DRAM cells, where the cell keeps "1"if a capacitor is charged, and "0"otherwise. However, it is also valid for 6-T SRAM memories. In this case, charge is stored in parasitic capacitors such as the gate/bulk in ON transistors and the PN junction capacitances between the drain and bulk of the OFF transistors in the two coupled CMOS inverters. A bit-flip occurs when the charge is removed by an energetic ionizing particle that hits one or more capacitances and makes the cell flip.

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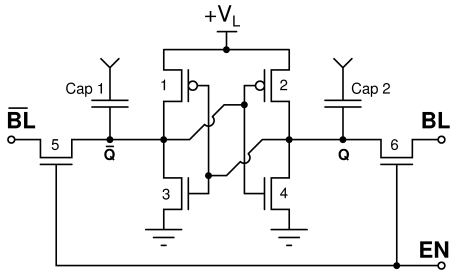
Raoul Velazco and Wassim Mansour are with the Université Grenoble-Alpes & CNRS, TIMA, Grenoble (France), e-mail: raoul.velazco, wassim.mansour@imag.fr.

Juan A. Clemente is with the Computer Architecture Department, Facultad de Informatica, Universidad Complutense de Madrid (UCM), Spain, e-mail: ja.clemente@fdi.ucm.es.

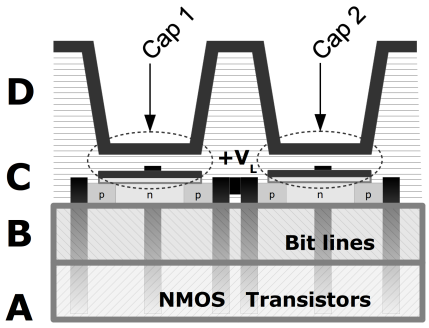
Guillaume Hubert is with the French Aerospace Laboratory (ONERA), Toulouse, France, e-mail: guillaume.hubert@onera.fr.

Carlos Palomar and Francisco J. Franco are with the Departamento Fisica Aplicada III, Facultad de Fisicas, Universidad Complutense de Madrid (UCM), Spain, e-mail: carlos.palomar, fjfranco@fis.ucm.es.

Maud Baylac, Solenne Rey, Olivier Rossetto, and Francesca Villa are with Laboratoire de Physique Subatomique et de Cosmologie LPSC, Université Grenoble-Alpes & CNRS/IN2P3, Grenoble, France, e-mail: baylac, solenne.rey, olivier.rosetto, francesca.villa@lpsc.in2p3.fr.



(a)



(b)

Figure 1. A typical 6T SRAM cell with extra capacitors (a). 3D-implementation of the circuit (b).

Many solutions were proposed and studied in the last decades to improve the Single-Event Upset (SEU) robustness of the SRAM cells. E.g., several Radiation-Hardened-By-Design (RHBD) memory cells are available in the literature: Heavy Ion Tolerant cell (HIT) [5], Dual Interlocked CEll (DICE) [6], Quattro [7], ... In these cells, the information is stored in at least 4 nodes so the discharge of only one capacitance is easily recovered. Other solutions consist in including additional resistors to the CMOS memory cell to filter the short peaks of current following the ion strike. Thus, the soft-error tolerance grows with the drawback of slowing down the cell response [8]. Also, some devices include redundant bits to incorporate error correction codes [9]. Finally, along with the purely CMOS-based technologies, new memories based on storing the information in the physical properties of new materials (MRAMS, PRAMs,...) have been developed [10]–[12]. As they do not store information as charge, they are immune to neutrons, heavy ions, etc. Unfortunately, they are not easily implementable in CMOS technologies. In consequence, it seems unlikely that, e. g., future generations of microprocessors or FPGAs include this kind of cells.

The advanced LPSRAM cell follows a very simple strategy. The trick is to increase the stored charge to make the bit-flip less likely to occur. As the typical power supply voltage is significantly lower in new technologies, the only way to increase the stored charge is by adding extra capacitors (Fig. 1a). However, the area penaly makes this choice unfeasible in many technologies.

This problem is solved in the advanced LPSRAM by building a 3D-structure instead of a planar one [2], [13], [14]. Fig. 1b shows a simplified schematic of how the advanced LPSRAM cell is built. The original picture on which this diagram is based can be found in the former references and has been simplified for illustrating purposes.

Basically, the cell can be divided into 4 layers (A to D in Fig. 1b). Connections among the layers A, B, and C are performed by means of vertical metallic columns. The deepest layer contains the 4 NMOS bulk transistors (3-6 in Fig. 1a). Above it, the layer B contains the bit lines (BL) and other signals. This layer is insulated by a dielectric from C, the upper layer. In this layer, two PMOS transistors are built. The main characteristic of these devices is that they are thin-film transistors (TFT) grown on a dielectric surface. Finally, a dielectric layer (D) separates the gates of the TFTs from a metallic layer with etched wells. This is the key-point to explain the robustness of the cell. The wells in the layer D, built using a DRAM-like technology, form capacitors with the gate of the PMOS transistors in such a way that the stored charge is increased. The manufacturer does not provide information about the node to which the other pad of the capacitor is connected (Ground, power supply, floating, ...). Besides, the use of vertical metallic columns avoids the creation of parasitic PNPN paths making the cell immune to single-event latch-up (SEL). This novel structure, in which capacitors, and transistors (PMOS, NMOS) share identical location on the XY plane, avoids the area penalty due to the incorporation of additional capacitors. Hence, the manufacturer claims that this cell in 150-nm CMOS technology occupies the same area as a cell in 90-nm planar CMOS technology.

To conclude, the temporal behavior and the power requirements (stand-by current and the quiescent current at 1 MHz) of this memory are similar to those of other pin-to-pin compatible conventional CMOS SRAMs.

III. Results

A. Description of the GENEPI2 neutron source

GENEPI2, a newly available facility under operation at LPSC (Laboratory of Subatomic Physics and Cosmology) de Physique Subatomique et de Cosmologie) was used for accelerated neutron testing of the studied SRAM memories [15]. This accelerator was originally developed to produce neutrons for nuclear physics experiments. It was used for the first time in 2013 to irradiate different types of SRAM memories.

GENEPI2 is an electrostatic accelerator producing neutrons by impinging a Deuterium ($^2_1$H) beam onto a fixed target. The target contains either Tritium ($^3_1$H or T) or Deuterium ($^2_1$H or D) according to the required neutron energy. After acceleration, ions of Deuterium (d) produce neutrons by one of the following processes:

- d + T $\rightarrow$ n + ^{4}He
- d + D $\rightarrow$ n + ^{3}He

The neutrons spread in all the directions with an average energy either of 14.2 MeV for the first reaction or of 2.5 MeV for the second reaction. For our irradiation campaigns, we only

consider, to first approximation, the neutrons emitted forward. In this case, the neutron energy is maximal: 15 MeV for d-T reaction and 3 MeV for d-D reaction.

An ion source, held at high voltage, generates the deuteron beam by ionizing Deuterium gas. The beam is shaped by a series of electrodes, and then accelerated at 250 kV through an accelerating column. After magnetic selection by a dipolar electromagnet, deuterons are guided through a $\sim$ 5 m long transport line, including focusing and steering elements. The beam line terminates with the target made of a Tritium or Deuterium compound.

Neutrons are emitted from the target in the whole accelerator room. LPSRAMs to irradiate are set facing directly the target at a distance determined to match the required neutron flux. Further neutron flux adjustments can be made by varying the average beam intensity on the target. While the LPSRAMs are fully exposed to neutrons, the readout electronic platform is protected by a dedicated neutron shielding. Neutron production is monitored continuously throughout experiments to determine the neutron dose for each irradiation.

To validate the method during this very first irradiation campaign, LPSRAMs were set at a fairly large distance from the target (40 cm) to limit the neutron flux to approximately 3×10^4 n·cm^{-2}·s^{-1}. Under these conditions, LPSRAMs were exposed to a fluence of 1.1×10^8 n·cm^{-2} within one hour.

B. Experimental results

A first neutron campaign at GENEPI2 was performed on an A-LPSRAM (R1LV1616RSA-5SI). This memory was biased at the nominal power supply (3.3 V) and written with a checkboard pattern, typically used in static tests. The memory is organized as a 2M×8 bytes (16 Mbit, 20-bit wide addresses) device and was continuously read during the radiation. No protection against latch-up was included in the 3.3-V power supply. Besides, the angle between the device surface and the neutron beam was 90°. Due to random rebounds over walls, some grazing neutrons are also expected. The irradiation was performed through the device front-side.

The device was tested for an hour until reaching the aforementioned total neutron fluence and *no bit-flip or latch-up was observed*. The absence of errors confirmed the immunity to neutrons of the studied A-LPSRAM. To certify these results, radiation ground tests in the same facility and conditions were performed on the pin-to-pin compatible Cypress SRAM memories, built in 90 and 130 nm technologies, and in these tests many errors were observed.

Everything suggests that the absence of errors is due only to the intrinsic robustness to radiation effects of this technology. These tests allow determining the upper bound of the cross section for this family of memories. Let us suppose that the cross section of this technology is σ, measured in cm^2/Mbit. After irradiating N Mbits with a 15-MeV neutron fluence of Φ n/cm^2, the expected number of bit-flips is

$$\mu = \sigma \cdot \Phi \cdot N. \tag{1}$$

It is well known that bit-flips are rare events and thus they can be depicted by means of a Poisson distribution. In this distribution, if N events are observed, the actual mean value, μ, is placed in the interval:

$$\frac{1}{2}\chi^2\left(\frac{1}{2}\left(1-\frac{k}{100}\right),2N\right) < \mu < \\ < \frac{1}{2}\chi^2\left(\frac{1}{2}+\frac{1}{2}\frac{k}{100},2\left(N+1\right)\right) \tag{2}$$

with a confidence of $k\%$. $\chi^2\left(x,p\right)$ is the chi-squared distribution with arguments x, p. As $N = 0$ and, e. g., $k = 95\%$, the value of μ is expected to be in the interval $\frac{1}{2}\chi^2\left(0.025,0\right) < \mu < \frac{1}{2}\chi^2\left(0.975,2\right)$. Therefore, $0 < \mu < 3.69$. Combining this with (1):

$$\sigma < \frac{3.69}{\Phi \cdot N} = \frac{3.69}{1.1\cdot10^8\cdot16} \simeq 2.1\cdot10^{-9}\ \frac{cm^2}{Mbit} \tag{3}$$

In terms of bits, the cross section becomes:

$$\sigma' = \frac{\sigma}{2^{20}} < \frac{2.1\cdot10^{-9}}{2^{20}} < 2.0\cdot10^{-15}\ \frac{cm^2}{bit} \tag{4}$$

The latch-up cross-section can be calculated in a similar way and in our case this value is below $3.36\cdot10^{-8}$ cm^2/device with a confidence of 95%.

As previously mentioned,two CMOS memories built in 90 and 130 nm CMOS technology, and pin-to-pin compatible with the Renesas memory were also tested in the GENEPI2 facility in identical conditions in order to put in context the A-LPSRAM results. In these memories, no Multiple Bit Upset (MBU) was observed but, sometimes, errors strangely appeared in logic addresses differing in one or two bits, fact that is interpreted as the occurrence of a multiple event in a memory with interleaving. Therefore, they were classified as Multiple Cell Upsets (MCU). Concerning the single upset events, the 130-nm memory underwent 98 SEUs after reaching a total neutron fluence of $1.07\cdot10^8$ n/cm^2 ($\sigma_{SEU} = (9.1 \pm 2.5)\cdot10^{-14}\ cm^{-2}$) and the 90-nm one, 92 ($\sigma_{SEU} = (8.1 \pm 2.3)\cdot10^{-14}\ cm^{-2}$). Concerning the multiple events, in the 130-nm memory, 17 2-bit MCUs and 7 3-bit MCUs were observed during the tests while in the 90-nm memory 8 2-bit, 3 3-bit and even 4 4-bit MCUs were reported. Thus, the total number of bit-flips detected in the 130-nm and the 90-nm SRAMs were respectively 153 and 133.

IV. Analysis and discussion

According to the manufacturer, advanced LPSRAMs offers a lower soft-error rate than other similar devices built in planar technologies. If so, the 15-MeV neutron cross-section must be much lower than those of equivalent devices not only in our own results but also in those reported in the literature. Table I shows a review of the SEU cross-section found in the literature focusing on commercial SRAM devices ranging from 90 to 180 nm CMOS technologies. These results were mainly extracted from works by Baggio [16], Normand [17], Hands [18], and Miller [19]. For brevity, works are called Bag07, Nor10, Han11, and Mil13 in the Table I. These authors include values of other devices that were discarded in this study due to either they were built in very old technologies (250 nm or more), the technology could not be identified, or the devices were rad-hard. Other references were found in the literature

Table I
SUMMARY OF CROSS SECTIONS FOUND IN THE LITERATURE.

Reference	Alias	Manufacturer	Tech.	σ (cm^2/bit)
Bag07	B2	Not reported	180 nm	$2.1 \cdot 10^{-14}$
	B3	Not reported		$2.5 \cdot 10^{-14}$
	A2	Not reported		$5.7 \cdot 10^{-14}$
Nor10	D	Not reported		$4.0 \cdot 10^{-14}$
	3	Not reported		$8.3 \cdot 10^{-14}$
	BS62...	BSI		$2.9 \cdot 10^{-14}$
	K6R4...	Samsung		$2.4 \cdot 10^{-14}$
	AS7C...	Alliance		$2.5 \cdot 10^{-14}$
Han11	BSI New	BSI		$4.7 \cdot 10^{-14}$
Nor10	2	Not reported	130 nm	$3.0 \cdot 10^{-14}$
	4	Not reported		$2.5 \cdot 10^{-14}$
Han11	CypE55	Cypress	90 nm	$4.5 \cdot 10^{-13}$
	CypE45	Cypress		$2.5 \cdot 10^{-13}$
Mil13		Cypress		$8.2 \cdot 10^{-15}$
				cm^2/bit

but are not included since the cross section is expressed in arbitrary units.

The SEU cross-sections in this set of devices are one or two orders of magnitude above the calculated upper bound for the studied A-LPSRAM memory. There is only one 90-nm device (Mil13) that shows a value of the cross-section on the order of that of the A-LPSRAM. The reason of this disagreement is the irradiation side. Unlike other works, including ours, Miller *et al.* measured this value irradiating *through the backside* to investigate an interesting phenomenon: 14-MeV neutron irradiations through the backside provoke several times less bit-flips than front-side irradiations. This can be explained by the presence, in the front side, of passivation layers rich in oxygen. Oxygen easily reacts with neutrons with energies below 50 MeV yielding recoil ions with higher ionizing power. This fact confirms that this technology is less sensitive to the 15-MeV neutrons than other similar devices in planar technology and validates the manufacturer's claim.

Years ago, the A-LPSRAM developers [14] reported that thousands of memories were tested for long periods without observing any bit-flip. These real-life tests were equivalent to exposing a 16-Mbit memory to natural radiation for 15,111,232 h at sea level. As exposed in Section III-B, from this result it is easy to estimate that the experimental soft error rate is lower than 15.4 FIT/Mbit with a 95% confidence (1 FIT = 1 error every 10^9 h). However, let us bear in mind that these promising results do not rule out the occurrence of soft error. On the Earth's surface, the products of the collisions of the primary cosmic rays with the atmosphere are mainly neutrons divided into three categories: High energy, spallation, and thermal neutrons [20]. Spallation neutrons can be ruled out since their energy (∼0.1-10 MeV) is in the same energy range as the 15-MeV neutrons used in the GENEPI2 experiments.

Regarding the thermal neutrons, bit-flips occur only if the neutron is captured by a ^{10}B nucleus and, in consequence, an alpha particle of 1.4 MeV is emitted. SRIM[1] calculations [21] show that the highest LET value of alpha particles in silicon is not higher than $\sim$ 1.5 MeV/cm^2/mg, corresponding to energy values about $\sim$ 0.5 MeV. Heavy ions experiments described in [1] led to a cross section of $\sim 3 \cdot 10^{-14}$ cm^2/bit with $LET = 1.7$ MeV/cm^2/mg. Besides, the chances of a boron nucleus capturing a thermal neutron is extremely low in technologies below 180 nm due tu the removal of the borophosphosilicate glass (BPSG) layers [22]. In conclusion, SEUs in the A-LPSRAM due to alpha particles coming from thermal neutrons are unlikely, or even not possible. A fact supporting this assertion is the complete absence of single events during the 15-MeV neutron irradiation even though recoil ions show LET values up to 8 MeV/cm^2/mg [19].

In addition, this analysis allows ruling out the occurrence of soft errors by alpha particles originating in radioactive impurities, such as the nuclei in the uranium and thorium decay chains, and some isotopes of platinum [23]–[25].

High-energy neutrons make up the last possible source of bit-errors. Their effects will be studied in the following section using the MUSCA SEP3 tool.

V. MODELING RESULTS WITH MUSCA SEP3

As it was previously said, 15-MeV neutrons in silicon only produce nuclear reaction yielding secondary ions with a LET below 8 MeV/cm^2/mg [19]. However, high-energy neutrons in the atmosphere can produce recoil atoms with larger values of LET that can eventually lead to the occurrence of bit-flips. To get an objective feedback about this possibility, simulations were performed using MUSCA SEP3 [4], including the atmospheric environment and the intrinsic alpha-impurities.

A. MUSCA SEP3 description

The development of this tool, started in 2007, aimed at proposing approaches adapted to nanometric technologies. It is based on the modeling of the successive mechanisms that occur between the entrance of a particle into matter and the SEE occurrence, including the environment descriptions [26], the radiation interaction [4], the transport/collection mechanisms at physical level [27] and the electrical mechanisms [28]. Alpha-emitting impurities can be found in some packaging materials, chemicals and materials used in the fabrication process of the chip. The emission rate can strongly vary depending on the quantity and purification grade of these materials. The α-emitter contamination effect is considered here as the sum of the package and wafer contributions. Four alpha emission categories can be considered for the package, the hyper-low-alpha (*HLA*, $\varepsilon < 5 \cdot 10^{-4}$ $\alpha/cm^2/h$), the ultra-low-alpha (*ULA*, $\varepsilon < 10^{-3}$ $\alpha/cm^2/h$), the low-alpha (*LA*, $\varepsilon < 10^{-2}$ $\alpha/cm^2/h$)

[1]SRIM: Stopping and Range of Ions in Matter

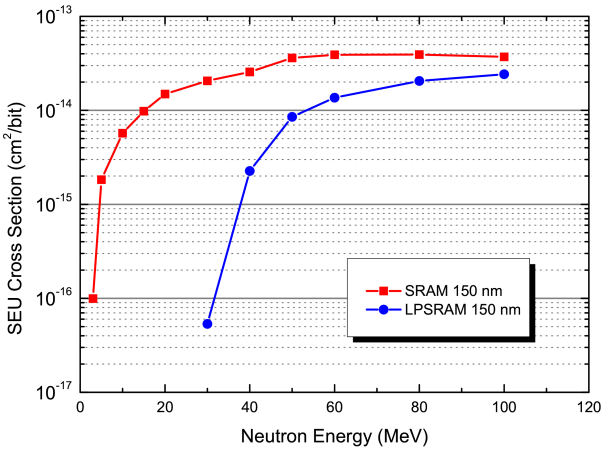


Figure 2. Neutron SEU cross-sections issued from MUSCA SEP3 calculations for the 150 nm 6T SRAM cell with (LPSRAM) and without extra capacitors implemented in 3D.

and the standard (S, $\varepsilon \sim 10^{-2} - 10\ \alpha/cm^2/h$), the alpha emissivity induced by the wafer contamination being typically much lower [29], [30].

Then, multi-physics modeling was applied to the advanced A-LPSRAM device investigated in this work. Two technologies were considered: firstly a typical 150-nm 6T SRAM cell and secondly the same technology with extra capacitors implemented in 3D.

B. Results and discussion

Fig. 2 presents the neutron SEU cross-sections issued from MUSCA SEP3 calculations in the neutron energy range from 1 MeV to 100 MeV. Results confirm the immunity to soft errors for 15-MeV neutrons. The neutron energy thresholds are respectively 3 and 30 MeV for the SRAM and LPSRAM. Moreover, SEU saturation cross-sections are very close. These results are consistent with experiments presented in [1], i.e., SEUs are observed at both 89 and 198 MeV proton energies.

It is possible to deduce the neutron Single Event Rate (SER in FIT/Mbit) thanks to the SEU cross-sections and the neutron spectrum. Moreover, the α-SER can be deduced from the emissivity value and the α-cross-section issued from calculations. Table II summarizes the neutron and α-SER obtained for the both devices and considering the ground and avionic altitudes. The neutron spectrum are issued from QARM (Quotid Atmospheric Radiation Model) tool [31], [32].

Besides, it is interesting to use the data related to the A-LPSRAM issued from MUSCA SEP3 to analyze the expected soft error rate at ground level in combination with QARM. Calculations indicate an estimated soft error rate of 58 FIT/MBit. The SEU threshold is greater than the deposited charge by alpha particles. Thus, the A-LPSRAM is not sensitive to alpha impurities. In Section IV, the experimental soft error rate was estimated below 15.4 FIT. Both values are on the same order, and the discrepancies can be attributed to the lack of technical information when the A-LPSRAM memory was modeled in MUSCA SEP3. QARM tool also predicts that, at 12-km above Toulouse (France), the expected soft error rate is 17400 FIT/MBit.

Table II
MUSCA SEP3 PREDICTIONS OF THE ESTIMATED VALUES OF THE SOFT ERROR RATES IN 150-NM DEVICES.

Altitude	**Conventional SRAM**						
	Neutron	**Alpha**			**Total**		
		HLA	ULA	LA	HLA	ULA	LA
0 m	206	1240	2270	23860	1446	2476	24066
12 km	68500				69740	70770	92360
	FIT						

	A-LPSRAM				
	Neutron	**Alpha**			**Total**
		HLA	ULA	LA	HLA, ULA, LA
0 m	58	0			58
12 km	17400	0			17400
	FIT				

Surprisingly, MUSCA SEP3 also forecast that, without capacitors, the soft error rate of a 150-nm planar CMOS cell is 206 FIT/MBit (68500 FIT/MBit at 12-km height). This result is not coherent with experimental data obtained in real-life tests [33], in which soft error rates on the order of 3000 FIT/MBit are observed in 130-nm CMOS memories. However, another work also performed on 130-nm memories, quite similar to the 150-nm technology, helps to solve this contradiction [34]. According to this paper, the tested memory showed an estimated soft error rate of 2489 FIT/Mbit at New York City. However, only a small fraction (409 FIT/MBit) is attributed to the effect of atmospheric neutrons and most of the errors are caused by alpha contamination (2080 FIT/MBit). This value of neutron-induced soft error rate is on the same order of the value predicted by MUSCA SEP3 & QARM for generic 150-nm technology, and allows extracting an interesting conclusion: The key of the low value of the A-LPSRAM soft error rate is not its tolerance to cosmic rays but the complete removal of the alpha particle contribution.

Thus for the standard SRAM technology, calculations performed by MUSCA SEP3 give an α-SER equal to 1242, 2270, and 23860 FIT/Mbit for HLA, ULA, and LA hypothesis, respectively. The orders of magnitude issued from HLA and ULA are consistent with underground experiments [34], [35]. On the contrary, SEUs induced by alpha-emitter were not observed for the A-LPSRAM devices. The A-LPSRAM is clearly better than the standard CMOS SRAMs at ground level, because its SEU threshold is higher than the alpha LET or energy deposition capability. Because of the neutron nuclear interactions, which yield secondary heavy ions characterized by a LET above the SEU threshold, the neutron contribution to SER is not negligible and must be taken into account for applications devoted to work at aircraft altitude.

VI. CONCLUSIONS AND FUTURE WORK

In this work were presented the neutron-test and simulation results obtained for a COTS SRAM with intrinsic SEU fault-tolerance resulting from a new design concept including capacitors benefitting of the 3D avoiding thus area penalties. Presented results provide experimental evidences on the immunity of the tested Advanced LPSRAM which did not show soft errors or latch-up during the tests performed with a 15-MeV neutron source at GENEPI2 facility available

at Grenoble and used for the first time to perform radiation ground test on integrated circuits. Our calculations show that the cross section is at least one or two orders of magnitude beneath the one of similar SRAM devices built in other general CMOS technologies. A consequence of these tests is that the pernicious events due to thermal neutrons, spallation neutrons, and radioactive impurities are ruled out. MUSCA SEP3 simulations also show that the threshold neutron-energy necessary to trigger a single event is on the order of 30 MeV. Therefore, of A-LPSRAM devices can be considered for being used critical systems devoted to operate in environments where mainly neutrons are a challenge to the reliability. Moerover, combining experimental results and predictions made with MUSCA-SEP3 tool allowed to put in evidence the absence of soft errors due to radioactive contamination which is one of the main advantages of A-LPSRAMS.

Recently, Renesas has announced the release of a new generation of 110-nm CMOS technology A-LPSRAM devices during 2014. In future work these devices will be tested in order to verify that the SEU mitigation strategy is in this case independent of the integration scale. To enhance the impact of these next radiation test campaings, different situations will be considered, such as: dynamic tests using patterns such as March, different ultra-low values of the power supply, etc.

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