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Gate quality of *ex situ* deposited Al/SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ devices after rapid thermal annealing

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Abstract. *Ex situ* deposited SiN_x:H/$In_{0.53}Ga_{0.47}As$ metal–insulator–semiconductor devices, with a minimum of interface state density of 3.5×10^{11} eV^{-1} cm^{-2} have been obtained by electron cyclotron resonance plasma method at a low substrate temperature (200 °C), after a rapid thermal annealing treatment. The effects of annealing temperature on interfacial and bulk electrical properties have been analysed using the C–V high–low frequency method and I–V measurements. The results show that, up to 600 °C, the annealing procedure gradually improves the interface properties of the devices. The frequency dispersion, the hysteresis and the interface trap density diminish, while the resistivity and the electrical breakdown field of the insulator film increase up to values of $8 \times 10^{15}\,\Omega$ cm and 4 MV cm^{-1}, respectively. We explain this behaviour in terms of the thermal relaxation and the reconstruction of the SiN_x:H lattice and its interface with the $In_{0.53}Ga_{0.47}As$. At higher annealing temperatures, a sharp degradation of the structure occurs.

1. Introduction

Metal–insulator–semiconductor field effect transistor (MISFET) horizontal technology is very promising in comparison to vertical devices, such as heterojunction bipolar transistor (HBT), because it is easily integrated into a circuit. III–V semiconductor compounds are very suitable for high speed and high frequency MISFET applications due to their excellent electrical properties, especially $In_{0.53}Ga_{0.47}As$ because its surface does not exhibit strong Fermi level pinning as it is usual in GaAs or InP binary compounds. However, good control and characterization of the insulator–semiconductor interface is needed for obtaining a high quality device performance. This is usually achieved by passivation of the semiconductor surface with the formation of a Si interface control layer prior to the insulator deposition [1–3] or with $(NH_4)_2S_x$ chemical treatments.

It has been recently reported that electron cyclotron resonance (ECR) plasma technique provides SiN_x:H/ III–V (GaAs [4, 5], InP [6] and $In_{0.53}Ga_{0.47}As$ [3]) semiconductor interfaces with appropriate characteristics, because of low radiation damage of the surface, and low deposition temperature which prevent evaporation of the volatile species from the III–V semiconductor [7, 8].

We have demonstrated that post-deposition rapid thermal annealing treatment at moderate temperatures promotes interface improvements on SiN_x:H/InP devices without any surface passivation procedure of the semiconductor surface prior to the SiN_x:H film deposition [9, 10].

In this paper, we enlarge the analysis of the influence of post-deposition annealing temperature on the electrical characteristics of MIS structures to n-$In_{0.53}Ga_{0.47}As$. We report on the results obtained on *ex situ* deposited SiN_x:H/$In_{0.53}Ga_{0.47}As$ devices with a post-deposition rapid thermal annealing procedure. These MIS capacitors show small frequency dispersion, small hysteresis and a minimum interface trap density of 3.5×10^{11} eV^{-1} cm^{-2}.

2. Experimental details

$In_{0.53}Ga_{0.47}As$:S epilayers were grown by metal organic vapour phase deposition (MOVPE) lattice-matched to (100) InP:S, supplied by EPI†, with a net donor concentration of 6.6×10^{15} cm^{-3}. The SiN_x:H films were deposited by ECR plasma technique. The reactor was an Astex 4500 attached to a deposition chamber, and the precursor gases were N_2 and SiH_4. The film stoichiometry was controlled by the gas flux ratio $R = N_2/SiH_4$, which was kept constant at $R = 5$. This is because the films obtained with flux ratios equal or greater than 5 are N-rich [11] and, according to our studies, they show the optimum electrical characteristics, as is commonly observed in others III–V MIS devices [11]. In all depositions, the total partial pressure and the substrate temperature were fixed at 0.6 mTorr and 200 °C, respectively. Prior to dielectric deposition, substrates were ultrasonically

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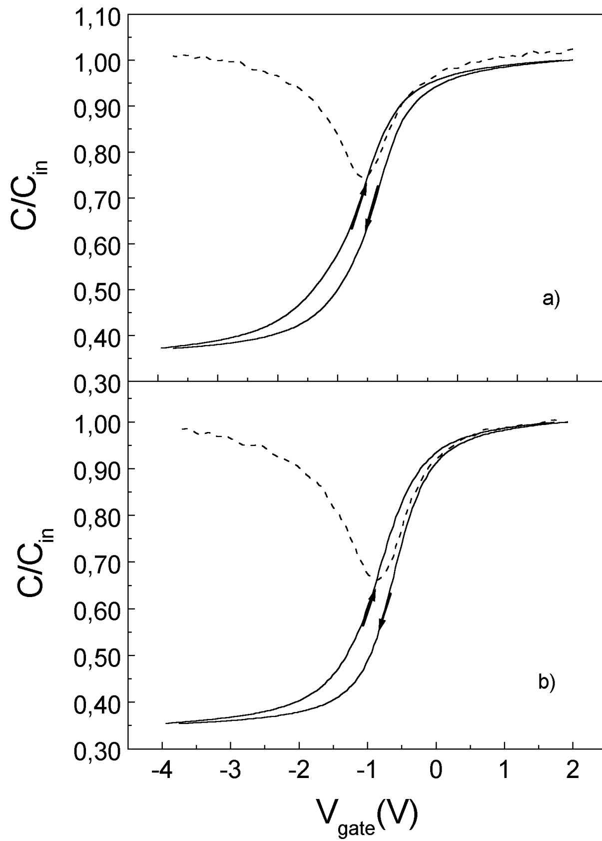

Figure 1. High-frequency (full curve) and quasistatic (broken curve) *C–V* characteristics versus gate voltage for Al/SiN_x:H/$In_{0.53}Ga_{0.47}$As capacitors: (a) non-annealed and (b) annealed at 600 °C for 30 s.

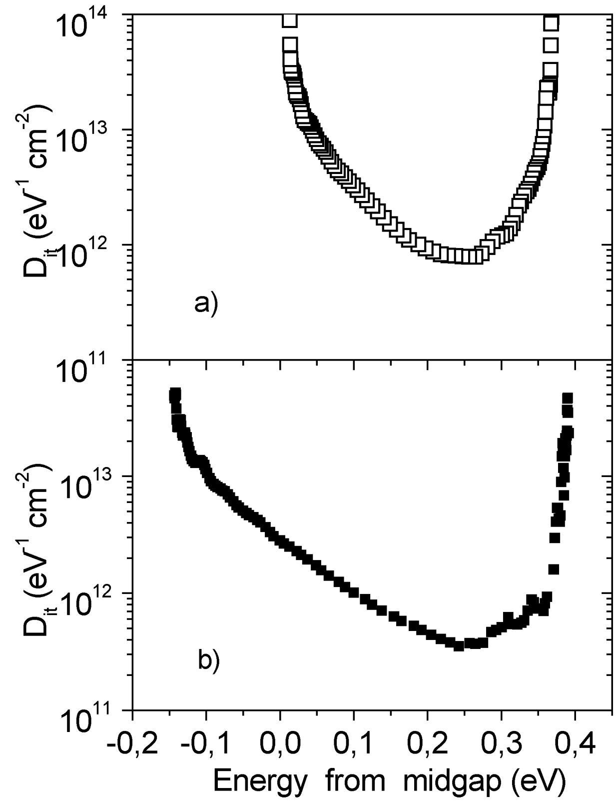

Figure 2. Distribution of interface trap density versus gap energy relative to the midgap for the *C–V* curves of figure 1:
(□) non-annealed Al/SiN_x:H/$In_{0.53}Ga_{0.47}$As;
(■) Al/SiN_x:H/$In_{0.53}Ga_{0.47}$As annealed at 600 °C for 30s.

degreased in trichlorethylene, acetone and propanol and deoxidized in HCl:H_2O (1:3) for 1 min before drying in N_2. Deposition of about 500 Å thick films was performed without any additional *in situ* treatment. Afterwards, an *ex situ* RTA of the structures was carried out with temperatures ranging from 400 °C to 700 °C, during 30 s, in Ar atmosphere. 1.2×10^{-3} cm^2 Al dots were thermally evaporated through a shadow mask as gate electrodes, whereas the back electrode was formed with an AuGe/Au film. A post-metallization annealing was done at 300 °C for 20 min in Ar atmosphere.

3. Results and Discussion

The SiN_x:H/$In_{0.53}Ga_{0.47}$As interface was characterized by measuring the *C–V* quasistatic and high-frequency dependences with a Keithley model 82 system, with sweep rates of 285 mV s^{-1}. Pure quasistatic behaviour is obtained at this high sweep rate, because no deformation of the quasistatic *C–V* curve is observed. *C–V* characterization at lower sweep rate (100 mV s^{-1}) has been performed, but it resulted in noisy measurements for some samples. The interface trap density (D_{it}) was calculated using the high-low frequency method [12]. The electrical properties of the insulator films (resistivity, ρ, and breakdown field, E_B) were obtained by measuring the *I–V* characteristics in the accumulation zone of the MIS structures.

Figure 1 compares the *C–V* curves of an Al/SiN_x:H/$In_{0.53}Ga_{0.47}$As before and after a rapid thermal annealing at 600 °C for 30 s. As a comment, and contrary to what occurs in Si-based MIS capacitors, III–V MIS structures show symmetric low-frequency *C–V* curves, as it is extensively reported for $In_{0.53}Ga_{0.47}$As-based devices [13] and in other similar III–V compounds, like GaAs [14, 15]. This effect is probably due to the distributed interface gap states, but further measurements are necessary to demonstrate it. The annealing cycle at 600 °C during 30 s results in the lowest D_{it}. It is clear that the annealing induces remarkable improvements in the *C–V* characteristics. A more pronounced dip of the quasistatic curve and a smaller hysteresis (from 240 meV to 160 meV) of the high frequency curve after the annealing are observed, i.e. a decrease in the density of slow interface traps. Moreover, the frequency dispersion of the capacitance in depletion and accumulation regions is drastically reduced, i.e., a reduction of the tunnelling-related traps, responsible for this effect in SiN_x:H/$In_{0.53}Ga_{0.47}$As [3], is achieved after the annealing treatment.

The distribution of the interface trap density within the forbidden gap obtained for the *C–V* characteristics for the devices of figure 1 is shown in figure 2. It is seen that an annealing at 600 °C reduces the minimum of D_{it} from 7.5×10^{11} to 3.5×10^{11} eV^{-1} cm^{-2}, whereas the surface potential modulation improves from 0.37 to 0.53 eV. If we compare our results with those obtained by other authors [3, 13, 16] we realize that similar interface characteristics could be obtained

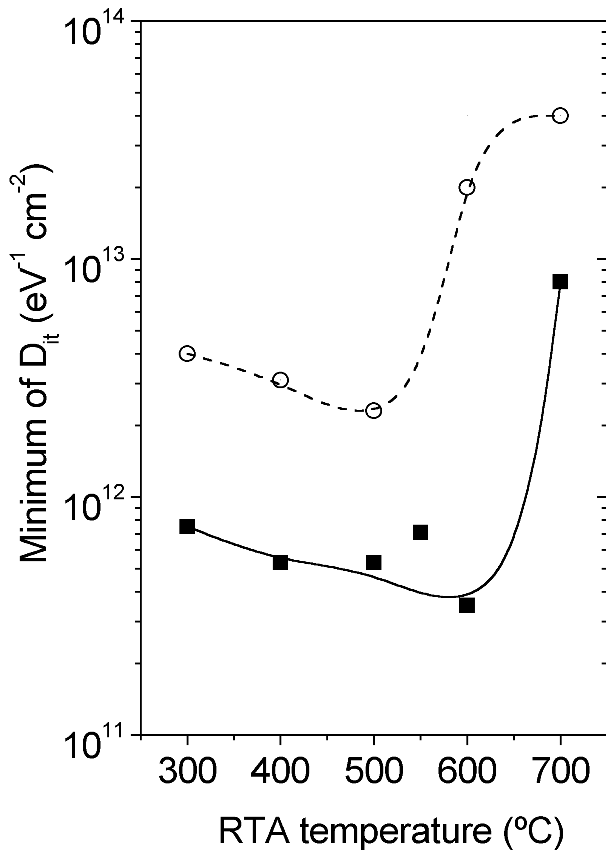

Figure 3. Influence of the RTA temperature over the minimum of the interface trap density: (○) Al/SiN$_x$:H/InP, (■) Al/SiN$_x$:H/In$_{0.53}$Ga$_{0.47}$As capacitors. Lines are drawn as a guide for the eye.

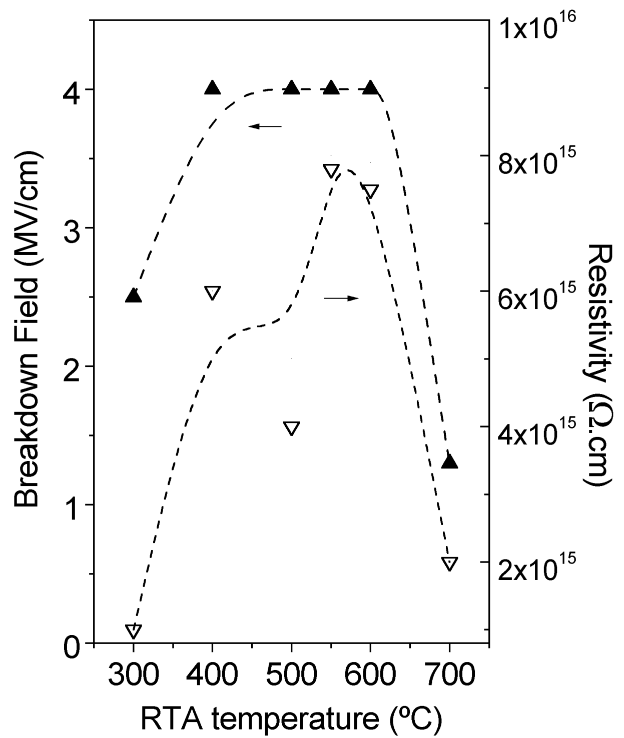

Figure 4. Electrical breakdown field (▲) and resistivity (▽) for Al/SiN$_x$:H/In$_{0.53}$Ga$_{0.47}$As capacitors, as a function of the RTA temperature. Lines are drawn as a guide to the eye.

for our *ex situ* SiN$_x$:H/In$_{0.53}$Ga$_{0.47}$As structures with a post-deposition RTA (3.5×10^{11} eV^{-1} cm^{-2}), compared with the *in situ* deposited samples with a silicon interface control layer reported by Mui *et al* [3, 13] (2.4–4 $\times$ 10^{11} eV^{-1} cm^{-2}). It should be pointed out that these authors calculated the distribution of interface trap density by the conductance method. Anyway, the accuracy of the conductance and the high–low frequency capacitance methods are comparable when the interface trap capacitance (C_{it}) and the depletion layer capacitance (C_D) are of the same order of magnitude [12], as occurs in this case ($C_{it} \approx 63$ pF against $C_D \approx 90$ pF). This result proves the effectiveness of the RTA method to reduce the interface trap density up to values of the order of those obtained in *in situ* deposited devices with Si interface control layer.

Figure 3 shows the minimum of the interface trap density versus the rapid thermal annealing temperature for SiN$_x$:H/n-In$_{0.53}$Ga$_{0.47}$As devices. As a comparison, we also show in the same figure the dependence of the interface trap density minimum on SiN$_x$:H/n-InP capacitors where the insulator was deposited at the same conditions that SiN$_x$:H/n-In$_{0.53}$Ga$_{0.47}$As devices, i.e. $R = 5$ and 500 Å thickness. It is evident that the behaviour of the D_{it} minimum with the annealing temperature is quite similar for both types of devices: a slight improvement with annealing temperature, up to values ranging from 500 °C to 600 °C where the D_{it} minimum is achieved, and a sudden increase for higher temperatures is observed. However, there is a significant difference: the temperature at which the degradation of the interface properties takes place is one hundred degrees higher for the SiN$_x$:H/In$_{0.53}$Ga$_{0.47}$As devices. This fact is probably due to the P outdiffusion towards the insulator in SiN$_x$:H/n-InP capacitors when they were subjected to an RTA, as evidenced by DLTS [9] and Auger measurements. Perhaps As does not diffuse so quickly as P, SiN$_x$:H/n-In$_{0.53}$Ga$_{0.47}$As structures improve up to higher annealing temperatures, and the device degradation does not take place until 600 °C.

In figure 4 we present the values of the bulk insulator resistivity and the breakdown field, as a function of the annealing temperature. A significant improvement of both parameters with the annealing temperature is observed. Between 500 °C and 600 °C, the maximum of ρ and E_B is obtained, with values of 8×10^{15} Ω cm and > 4 MV cm^{-1}, respectively. For a film thickness of 500 Å, this value of breakdown field means gate voltages greater than 20 V, which is high enough for the proper performance of any microelectronic device. Above 600 °C, the insulator electrical properties sharply deteriorate.

It is known that low temperature annealing in SiN$_x$:H promotes a decrease of dangling bonds density [11, 17] and a thermal relaxation and a reconstruction of the lattice, both in the bulk and at the insulator–semiconductor interface, as was shown on SiN$_x$:H/n-InP capacitors (figure 3), and on SiN$_x$:H/n- Si [18] devices. For temperatures above 600 °C, the thermal stress on the structure is high enough so that insulator and the interface properties degrade rapidly.

4. Conclusions

We have shown that Al/SiN_x:H/n-$In_{0.53}Ga_{0.47}As$ structures with excellent interface and bulk properties could be obtained by low-temperature ECR-CVD technique, avoiding the deposition of Si interface control layers or surface passivation methods. A simple cleaning step prior to the insulator deposition, and a post-deposition rapid thermal annealing process at 600 °C for 30 s are just enough to achieve n-$In_{0.53}Ga_{0.47}As$ capacitors with small frequency dispersion and hysteresis, a minimum interface trap density of 3.5×10^{11} eV^{-1} cm^{-2}, with high resistivity (8×10^{15} Ω cm) and electrical breakdown field (4 MV cm).

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