

Design of a variable width pulse generator feasible for manual or automatic control[☆]

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Abstract

A variable width pulse generator featuring more than 4-V peak amplitude and less than 10-ns FWHM is described. In this design the width of the pulses is controlled by means of the control signal slope. Thus, a variable transition time control circuit (TTCC) is also developed, based on the charge and discharge of a capacitor by means of two tunable current sources. Additionally, it is possible to activate/deactivate the pulses when required, therefore allowing the creation of any desired pulse pattern. Furthermore, the implementation presented here can be electronically controlled. In conclusion, due to its versatility, compactness and low cost it can be used in a wide variety of applications.

Keywords: pulse generation, signal on transition, variable width

1. Introduction

Compact pulse generators in the ns and sub-ns range have a number of applications in scientific research. They are required in both laboratory and field tests, and sometimes size and low cost demands make commercially available instruments unsuitable to cover these needs. This may happen for instance when building up a complex instrument, where signal processing boards need to integrate pulse injection subsystems for diagnosis. In some other applications it is necessary to provide multichannel signals, and pulse division or amplification significantly degrade signal integrity when the widths are in the range of nanoseconds or below. One example application was the construction of Cherenkov telescopes for MAGIC [1] and CTA [2] experiments, which are cornerstone instruments for Astroparticle Physics research. Based on the pioneer work of one of the recipients of 1958 Nobel prize on physics, these instruments take benefit of the radiation emitted by particles traveling faster than light in the atmosphere [3]. Since the duration of the Cherenkov light is on the order of a few nanoseconds, compact pulse generators were soon needed in the experiment for performing both laboratory and field tests in several parts of the telescope, such as the photodetector signal acquisition chain or the camera calibration subsystem [4].

In previous work we proposed prototypes of compact, fixed pulse width generators in the nanosecond range, such as the one described in [5], which was based on a scintillator, or the one presented in [6], based on step recovery diodes. Interesting papers devoted to high-bandwidth compact pulse generators can be found in scientific journals. It is worth to mention the picosecond-range pulse generator of Lee and Nguyen [7], the design of Ziegler et al. based on FPGA with 64 channels [8], or the prototype presented by Sanchez et al. in [9], which features the possibility of modifying the pulse width. Gil et al. presents in [10] a pulse generator for the HADES experiment able to provide random patterns, and Zhu and Wang published another one in [11] based on FPGAs. Other designs devoted to driving LEDs can be found in [12] and [13]. A good review of picosecond pulse generator topologies based on transistors and avalanche diodes can be found in [14]. Pulse generators based on solitons propagated through

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nonlinear transmission lines (NLTLs) have been the subject of fascinating and extensive research [15, 16, 17]. NLTLs exhibit difficulties in impedance matching and rising/fall end control, but have been very successful for the development of comb generators [18, 19]. Rise and fall times of few picoseconds can be obtained with special differential amplifiers fabricated with InP Heterojunction Bipolar Transistor technologies [20].

The pulse generator we present in this work offers the possibility of electronically tuning the pulse width with independent control of the rise and fall times. This feature multiplies the potential to develop fast quality control and calibration protocols. The design is compact, has a low cost and is easy to manufacture. We have obtained pulses with widths of 10 ns and amplitudes in excess of 4 V without using integrated ASIC technologies. With the guidelines described here the design can also be implemented in a single chip but at the expense of a significant cost increase for a single unit. Given the fact that our major limitations in this design come from layout and interconnection parasitics, it is expected to achieve narrower pulses with an ASIC version of the core of the pulse generator. In this paper we describe in detail the schematics, the pulses we have obtained and the key specifications.

2. Pulse generator design

The overall structure of the pulse generator is shown in Figure 1. The design has been divided into several blocks, which have been implemented in different subcircuits. Thanks to the modularity of the design, each block has been designed, implemented and tested separately, though the integration in one single circuit is straightforward. High speed PCB layout techniques should be employed in the implementation of the circuits in order to preserve the signal integrity throughout the entire system.

The main stage is the Signal On Transition (SOT) Pulse Generator. This circuit is the responsible of the variable width, ns-range pulse generation. The main feature of the SOT is the ability to select the pulse width by means of an external control voltage, which usually consists in a low frequency pulse generator. A matching stage is also necessary in order to adapt the raw pulse to the required output characteristics (voltage levels, load effects, high current, 50- Ω impedance).

The Transition Time Control Circuit (TTCC) produces the control signals that determine the output pulse characteristics.

As the system is biased by means of current sources, the construction of the bias generation stage will be discussed in section 2.2.

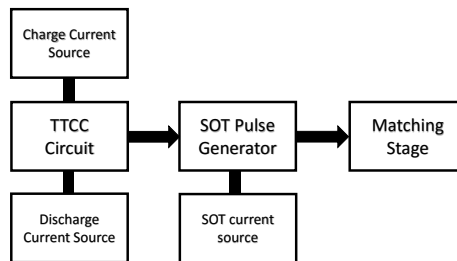


Figure 1: Block diagram of the SOT pulser full system

2.1. Signal On Transition (SOT) pulse generator

The pulse generator schematic is shown in Figure 2(a). It is composed of a current source, a resistor and four N-channel enhancement transistors. Two reference voltages (V_1 and V_2) and one control signal ($V_{CONTROL}$) are needed to control the conduction and cut-off state of the transistors, which determine the path of the current. The

signal used as $V_{CONTROL}$ is a low-bandwidth pulse generator. When there is a transition from low to high in this control signal (or vice versa), around the middle point of the transition, the current is driven through the resistor and the voltage drop across it produces the output pulse. For that reason this circuit has been named Signal On Transition Pulse Generator. This design is based on the Patents US 6433720 [21] and US 6642878 [22].

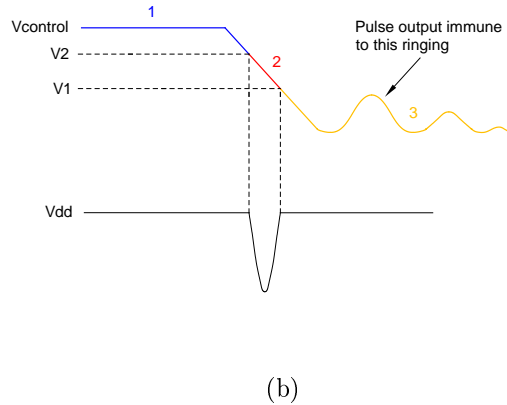
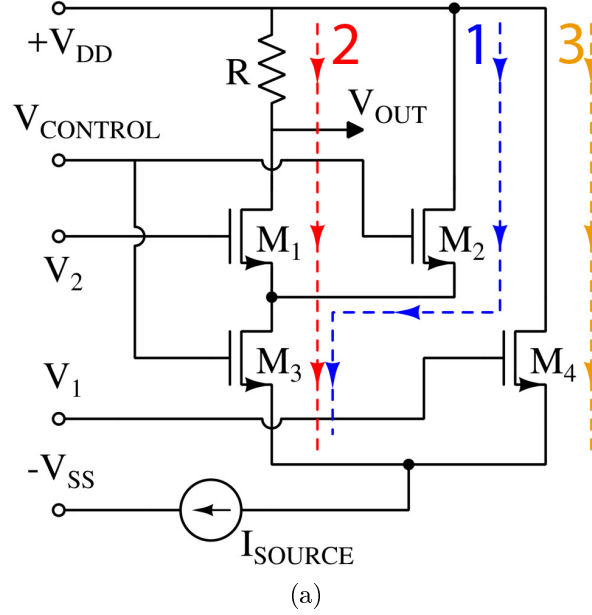


Figure 2: (a) SOT pulser schematic. (b) Output signal.

58

Initially $V_{CONTROL}$ is at a high level with a value higher than V_2 , so transistors M2 and M3 are ON, while M1 and M4 are OFF (marked as path 1 in Figure 2). When $V_{CONTROL}$ decreases to a value between V_2 and V_1 , transistor M1 changes to conduction state and M2 to cut-off (path 2 in Figure 2). Finally, $V_{CONTROL}$ decreases below V_1 and consequently transistor M4 enters into conduction while M1 and M3 change to off state (path 3 in Figure 2). While $V_{CONTROL}$ is between the reference voltages V_1 and V_2 , the current passes through the resistance R. Therefore, a negative pulse is generated at the output of the circuit (i.e., at the drain terminal of transistor M1). This pulse is base-lined at the voltage V_{DD} . Similarly, a second pulse is created in the low-high transition of the control signal. As will be discussed later, these pulses created on the leading and trailing edges of $V_{CONTROL}$ can have different widths depending on the rise and fall times of the control signal. It is possible to turn off the current

67

source during one of these edges to obtain only one pulse, if desired. A significant characteristic of the SOT pulser is its high immunity to the ringing of the control signal, as the pulse is produced only in the central part of the transition and therefore it is not affected by the very common signal distortion produced at the start and end of the edges, as can be seen in Figure 2(b). As the pulse width corresponding to the time $V_{CONTROL}$ is between V_1 and V_2 , it can be controlled by two means: increasing the difference between V_1 and V_2 , or changing the slew rate of the control signal. The first approach implies a smaller range of variation, as if the reference voltages are too similar or too different the transistors could be biased into a non-desirable operation point. Consequently the second approach is developed, i.e. voltages V_1 and V_2 are fixed and the rise and fall time of $V_{CONTROL}$ are variable. In order to perform a preliminary analysis of the circuit behavior, an implementation with discrete components has been produced and tested. Nevertheless, an integrated circuit implementation is straightforward and recommendable, as the design only contains resistors and four identical transistors.

2.2. Bias stage

One of the guidelines in the design has been the use of as few components as possible in order to avoid complexity and to decrease the cost. There are several ways to implement current sources, which can be looked up in the literature, and we finally decided to use a quite simple topology, shown in Figure 3(a), instead of other more complex designs with operational amplifiers (op amps), cascode output transistors, etc. R1 is used to limit the maximum current through the JFET. Due to the variations in the value of the drain-source saturation current and pinch-off voltages (I_{DSS} , V_P) between transistors [23], a variable resistor has been chosen, so it is possible to calibrate the current source to the maximum current desired. Once R1 has been fixed, the value of the current source is changed by means of R2. The design based in JFET has several advantages: Only two or three devices are necessary, with simple connections. Also, the current source can be used as a floating device and, unlike other topologies, it is not necessary to connect one of the outputs to the power supplies. Negative feedback makes it stable for temperature or bias voltage drifts. Feedback also increases the output impedance.

The current source works only if $|V_{AB}| > |V_P|$. In our design, we chose the J107 JFET transistor with nominal values of $V_P = -2.9$ V and $I_{DSS} = 100$ mA. Resistors between 40 and 550 Ω yield output current values of 34 and 4 mA with equivalent output resistances of 2.7 and 77 k Ω . These values seem too low to be acceptable for current sources but we could observe in lab tests that the design performed well despite this non-ideality.

Similar current sources will be used in other stages as it will be shown in next sections. Finally, the addition of a low-resistance analog switch in series with the current source allows turning it off if necessary.

The system has been designed to work with a single external +12 V power supply. With typical LM117 voltage regulators, able to provide more than 1 A, all the required positive voltages can be obtained (+2.5 V, +6 V and +7.5 V). Positive reference voltages, which do not require to provide high currents as they are used to bias transistor gates, are obtained just with high resistance partititors.

Negative reference voltages will be obtained from the accurate +6 V reference voltage with potentiometers and common operational amplifiers in inverter configuration. It is evident that these op amps, and other parts of the system to be depicted in next sections, require negative power supplies. In particular, the system requires three negative power supplies, (-2.5 V, -6 V and -12 V) that can be obtained using the corresponding positive values as inputs of a TC962 DC-DC converter (Figure 3(b)). The model TC962 from Microchip [24] has been selected due to its high output current (80 mA) and its wide operation range (+3 V to +18 V). Additionally, it has a power conversion efficiency of 97% and voltage conversion efficiency of 99.9%. The configuration shown in Figure 3(b) allows obtaining a negative bias voltage of $-V_{CC}$ from an original positive voltage $+V_{CC}$.

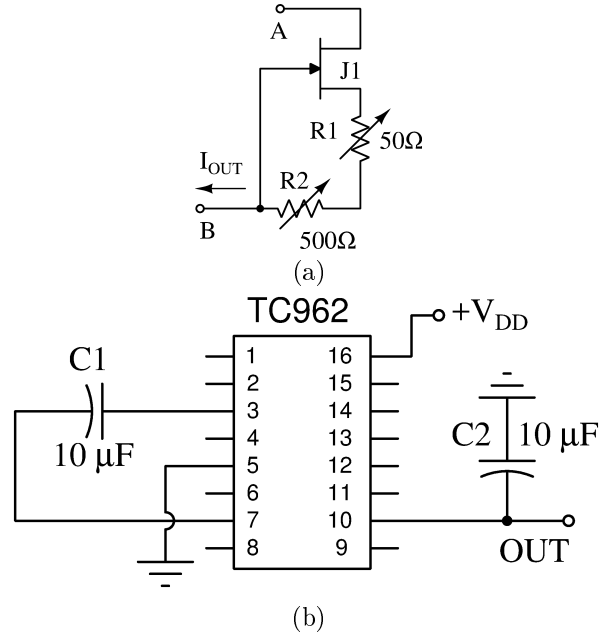


Figure 3: Variable current source circuit (a) and negative voltage source (b)

2.3. Matching stage

The purpose of this circuit is multiple, and it must fulfill the following requirements: 1) It must invert the output pulse and filter the DC signal, in order to be referenced to ground level and to have a positive amplitude. 2) The input impedance must be high in order to avoid input currents. 3) The output impedance must be low in order to be matched to a 50-Ω load. 4) The output current must be high to connect it to a low impedance load providing a high amplitude pulse output. 5) Finally, this stage must feature a high bandwidth as the pulses are in the range of a few nanoseconds. All these requirements are fundamental in order to achieve high amplitude pulses free of distortion.

After considering several options, a solution based on instrumentation amplifiers was chosen for that purpose [25, 26], configured for getting an overall unity gain since no signal amplification is needed. Figure 4 shows the matching stage connected at the output of the SOT pulse generator.

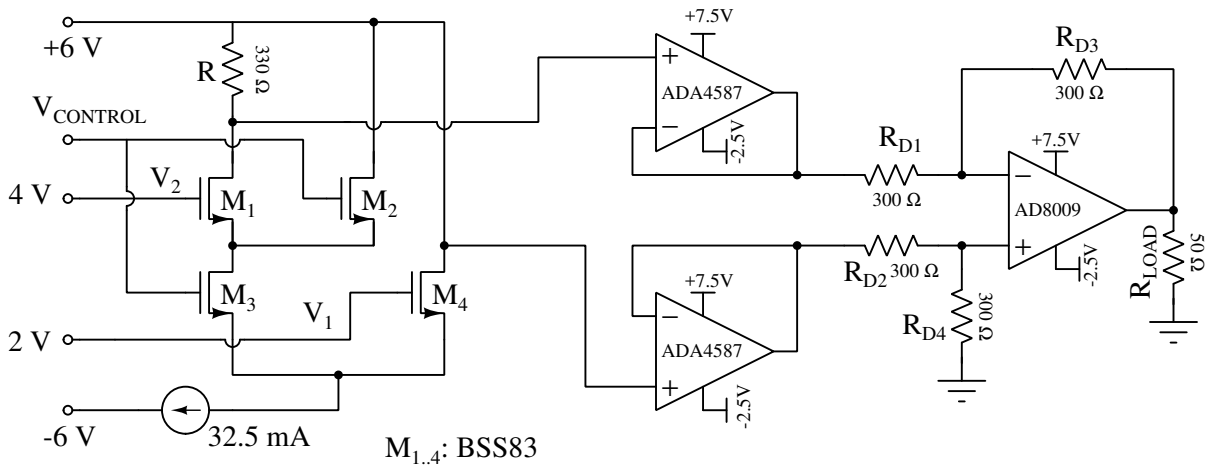


Figure 4: SOT pulse generator plus matching stage schematic. All supply capacitors are omitted.

The structure is based in the widely-known classic 3-opamps instrumentation amplifiers with several modifica-

tions. Unfortunately, to the authors' knowledge there is not any integrated instrumentation amplifier fulfilling the five assumptions listed in the previous paragraph so it was built with discrete operational amplifiers. Two high-speed operational amplifiers were selected to build the input stage, namely ADA4857 from Analog Devices [27]. This is an ultralow distortion, low-noise and high-speed op amp that features an input impedance of several $M\Omega$, a bandwidth of 750 MHz and a slew rate of 2800 V/ μ s. As it can only provide 50 mA of output current, another model must be selected for the difference operational amplifier in the output stage. We employed the very high speed amplifier AD8009 from Analog Devices [28]. It provides a bandwidth of 1 GHz, a slew rate of 5500 V/ μ s and an output current of 175 mA. It is extremely relevant to indicate that, unlike the two first op amps, this component is a less common current-feedback operational amplifier. This is the reason of using low values of resistance (300Ω , 1%), necessary to correctly feedback this component.

2.4. Transition Time Control Circuit (TTCC)

The purpose of the TTCC is to provide the SOT pulser with a control signal whose rise and fall times can be set at will. A longer rise or fall time results in wider pulses at the output, and vice versa. The circuit is based on the charge and discharge of a capacitor by means of two current sources (I_{CHARGE} , $I_{DISCHARGE}$) [29, 30]. Thus, rise and fall times are independently controlled. The constant current guarantees a linear rate of change of the voltage across the capacitor, $\frac{dV}{dt} = \frac{I}{C}$. Transition times are therefore dependent on the values of the capacitor and the current. The capacitor will be fixed to a constant value but the current will be variable, so modifying the value of the current source will change the slope of the output pulse. A four transistor design (Figure 5) has been implemented in order to keep both current sources always active, so faster transition times and a better performance can be achieved. During the rising edge the transistors M2 and M3 are on (path 1, red, in Figure 5). The transistor M2 allows the current coming from the top current source to charge the output capacitor. Transistor M3 creates a path to ground for the discharge current source in order to keep it active. Contrarily, during the falling edge transistors M1 and M4 are on (path 2, blue, in Figure 5).

carefully selected to match with the input and output voltages required: NMOS (BSS83) for transistor M1, PMOS (BSS84) for transistor M2, PMOS depletion for transistor M3 and NMOS (BSS83) for transistor M4. Unfortunately we could not find a P-channel depletion MOSFET in the market, but as JFET transistors are also compatible with this design [31], a JFET J175 is used. The final schematic is shown in Figure 6.

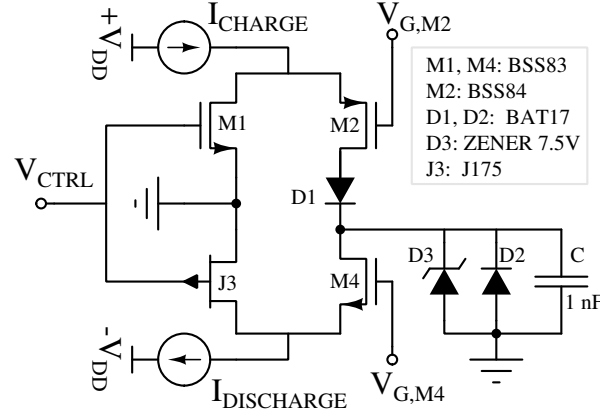


Figure 6: Schematic of the variable rise and fall time pulse generator

Transistors M1 and J3 sources are grounded, so they are directly controlled by the control signal on their gates. At the gates of the other transistors a constant voltage is applied, whose value is determined by the voltage drop in its mirror transistor when it drives the maximum current to be used. Additionally, the maximum limit of the current is set by the maximum one allowed in the linear region. Higher currents are not recommended since in the saturation region small changes on the current involve large voltage drops across the transistor. In the case of transistor M4 we obtain that the voltage drop across J3 when it is on ($V_{GS} = 0$ V) is about +3.2 V for a value of the current source of 30 mA (limit between linear and saturation regions). A value of -4 V has been then chosen for biasing the gate terminal of transistor M4. In the case of transistor M2, the drain to source voltage of transistor M1, V_{DS} (M1) for a current of 30 mA and a gate to source voltage V_{GS} (M1) of +5 V is inferior to +1 V. Therefore the gate voltage of transistor M2 is fixed to +1 V. The maximum value of the charge current source (i.e. the one that controls the rise time) is also limited to 30 mA for symmetry. Nevertheless, according to the I-V characteristic curve of transistor BSS83 higher values may be used if desired. Thus, the behavior of the bottom part of the circuit is the following: when the control signal is at low level (0 V), J3 is ON (V_{GS} (J3)=0 V). On the other hand, the highest drain to source voltage of transistor J3 is reached when the value of the current is maximum, which corresponds to +3.2 V at 30 mA as discussed above. Consequently transistor M4 is OFF for the entire current source range since $V_{GS}(M4) \leq -4\text{ V} - (-3.2\text{ V}) = -0.8\text{ V}$. When the control signal changes to high level (+5 V), transistor J3 goes immediately into cutoff. The voltage in the terminal source of transistor M4 (i.e. the top of the discharge current source) starts to increase negatively trying to keep the current level constant. When the Thevenin voltage is reached, transistor M4 is turned on. The analysis of the upper part of the circuit is similar to that of the bottom part, with just one exception. A diode is added between the drain of transistor M2 and the output capacitor to prevent the inverse biasing of transistor M2 that could otherwise take place in the transitions of M2 from conduction (capacitor output voltage at +5 V) to cutoff.

3. Simulations

3.1. SOT

A simulation of the SOT circuit has been performed using Orcad PSpice. The dependence of the output pulse on several parameters is studied. These parameters are: 1) current provided by the source, 2) value of the resistance

182 R on which the pulse is produced, 3) gate voltage on the transistor M1, 4) rise and fall time of the control signal.
 183 Figure 7 shows the results of this simulation.

184 From the bottom graphic of Figure 7 it is deduced that the longer the rise time is (T_r), the wider the pulses
 185 are. The amplitude remains constant for all the values of the rise time. These conclusions are equally valid for the
 186 falling time. In the same way, the greater the voltage difference between V_1 and V_2 is, the wider the pulses are. In
 187 this case the amplitude is also increased.

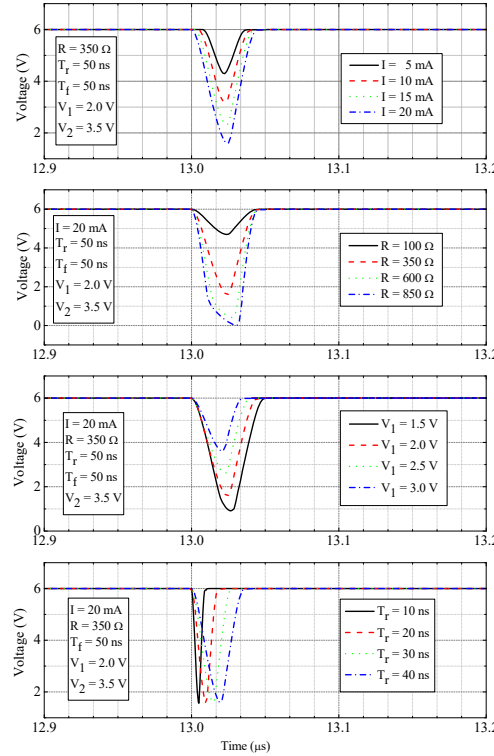


Figure 7: SOT pulse simulation obtained varying, from top to bottom: the current source value (I), resistance (R), M1 gate voltage V_1 and the rise time (T_r). The trigger signal took place at 13 μ s.

188 Higher values of the output resistance R yield in higher amplitude pulses. It can be noticed that there is a point
 189 from which the shape of the output pulse starts to be distorted and there is a loss of symmetry. This situation takes
 190 places when there is an excessive voltage drop across the resistor and the transistors are away from its operation
 191 point. For this reason the value of this resistor will be fixed to 330 Ω . Finally, the value of the current source
 192 has also a direct effect on the output pulse (top of Figure 7). Higher values of the current source will result in
 193 higher-amplitude, but also wider, pulses.

194 4. Results

195 4.1. SOT

196 In order to measure the output of the pulse generator, a DC-block is used to avoid the flow of direct current
 197 towards the oscilloscope, what would cause an improper output. Broadband performance and matching to the 50
 198 Ω input impedance of the oscilloscope are critical issues in order to minimize the pulse distortion and ringing. The
 199 selected model is a coaxial DC-block BLK-89+ from Mini-Circuits [32], which features a wide band from 0.1 MHz to

8 GHz and a low insertion loss. The parameters of the SOT pulse generator have been fixed as follows: $R = 330 \Omega$, $V_{DD} = +6 \text{ V}$, $V_1 = +2 \text{ V}$ and $V_2 = +4 \text{ V}$. The current source provides 32.5 mA and the control voltage consists in a periodic pulse of 400 ns, with low and high values of 0 and +7.5 V respectively. This signal is provided by a Tektronix AFG3252 waveform generator. The high level of the control voltage has been chosen several volts greater than V_2 in order to guarantee the correct turn off of the transistor M1 when the voltage control level is at high state. The measurements have been taken for various values of the leading and falling edge times (Figure 8) with the oscilloscope Agilent Infiniium DSO81204B (12 GHz, 40 GSa/s).

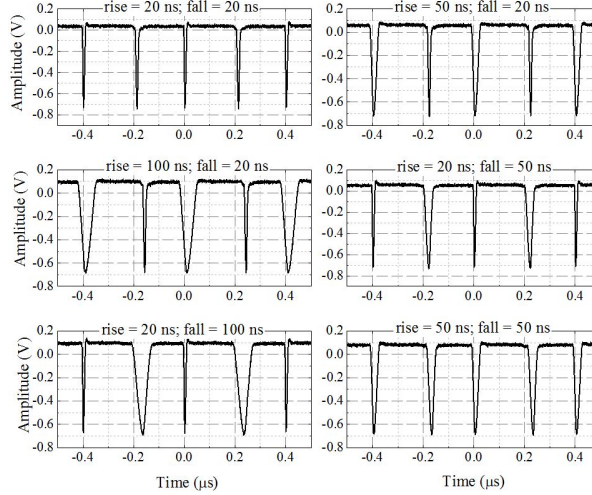


Figure 8: Measured output of the SOT pulse generator stage.

The dependence of the pulse width on transition times is observed in the Figure 8. Thus, for values of 20, 50 and 100 ns the obtained widths are 7.1, 19.4 and 38.5 ns, respectively. These pulses occur in both the rise and fall transitions. Consequently, it is possible to achieve alternated pulses with different widths. As previously remarked, the SOT generator output are inverted pulses base-lined at the voltage V_{DD} . If a unique pulse is required, it is enough to switch on and off the current source when necessary. In the same way, it is possible to control the time the pulses appear by just controlling the operation of the current source. From Figure 8 can be remarked that the amplitude of the pulses is lower than what we expected from simulations (Figure 7). This is due to the 50Ω input impedance of the oscilloscope, as the SOT output pulse requires a high impedance load.

With this circuit pulse widths down to 1.4 ns for transition times of 5 ns have been achieved, but the pulse is distorted and loses amplitude. Below 5 ns the pulse has lost almost all its amplitude and shape. To obtain much narrower, free of distortion pulses it is necessary to implement this design in an ASIC, in order to eliminate parasitic capacitances and inductances coming from the PCB traces and from discrete devices package. Finally, the jitter of the pulse width is measured for a pulse corresponding to the rise edge of the control voltage, with a transition time of 20 ns. The results show a jitter of 168 ps for a pulse width of 7.12 ns. This result is not as good as expected. This is probably due to the use of current sources based on JFETs, which can cause small fluctuations affecting to the SOT generator stability. The use very stable current sources will presumably improve considerably this value.

4.2. SOT + Matching stage

Figure 9 shows the output of the SOT generator and the matching stage. The control signal is the same that the one used to obtain the results of Figure 8. The three op amps have the same bias: $V_s^+ = +7.5 \text{ V}$, $V_s^- = -2.5 \text{ V}$. These values are several volts in excess of the maximum and minimum voltages of the intended final pulse, respectively, in order to adequate the pulse to the input and output voltage ranges of the op amps [33].

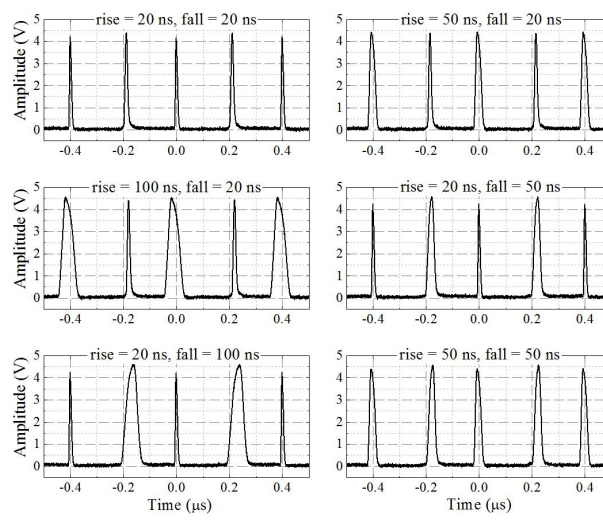


Figure 9: SOT output pulse with the matching stage. Measurements carried out for several values of the transition times.

Pulses in excess of 4 V have been obtained. Pulse widths of 8.5, 22.9 and 45.0 ns have been measured for transition times of 20, 50 and 50 ns, respectively and for both the rise and fall edges. As expected, the matching stage practically has no influence in the pulse width, neither in the pulse amplitude as a unity gain has been implemented. For higher pulse amplitudes, higher gains can be selected. For a transition time of 20 ns in the rise edge of the control signal, pulse width of 8.47 ns with 149 ps jitter is obtained, which is very similar to the results obtained without the matching stage.

4.3. TTCC

Figure 10 shows the final schematic of the implemented circuit. A low-bandwidth pulse generator based on a Smith trigger inverter has been used as control signal. The load connected to the output of the TTCC circuit must feature high impedance, otherwise the output capacitor of the TTCC circuit will be discharged through the load path resulting in an improper working. Thus an oscilloscope with the possibility of selecting an input impedance of 1 M Ω has been used for taken measurements. The value of the output capacitor must be large enough to not be affected by the input capacitance C_{iss} of the SOT generator MOSFET transistors. A value of 1 nF has been chosen so it is almost not influenced by the 3 pF input capacitance of the two BSS83 transistors (1.5 pF each). Nevertheless, there is a significant trade off since the smaller the value of the output capacitor is, the faster the transition times are achieved.

Figure 11 shows the working of the TTCC circuit for various values of the sourced current. Transition times from 250 ns to 1.8 μ s have been achieved for both rise and fall edges. As previously discussed, faster transition times can be obtained by decreasing the value of the output capacitor. All measurements were performed with the oscilloscope Tektronix TDS3052 (500 MHz, 5 GS/s).

4.4. SOT + matching stage + TTCC

Finally, the SOT pulse generator plus the adaptation stage when controlled with the TTCC circuit has been measured. A block diagram of the full system is shown in Figure 1.

As previously remarked, some aspects have to be taken into account. First, the load connected to the output of the TTCC must present high impedance, this is accomplished by the MOSFET gate impedance of the SOT pulse generator. Second, the input capacitance of the SOT transistors can affect the result as its capacitance is added to the value of the TTCC output capacitor, causing slower transition times. Finally, an adaptation stage is

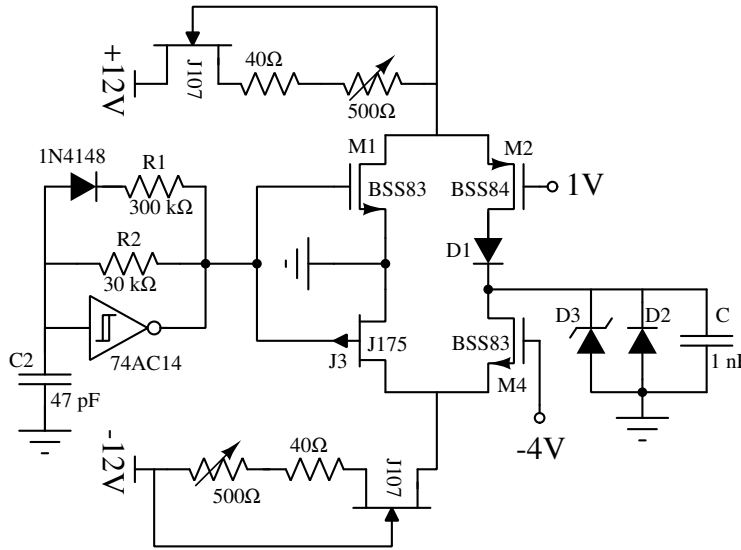


Figure 10: TTCC circuit schematic

necessary in order to connect the high impedance required by the SOT pulser to a low impedance load. The results are presented in Figure 12. Pulse widths of 355, 180 and 115 ns have been achieved for charging / discharging currents of 10, 20 and 30 mA, respectively. All the measurements were taken with the oscilloscope Agilent Infiniium DSO81204B (12 GHz, 40 GSa/s). It must be pointed out that these pulses could have been measured with scopes of lower bandwidths and lower sampling speeds than those featured by the one used here, but with the risk of missing information about possible parasitic ringings.

These results show the proper behavior when the SOT pulse generator is controlled by the variable transition time circuit. Furthermore, the design presented here is viable for remotely controlling both the generation and the width of the pulses. The former is achieved by adding the circuitry necessary for enabling and disabling the SOT current source, so the pulses are generated when desired. It could be performed, for example, with a transistor which turns on and off the current source. The control of the pulses width can be implemented by replacing the analog potentiometers of the variable transition time circuit with digital ones. Thus, controlling both of them it is possible to create any pulse pattern. In conclusion, this possibility of electronic control opens a new range of applications in automation processes.

5. Conclusions

A ns-range pulse generation featuring electronic control of pulse width has been developed, named Signal On Transition (SOT) pulser. In the design the pulse width is simply controlled by means of the control signal slope, so the same PCB can provide a large range of widths which will depend on the degree of slope variability. This feature grants high versatility to the pulse generator. Additionally, a matching stage was developed, composed of three high speed and low distortion OPAMPs. Pulses of more than +4 V amplitude and less than 10 ns FWHM have been achieved with the SOT pulser. The implementation carried out has been with discrete components and it is expected to reduce to a great extent the value of the minimum pulse wide achievable in an integrated circuit design.

In the SOT circuit, the maximum pulse repetition frequency achievable is just limited by the commutation of the transistors and not by other physical constraints, as for example the charge and discharge times required in SRD generators. On the other hand, since the pulse is created during the middle of the control signal transition, it is not affected by any ringing occurring at the beginnings and ends of the control signal edges. Additionally, the design is

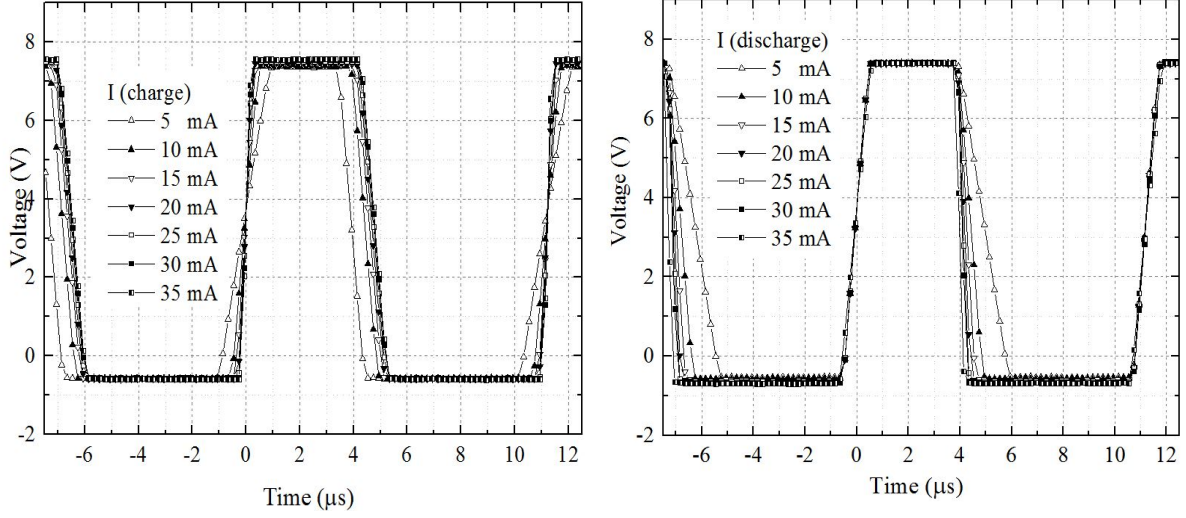


Figure 11: Left: leading edge transition time. $I_{\text{discharge}} = 10$ mA, $I_{\text{charge}} = 5$ to 35 mA, and right: falling edge transition time. $I_{\text{charge}} = 10$ mA, $I_{\text{discharge}} = 5$ to 35 mA.

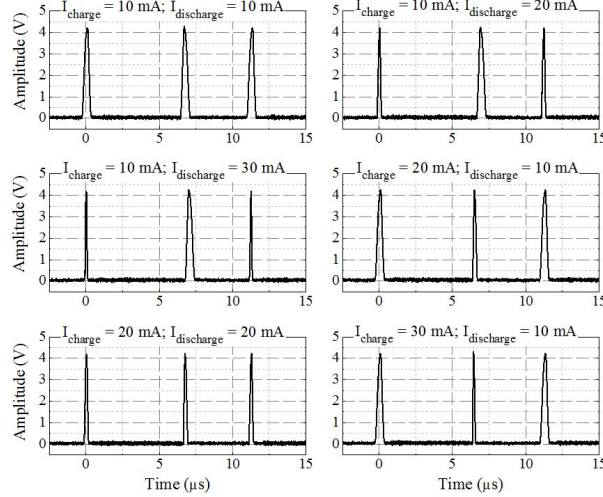


Figure 12: Full system output.

highly appropriated for an integrated circuit implementation, since it is essentially composed by transistors. The pulse generation is controllable by activating/deactivating the SOT current source, being able to produce pulses just when required, allowing to create custom pulse patterns. The combination of this property and previous one make this generator ideal for being used in applications where high repetition frequency rates and discontinuous pulse generation are required.

Finally, a variable transition time circuit (TTCC) has been designed for controlling the width of the pulses. This circuit is based on the charge and discharge of a capacitor by means of two variable current sources. A four transistor design has been developed for keeping the current sources always active and achieving faster slopes. The transition time range can be adjusted by modifying the value of the capacitor. On the other hand, rising and falling times are independently controlled by just changing the value of the current sources. In the design presented here it is performed by means of a potentiometer, thus using a digital one is possible to control the pulse width by means of a computer or a remote control system.

In conclusion, we demonstrated the great potential of the SOT pulse generator, and its versatility when combined with a variable transition time generator for leading to a variable pulse width generator. Additionally, as it can be

remotely controlled, the generator is suitable for automation applications.

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