Multiple Cell Upsets in the Configuration RAM of a 7-nm FinFET SoC under Heavy Ions

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Abstract

This manuscript investigates the heavy ion effects on the novel 7-nm FinFET AMD (formerly, Xilinx) Versal SoC, namely on the configuration memory of the embedded FPGA. The experiment consisted in loading a program in a delidded device, irradiating in static mode and reading back the content. Several species and configurations were used to test the device. First of all, it was tested the efficiency of the XilSEM tool, provided by the manufacturer to fix erroneous bits. Second, this tool was disabled to find out the cross sections of the single event upsets of different multiplicities. Flipped upsets were classified using statistical techniques to reconstruct the multiple cell upsets. No multiple bit upset occurred and only 4-bit multiple cell upsets were observed in the worst cases, although it is clear that the cross section of the 2-bit multiple cell upsets is comparable to that of single bit upsets. Later, a strategy to carry out fault injection campaigns is proposed taking into account the knowledge acquired after the radiation tests, and the expected error rates in actual space environments is studied.

Index Terms

FinFET, FPGA, heavy ions, single event effects

I. Introduction

SYSTEMS-ON-CHIP (SoCs) and Field Programmable Gate Arrays (FPGAs) are widely used in space applications. AMD Versal is one of the most advanced SoC manufactured on a FinFET TSMC 7-nm technology offering various versions [1] with dedicated Intellectual Properties (IPs) for Artificial Intelligence or Radio Frequency applications that are essential on space communication systems.

Characterization of complex Integrated Circuits (ICs) containing memory cells is fundamental for taking into account the suitable mitigation techniques to guarantee the reliability and feasibility of the systems on all the stages of a space mission, including the launcher, earth rising orbit phase and Single Event Effects during the complete lifetime of the mission.

The promising features of the AMD Versal have drawn the attention of the space community [2]. Two papers by H. Quinn *et al.* [3], [4] investigated its behavior under neutrons. In 2022, Chen et al. [5] showed how efficient the dedicated IP for the Soft Error Mitigation by Xilinx (XilSEM) was to mitigate single event upsets induced by 64-MeV protons as well as the proportion of multiple cell upsets (MCUs). Another paper [6] showed the different values of cross sections for the configuration, block and ultra RAMs for protons and neutrons, and helped to estimate the soft error rates at ground level due to atmospheric neutrons. Latch-up has also been a big concern, so some works have addressed this issue. For example, previous papers usually report not having observed such phenomenon, even at high temperature (~120 ^{o}C) [7]. Finally, latch-up under heavy ions was ruled out on [8] setting an upper threshold value about 10^{-7} cm^2/device with 69 MeV·cm^2/mg ions, with the exception of easily removable soft micro latchups. It is important to remark that not all the papers have tested exactly the same model of the Versal.

II. Test setup

A. Electronic set-up

On this test, the setup is based on the AMD evaluation board VCK190 [9], which contains a Versal AI Cores VC1902 device. Readback operations were performed by JTAG through the USB-C on the VCK190 with Vivado 2020.2 hardware manager [10], saving so the content of the whole configuration memory. The baseline of the test was to compare a readback of the configuration RAM (CRAM) after the irradiation against the golden file before the test. Hence, these experiments can be classified as static [11]. Bias voltage was not controllable and were imposed by the development kit design, being set between 1.1 V and 3.3 V depending on the bank.

It is important to notice that on this setup design for the test was based on the Versal Control Interfaces and Processing System (CIPS) so no additional programmable logic (PL) neither processing system (PS) at application level were implemented for the test. XilSEM, which is the IP dedicated for error mitigation on Versal devices that can be activated by the CIPS IP was also tested on this heavy ions campaign.

This activity has received funding from the European Union's 2020 research and innovation programme under grant agreement No 101008126 (RADNEXT) [48]. Dr. Franco's collaboration was funded by the Spanish MICIINN project PID2020-112916GB-I00.

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TABLE I
NUMBER OF BITFLIPS OBTAINED UNDER HEAVY IONS TESTS.
^{129}XE WAS USED AT TAMU, THE REST AT RADEF.

XilSEM	Ion	LET @0μm	LET @105μm	Fluence	Bitflips
OFF	^{20}Ne	2.3	2.8	2	14
	^{40}Ar	7.2	8.8	9	1166
	^{57}Fe	13.3	18.1	21.5	6775
	^{83}Kr	24.5	32.1	5.5	3761
	^{129}Xe*	41.8	54.3	14.8	9789
	^{126}Xe	48.5	62.4	3	3739
ON	^{40}Ar	7.2	8.8	1.5	0
	^{57}Fe	13.3	18.1	1.5	0
	^{83}Kr	24.5	32.1	1	0
	^{126}Xe	48.5	62.4	2	0
		MeV·cm^2/mg		$\times10^5$#/cm^2	

The size of the binary readback files was 59,842,000 bits (L_N). The manufacturer does not provide information about the internal organization of the configuration memory in the official documentation. However, the handbook for using libraries such as XilSEM [12] as well as the related open-source code [13] explain that the configuration memory is organized in frames of 25 128-bit quad words (4×32).

Besides, the golden file written in the FPGA was formed almost exclusively with 0's (only 1129 cells contained 1's). Hence, it was expected that most flipped bits would undergo the switch from 0 to 1.

B. Irradiation set-up

The device was irradiated in two different campaigns. The main irradiation campaign took place at the Radiation Effects Facility (RADEF) of the University of Jyväskylä [14] with the 16.3 MeV/u heavy ion cocktail produced by the JYFL K-130 cyclotron. This allowed getting five different values of Linear Energy Transfer (LET), shown in Section III. Devices were irradiated at room temperature and with an incidence angle of 0^o. Finally, Fig. 1 shows a picture of the device ready to be irradiated at this facility.

Another campaign took place at the Texas A&M University (TAMU) Radiation Effects facility [15], with with 25 MeV/amu Xenon, providing an additional value of LET, marked with a star in Table I.

In both campaigns the configuration memory was read and written while the beams were off. Therefore, errors attributed to single event transients (SET) or Single Event Functional Interrupts (SEFIs) are minimized.

The thinning of the sample for the test was performed by Thales SIX laboratories. The VC1902 device is offered with the VIVA1596 package, a member of the large family of ball grid array (BGA) packages (Fig. 2). The die is flipped to make contacts with the ball grid easier, so the topside package could be removed and the silicon thinned to 105 μm on the backside giving a suitable range for an effective Linear Energy Transfer up to 62.5 MeV·cm^2/mg. As they travel along the silicon bulk, the ions lose energy and in consequence their LET change. The original LET values at the silicon surface were modified by means of the University of Jyväskylä specific tool [16] to include the effect of crossing the silicon bulk. In the case of the irradiation at the TAMU facility the energy decay in air before reaching the exposed surface was also taken into account.

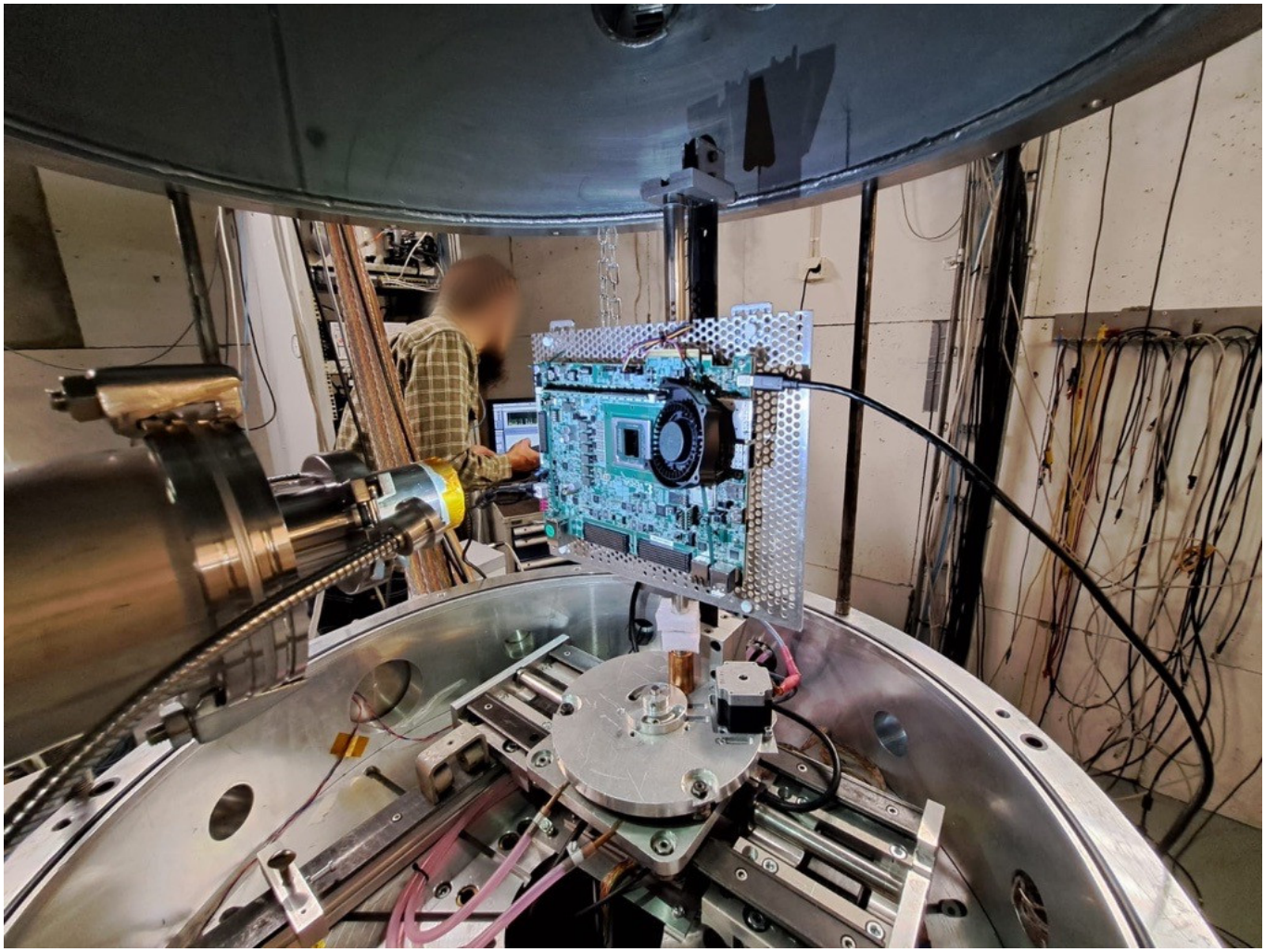
The internal temperature of the device was measured during the irradiation by means of the System Monitor (SYSMON), and it did not show sudden or large increases. In both facilities the uncertainty in particle fluence is bounded by ±10 % and it is included in the uncertainty margins of the graphs.

III. RESULTS

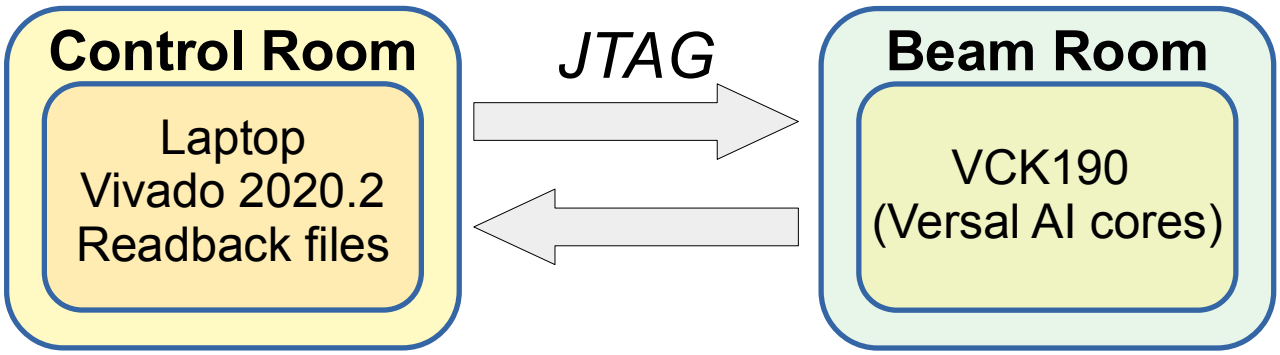
The irradiation campaigns were planned with a twofold goal: first, the verification of the efficiency of the XilSEM tool; second, the study of the single event effects in the device. Hence, in some rounds the XilSEM was on, while in others the XilSEM was disabled for some runs to gather data for further MCU analysis. Due to time constraints, the efficiency of the XilSEM tool was not tested in TAMU. Table I shows the characteristics of every species, the total fluence as well as the total number of observed bitflips. Further information about the rounds can be found on the report delivered to the RADNEXT project [17].

A. Efficiency of XilSEM

In some irradiation rounds, the XilSEM tool was enabled to test if it could remove the induced bitflips. The inspection of data shown in the second part of Table I, labeled in the first column as ON, allows discovering that no single event upset (SEU) of any multiplicity was observed in the device. The configuration files downloaded after every irradiation round were



(a)



(b)

Fig. 1. (a) AMD VCK190 evaluation board with Versal SoC AI Cores device assembled and opened for heavy ions test. (b) Schematic of system.

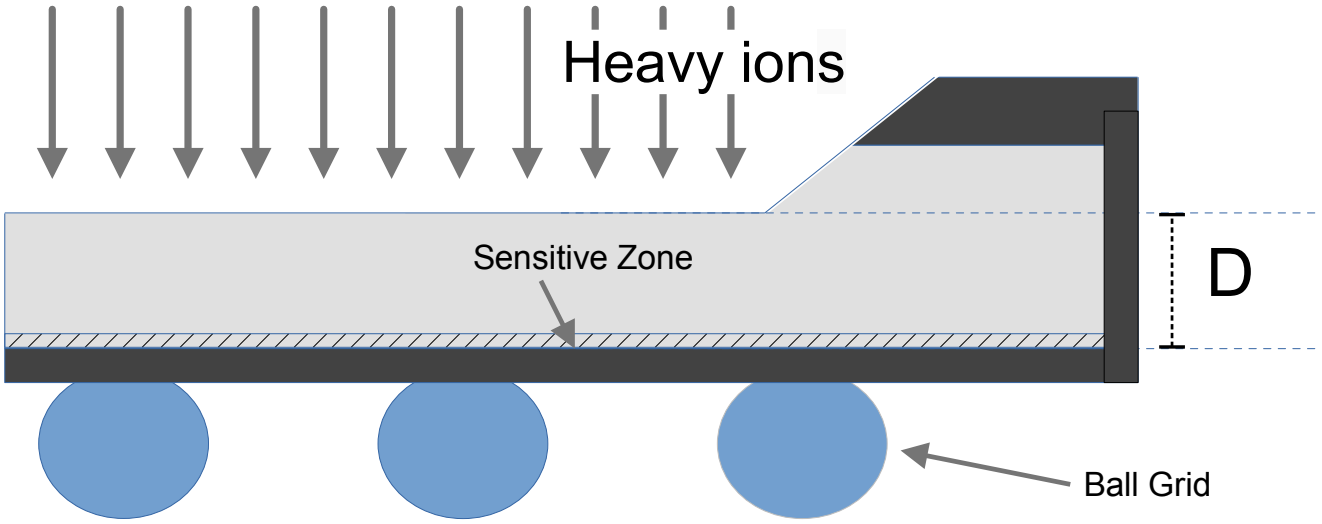


Fig. 2. Outline of the delidded device. As the chip is flipped for an easy access to the ball grid of the BGA package, the material on the top side could be removed and the silicon bulk removed. The die could be thinned down to $D = 105\ \mu m$.

identical to the golden one used as reference. This fact certifies the power of this technique to mitigate single events, at least in static tests.

It is interesting to provide upper bounds for the effective cross sections with enabled XilSEM. Assuming that the cross section for events of i-multiplicity at a known LET value, σ_i, the expected number of events would be $\mu_i = \sigma_i \cdot \phi \cdot N_B$, ϕ being the total fluence and N_B the memory size in bits. This value can be used as the central parameter of a Poisson distribution. The absence of observed events points out to a very low value of μ_i, such that

$$0 \ll r < \exp(\mu_i) < 1 \rightarrow \mu_i < -\ln r$$

since the probability of not occurring events in the Poisson distribution is $P(0) = \exp(-\mu_i)$. Hence:

$$\sigma_i < -\frac{\ln r}{\phi \cdot N_B}. \tag{1}$$

Using $r = 0.95$, as done in many fields of physics and engineering, one can deduce that the cross section is lower than $(4.3 \pm 0.4) \cdot 10^{-15}\ cm^2/bit$ for $LET = 62.4\ MeV \cdot cm^2/mg$. Uncertainty comes from that of the fluence value.

Finally, it is necessary to indicate that XilSem can provide real-time information about the number of corrected errors. However, this feature could not be used in the experiments, since the readback was done after the irradiation rounds, losing that information. As it will shown in the next section, several thousands of bitflips should have occurred at least in the ^{126}Xe rounds, but none of them was able to escape from XilSem correction.

B. Single event upsets with disabled XilSEM

After testing the efficiency of the XilSEM tool, the following irradiation rounds were devoted to know the characteristics of the single event upsets in the configuration memory of the device. As indicated, XilSEM could be disabled thus allowing full access to the configuration memory content including flipped bits. By comparing the downloaded raw file got after each radiation step with the pristine one and considering that the files are just streams of bits to which it is feasible to assign an index, it was possible to identify the positions of the flipped bit in that binary file. The range of accepted values for the indexes is from 1 to L_N. As expected given the initial content of the golden file, the vast majority of the flipped bits changed from 0 to 1.

Text files with the position of the flipped bits in each round were checked with the LELAPE toolbox [18], [19] looking for statistical anomalies pointing out to the existence of multiple cell upsets. This strategy has been adopted by several research groups in order to identify this phenomenon in spite of the fact of not having access to confidential information about the memory layout [20]–[29].

The analysis shows that there is a clear and unequivocal excess of pairs of flipped bits for which the indexes are separated 3200, 6400. 19199, 22399 and 47998 positions, fact that cannot be explained by random fluctuations. Values in this set can be calculated with simple arithmetical expressions using 3200 as initial seed (Table II). This value is exactly the size of frames, so one can deduce that this anomaly relates cells in the same position in adjacent frames. 6400, which is 3200 + 3200, links similar cells in frames with another one in between. The other three anomalies are more difficult to interpret. If frames are

supposed to be distributed along the Y-axis, 3200 & 6400 must be related to displacements along the X-axis and the rest along the other one, relating adjacent cells in the same frame or along diagonals, after applying some sort of scrambling & interleaving.

TABLE II
ANOMALIES EXPRESSED IN FUNCTION OF 3200.

Value	Expression	Value	Expression
3200	1×3200	19199	$6 \times 3200 - 1$
6400	2×3200	22399	$7 \times 3200 - 1$
		47998	$15 \times 3200 - 2$

Besides, another interesting fact is that, unlike other older FPGAs by the same manufacturer, there is no excess of flipped bits separated by very low values (1, 2, 3, ...). If so, these flipped bits would have occurred in the same word so pernicious multiple bit upsets did not occur. This fact backs up the previous supposition about use of interleaving by the manufacturer, as it occurs in other CMOS memories.

The statistical anomalies allows classifying the bulk of apparently unrelated bitflips into events of different size. All the positions of the flipped cells in every irradiation round were grouped in pairs and, for every possible pair, it was verified if the difference between positions was one of the possible values of Table II. If so, both cells were marked as members of the same multiple event. If a cell was related to two different cells, the events has at least 3-bit multiplicity, and this process is done until all the positions are classified. It is worth mentioning that most of the pairs of related flipped cells (around 85-90 %) are related by 3200, the rest of values being much less probable or even redundant. This analysis shows that there were multiple cell upsets with a size up to 4-bit, and this only occurring at the highest values of LET (Table III). This table also shows the expected number of false multiple 2- & 3-bit events due to the random occurrence of events of lower multiplicity in neighbor cells. These values were calculated using the expressions found in [30] for individual rounds and adding the partial values. The number of expected false events is two or three orders of magnitude below the observations.

Fig. 3 shows the single event cross sections for this device. Some details of interest are the following:

- The absence of dots for some sizes indicates that no event of this sort was observed. Gray zone on the bottom side shows the upper threshold for undetected events, calculated with Eq. 1.
- Error bars are calculated combining the uncertainty in the measurement, which was estimated as $2 \cdot \sqrt{N}$, N being the number of observed events for every LET and size, and the uncertainty in the fluence.
- The probability of observing false multiple events due to the accumulation of bitflips, calculated with the expressions in [30], is negligible.

The shape of the curves for SBU and MCUs strongly reminds of a typical Weibull function. However, fitting the set of data to this curve casts too weird values, since recent studies have observed a non-saturating behavior in FinFET technologies [31]. Therefore, it is necessary a visual inspection of Fig. 3 to gather some useful information.

First of all, the saturation cross section for both phenomena are quite similar. For example, the cross sections at 62.4 $MeV \cdot cm^2/mg$ is $(5.73 \pm 0.67) \cdot 10^{-11}\ cm^2$ for SBUs and $(5.97 \pm 0.70) \cdot 10^{-11}\ cm^2$ for 2-bit MCUs. In other words, SBUs and 2-bit MCUs are almost equiprobable for high values of LET, and seems that MCUs are more likely to induce than SBUs. This fact confirms the predictions done in previous simulation works [32]. Secondly, it seems that the LET threshold value is lower for SBUs than for 2-bit MCUs, fact easy to understand given that the critical charge to trigger this single event must be higher.

IV. DISCUSSION

The results and their analysis presented in the previous section provide useful information about the single event effects caused by heavy ions on this new technology of SoCs and FPGAs. This broadens the state-of-the art depicted in the Introduction,

TABLE III
TOTAL NUMBER OF EVENTS PER LET VALUE ACCORDING TO THE MULTIPLICITY.

LET	Fluence	SBU	MCU			False MCU	
			2-bit	3-bit	4-bit	2-bit	3-bit
2.8	2	14	0	0	0	0.00	0.00
8.8	9	874	146	0	0	0.04	0.01
18.1	21.5	3949	1401	8	0	0.83	0.35
32.1	5.5	1448	1095	41	0	0.18	0.08
54.3	14.8	3657	2828	152	5	2.88	1.12
62.4	3	1028	1071	183	5	0.39	0.12
$MeV \cdot cm^{-2}$ /mg	$\times 10^5$ #/cm^2						

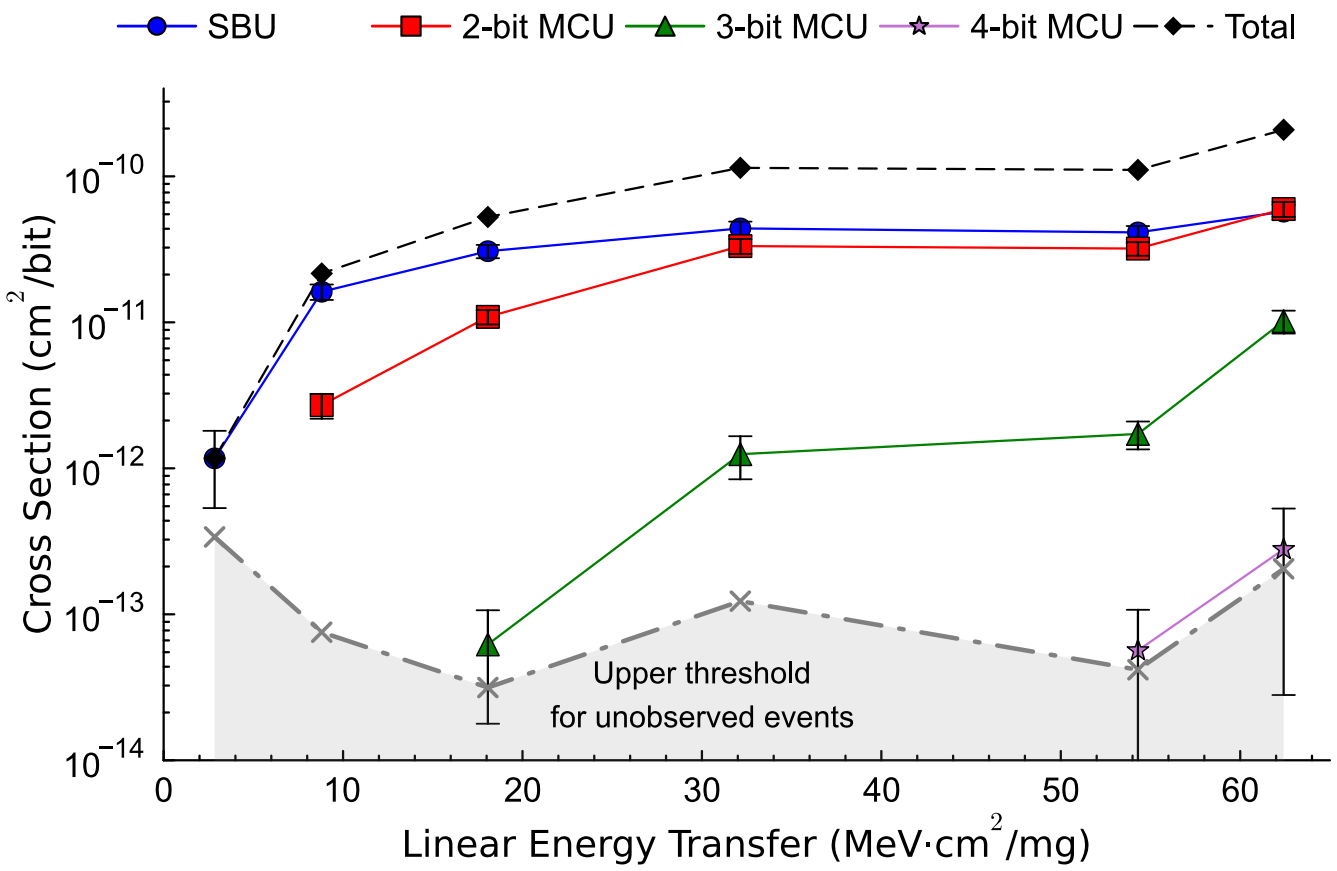


Fig. 3. Single event cross section for the Versal FPGA. All dots have have error bars, although sometimes they are smaller than the dot size.

although there are still some points that need to be investigated. First of all, the role of the written pattern. In Section II-A it was explained that most of the cells in the configuration memory were set to 0, with only a few scattered cells containing 1. It is well known that the pattern is not a key issue in the single bit upset cross section of SRAM cells [33], [34], but it is so for multiple cell upsets [35], [36]. Given that in this technology the number of expected MCUs is larger than that of SBUs, tests using more realistic golden files are of interest. Another parameter to be investigated is the angle of incidence, not only with respect to the normal direction but also to the X and Y axes. Recent experiments have shown that FinFET SRAMs are more sensitive to heavy ions when particles flow along the line formed by the transistor fins [37], so heavy ion irradiations in different combination of angles are advisable. The operation mode is also relevant; single events in dynamic tests are more varied and likely than in static ones [38]. However, they can be technically impossible, since dissipators are necessary and will block the arrival of heavy ions to the die.

At any rate, some topics can be discussed using the information shown in the Section III: the occurrence of single event upsets in comparison to other technologies, the improvement of fault injection tests, and the estimation of the probability of failure in known environments.

A. Single event vs. technology roadmap

It is well known the higher tolerance of FinFET technologies to single events than that observed in equivalent bulk CMOS counterparts due to the increase in the LET threshold value [37], [39], as well as the decrease of the cross section values [40], [41].

This trend seems to hold in this family of FPGAs. In [26]. Vlagkoulis *et al.* tested the Xilinx Zynq-7000 FPGA, built in 28-nm bulk CMOS technology, in different environments and observed that the single event upset cross section for $LET = 8.8\ MeV \cdot cm^2/mg$ at 0^o-incidence was $2.12 \cdot 10^{-9}\ cm^2$, near two order of magnitudes higher than the equivalent dot in Fig. 3. In identical conditions, the cross section for 20-nm devices such as the Ultrascale Kintex is $4.5 \cdot 10^{-10}\ cm^2$ [42]. Newer tecnologies below 20 nm quit the bulk technology and adopt FinFET devices. Thus, the following devices released by Xilinx (UltraScale+) are built in 16-nm technology. It has been observed a dramatic reduction in the value of the SEU cross section, as the values reported by Glorieux *et al.* [43], who measured a cross section around $1.0 \cdot 10^{-10}\ cm^2$ at the LET value used as

TABLE IV
NUMBER OF 2-BIT MCUS ACCORDING TO THE POSSIBLE VALUES OF THE DIFFERENCE OF POSITIONS.

	Distance between flipped bits					
LET	3200	6400	19199	22399	47998	Total
2.8	0	0	0	0	0	0
8.8	129	0	0	6	11	146
18.1	1235	0	0	70	96	1401
32.4	992	0	2	55	46	1095
54.3	2534	4	1	156	133	2828
62.4	966	1	2	62	40	1071

$MeV \cdot cm^2/mg$

reference in this section for comparison. It seems as if this trend has slowed down, since the cross sections for 7 and 16 nm are not very different from each other.

Another striking point is the small size of the observed multiple cell upsets. Unlike older FPGAs, where large MCUs have been observed [23], [26], [44], no event larger than 4 bits have been observed. This behavior seems to be in agreement with previous experiments in this FPGA [5] as well as in static random access memories (SRAM) in the same technology [45], as long as the device works far from the minimum power supply value, where events up to 50 cells have been observed.

B. Considerations about the fault injection campaigns

Failure injection is a good approach for analyzing the performance of the FPGA or SoC CRAM against single or multiple upsets. Moreover, on Versal SoC errors can be injected on NPI registers for improving designs on PS. Setup improvements and failure estimations can be obtained by performing massive error injection campaigns. Then, an initial approach of the performance of the device under test for future heavy ions test can be estimated. Nevertheless, it is well known that they cannot substitute SEE test campaigns as there are some errors like those related to BRAM that cannot be simulated easily on the laboratory.

However, some interesting lessons can be learnt from the results depicted in the previous section. First of all, flipped bits seem to be uniformly distributed along the full body of the readback files, but the absence of knowledge about the internal structure of the device only allows to consider this just a first order approach.

The second detail is very interesting. As the cross sections for single bit upsets (SBUs) and 2-bit MCUs are quite similar, it is unrealistic to base the fault injection campaign on supposing that only SBUs occur. However, a good depiction of the shape of the 2-bit MCUs is necessary. This improvement in fault injection campaigns was proposed by Pérez-Celis et al. [46] and can use the results got from the radiation experiments. In general, these events can be depicted just using the distance between the positions of the flipped bits, which can only be one of the values of Table II. Table IV shows the number of occurrences of every type of 2-bit MCU observed for different values of LET. Fig. 4 is related to this table and is even more illustrating, since it demonstrates that around 90 % of the 2-bit MCUs are pairs of flipped bits in addresses with an offset of 3200, and most of the residual 10 % are pairs separated 22399 or 47999 positions, the former being more likely at high LET values. The occurrences of the two remaining possible values are negligible. This overwhelming presence of 3200 in Fig. 4, which also appears in 3-bit MCUs, can be explained by the strong directionality mentioned in Section IV-A [37].

A similar analysis can be applied to 3-bit MCUs. However, it is necessary to label the every possible combination. Let us suppose that a 3-bit MCU affects the addresses A_0, $A_0 + p$, $A_0 + q$, will be labeled as (p, q)-type, with $p < q$ by definition. p & q must belong to the set of five possible values indicated in Table II and perhaps their combinations, at least theoretically. In practice, only five kinds of 3-bit MCUs were observed (Table V). As in the case of the 2-bit MCUs, Fig. 5 shows the probability of occurrence of the different kinds of events. It can be seen that more than 90 % of the 3-bit MCUs are just three cells separated 3200 positions from the central cell. The other kinds seem to have a dependence on the LET value, although due to the low number of occurrences the uncertainty is relatively high. It must be indicated that an odd value, 44798 = 47998 − 3200, appeared due to the use of the cell with the lowest position as origin for the depiction of the bitflip, but this is just artificial, an was not observed at the time of analyzing the set of data with LELAPE.

Finally, little can be said about the 4-bit MCUs since only 10 events were registered. Six events are just 4 cells with steps of 3200 positions between successive flipped cells.

The previous study allows defining a good strategy to inject bitflips in this kind of FPGA. The effects of the SEUs in the configuration memory can be expressed in terms of the shape of the events in an abstract way, using just the difference of position between flipped cells in the configuration memory. The steps would be the following:

1) A random value is selected is chosen from the set $1 \rightarrow L_N$.
2) This address is the seed of an SBU or an MCU. The probability of occurring one of the possible kinds of events must be proportional to the cross sections observed at that specific value of LET (Fig. 3).
3) If the program decides that there will be an SBU, only this position is flipped.

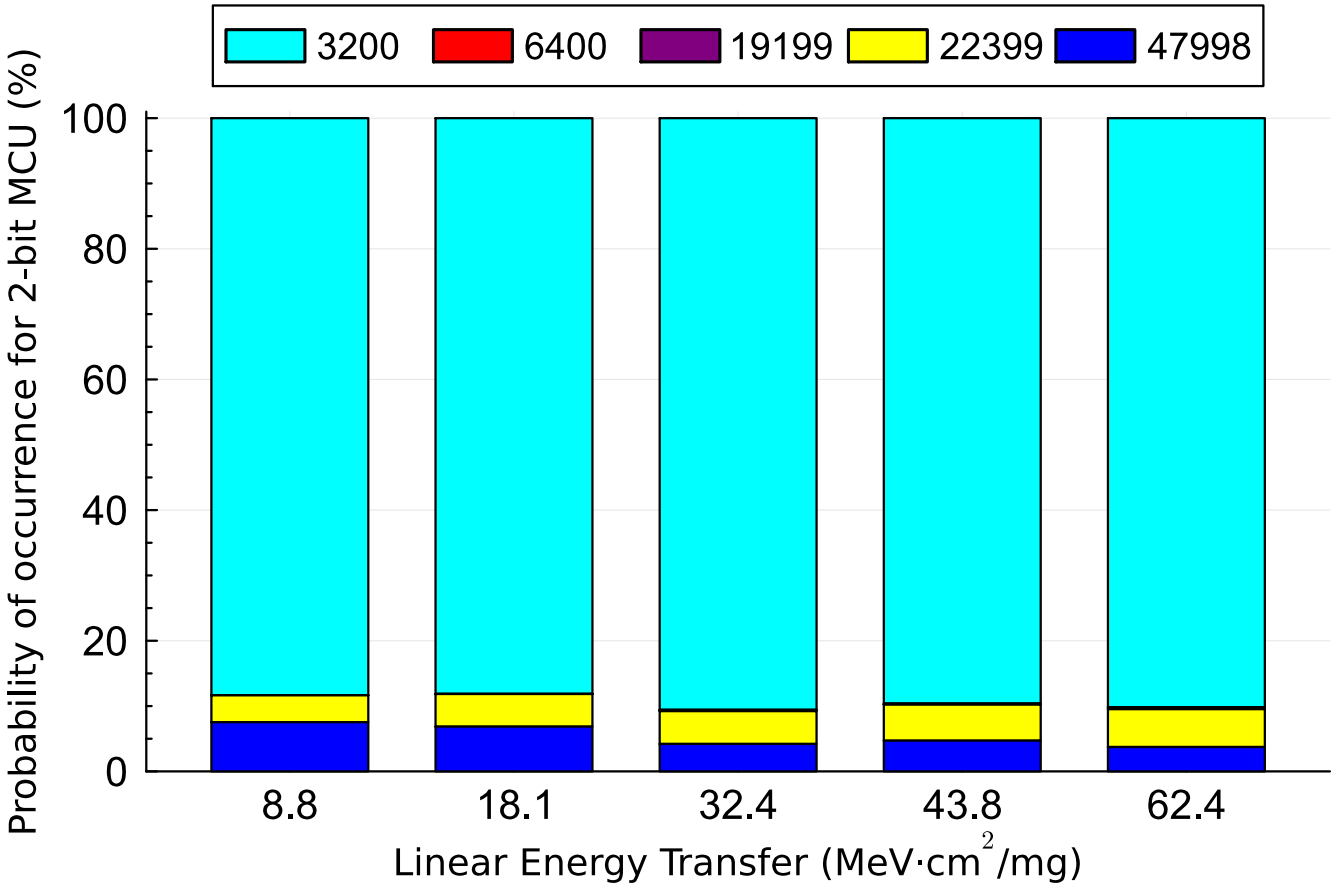


Fig. 4. Distribution of types of 2-bit MCUs according to the offset between involved positions.

TABLE V
TYPES OF OBSERVED 3-BIT MCUS AND OCCURRENCES.

		LET (S.U)			
Type	(p, q)	18.1	32.1	54.3	62.4
A	(3200, 6400)	7	34	125	161
B	(3200, 22399)	0	2	6	3
C	(3200, 47998)	0	1	9	4
D	(19199, 22399)	0	1	9	8
E	(44798, 47998)	1	3	3	7
	Total	8	41	152	183

4) If the decision is to emulate a 2-bit MCU, the cell at that position must be flipped as well as a partner, which will be 90 % times that 3200 positions above, and the rest of times 22,399 or 47998 for simplicity.
5) In the case of emulating a 3-bit MCU, the cell will be flipped and the two other cells will be chosen following the indications of Fig. 5. Thus, 70-80 % of the times the cells 3200 & 6400 positions above will be flipped, and the rest of times the other possible combinations.

In spite of the fact that the previous algorithm makes some simplifications (e.g., the supposition of all the cells being equally likely to flip), the results obtained from injecting bitflips with the previous algorithm will be closer to reality than just injecting isolated bitflips as classically done, allowing the discovery of bugs and weak points that otherwise would have passed unnoticed.

C. Behavior in actual radiation environments

Another interesting application of the results shown in previous sections is that it is possible to estimate the event rate in typical radiation environments in space. For example, Table VI shows the soft error rates for a typical mission in geosynchronous orbits, calculated using the OMERE software [47] with the CREME 96 for heavy ions and galactic cosmic rays in standard environments.

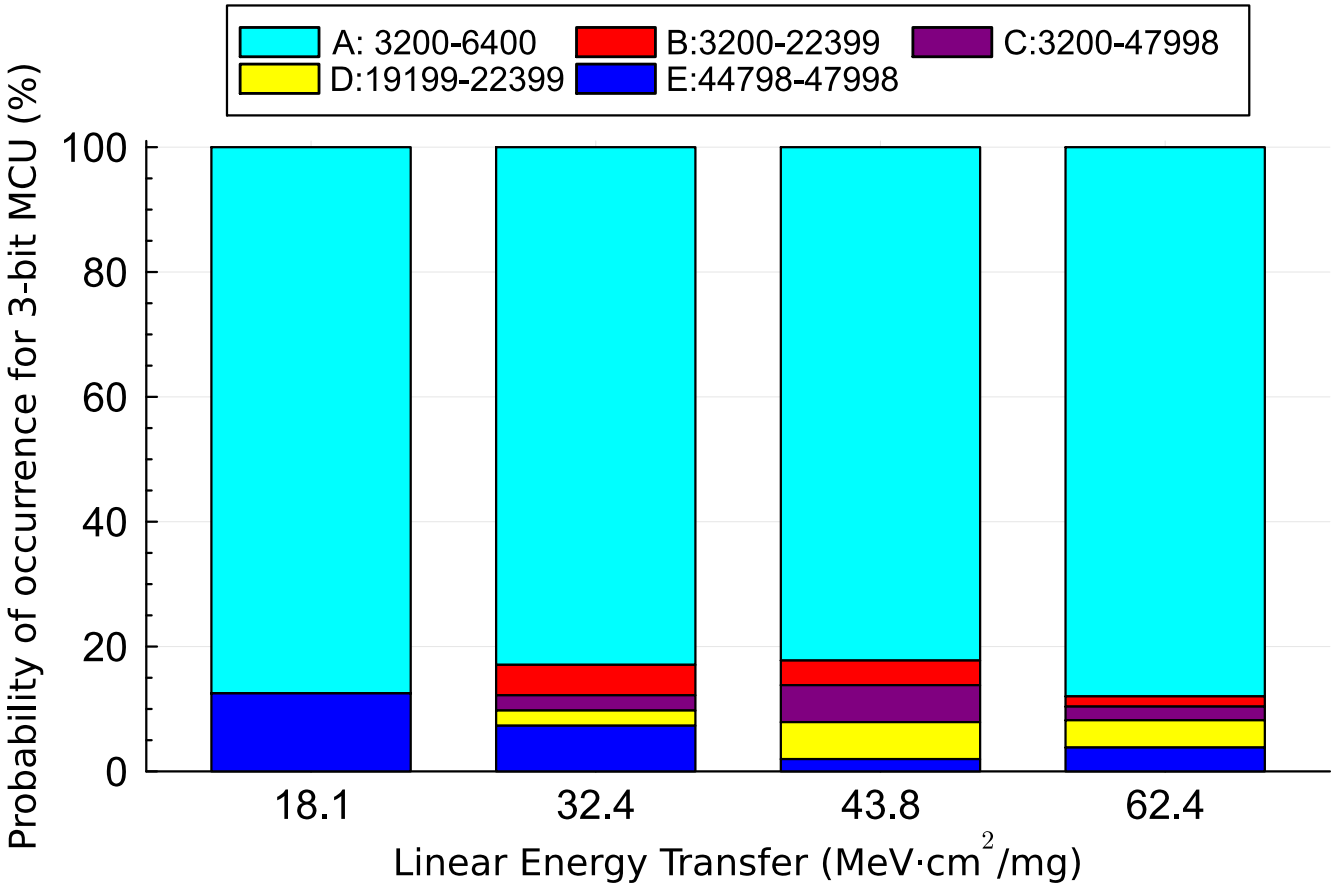


Fig. 5. Distribution of observed 3-bit MCUs according to the identified types.

TABLE VI
SBU AND 2-BIT MCU EVENT RATE FOR A 15-YEAR GEO MISSION.

Event	Galactic cosmic rays steady contribution	Solar flare worst week october 1989
SBU	$1.21 \cdot 10^{-12}$	$1.07 \cdot 10^{-10}$
2-bit MCU	$1.50 \cdot 10^{-14}$	$1.35 \cdot 10^{-12}$
	# events/day/bit	# events/day/bit

V. CONCLUSIONS

Heavy ion tests on a commercial 7-nm FinFET SoC for a wide span of LET values show that the multiple events are small, with multiplicity not higher than 4, unlike those observed in previous generations built in classic bulk CMOS technologies. However, the number of 2-bit multiple events are similar to single bit upsets at high LET values, bringing new challenges to the design of actual systems. Besides, it was demonstrated that the XilSEM, the feature against bitflips implemented by AMD, has proven to be extremely efficient to remove single event upsets, although tougher future tests are necessary.

The extraction of multiple events was done analyzing statistical properties of the flipped bits, and a side effect is that these information can be used by testers to improve fault injections campaigns to validate actual designs.

Further works must study the possible effects of the content stored in the configuration memory of the device, the behavior of the system when irradiated at grazing angles, as well as the effects of other particles and energies.

REFERENCES

[1] Xilinx AMD, "Versal Adaptive SoCs." [Online]. Available: https://www.amd.com/en/products/adaptive-socs-and-fpgas/versal.html.
[2] N. Perryman, C. Wilson, and A. George, "Evaluation of Xilinx Versal Architecture for Next-Gen Edge Computing in Space," in *IEEE Aerospace Conference*, pp. 776–786, Mar. 2023. doi: 10.1109/AERO55745.2023.10115906.
[3] H. Quinn, C. Corley, and P. Thelen, "Neutron-Induced SEEs in the Xilinx Versal Prime," in *IEEE Radiation Effects Data Workshop (REDW) (in conjunction with NSREC)*, pp. 1–8, July 2022. doi: 10.1109/REDW56037.2022.9921523.

[4] H. Quinn, C. Corley, G. Tompkins, and P. Thelen, "Follow-On Testing of the Xilinx Versal Prime," in *IEEE Radiation Effects Data Workshop (REDW) (in conjunction with NSREC)*, pp. 62–70, July 2023. doi: 10.1109/REDW61050.2023.10265849.

[5] Y. P. Chen, P. Maillard, R. D. Veggalam, S. R. Madem, E. Crabill, J. Barton, and M. Voogel, "64MeV Proton single-event evaluation of Xilinx Single Event Mitigation (XilSEM) firmware on 7nm Versal ACAP devices," in *IEEE Radiation Effects Data Workshop (REDW) (in conjunction with 2022 NSREC)*, pp. 14–17, July 2022. doi: 10.1109/REDW56037.2022.9921508.

[6] P. Maillard, Y. P. Chen, J. Arver, V. Merugu, A. Shui, A. Dhavlle, and M. Voogel, "Heavy-Ion and Proton Evaluation of AMD 7nm Versal Multicore Scalar Processing System (PS)," in *IEEE Radiation Effects Data Workshop (REDW) (in conjunction with NSREC)*, pp. 56–61, July 2023. doi: 10.1109/REDW61050.2023.10265824.

[7] P. Maillard, Y. P. Chen, J. Barton, and M. L. Voogel, "Single Event Latchup (SEL) and Single Event Upset (SEU) Evaluation of Xilinx 7nm Versal ACAP programmable logic (PL)," in *IEEE Radiation Effects Data Workshop (REDW)*, pp. 41–46, July 2021. doi: 10.1109/NSREC45046.2021.9679343.

[8] A. Dufour, J. Carron, F. Pierron, M. Fongral, D. Dangla, G. Bascoul, F. Bezerra, J. Mekki, F. Malou, and P. Maillard, "7nm FinFET technology heavy ion SEL evaluation using Xilinx Versal as case study," in *21th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, pp. 75–80, Sep. 2021. doi: 10.1109/RADECS53308.2021.9954564.

[9] AMD, "Versal AI Core Series VCK190 Evaluation Kit." [Online]. Available: https://www.xilinx.com/products/boards-and-kits/vck190.html, 2023. doi: .

[10] AMD Xilinx, "Vivado Design Suite User Guide: Release Notes, Installation, and Licensing (UG973)." [Online]. Available: https://docs.amd.com/r/2022.2-English/ug973-vivado-release-notes-install-license/Release-Notes, 2022.

[11] L. Dilillo, G. Tsiligiannis, V. Gupta, A. Bosser, F. Saigne, and F. Wrobel, "Soft errors in commercial off-the-shelf static random access memories," *Semicond. Sci. Technol.*, vol. 32, no. 1, Dec. 2016. article no. 013006. doi: 10.1088/1361-6641/32/1/013006.

[12] AMD Xilinx, *Xilinx Standalone Library Documentation. BSP and Libraries Document Collection (UG643 v2022.2)*, ch. 12, p. 605. Oct. 2022. [Online]. Avalable: https://www.xilinx.com/support/ documents/sw_manuals/xilinx2022_2/oslib_rm. pdf.

[13] AMD Xilinx, "Open source code for XilSEM on GitHub.." [Online]. Available: https://github.com/Xilinx/embeddedsw/blob/master /lib/sw_services/xilsem/doc/html/api/struct_x_sem_cfr_status.html.

[14] University of Jyväskylä, "RADEF, RADiation Effects Facility." [Online] Available: https://www.jyu.fi/en/science/accelerator-laboratory/facilities-and-instruments/radiation-effects-facility.

[15] Texas A&M University, "Cyclotron Institute's Radiation Effects Facility." [Online]. Available: https://cyclotron.tamu.edu/ref/index.html.

[16] University of Jyväskylä, "European Component Irradiation Facilities Cocktail Calculator." [Online]. Available: http://research.jyu.fi/radef/ECIFcalc/dedx.html.

[17] F. J. Franco and J. Cueto-Rodriguez, "TA06-133: Radiation and Investigation of Memory-based Devices under Heavy IOns (RIMEDHIO)," tech. rep., RADNEXT, May 2024. Zenodo. doi: 10.5281/zenodo.11280181.

[18] F. J. Franco, M. Rezaei, J. C. Fabero, H. Mecha, and J. A. Clemente, "LELAPE: Listas de Eventos Localizando Anomalías al Preparar Estadísticas." [Online]. Available: https://zenodo.org/records/10671559.

[19] J. A. Clemente, M. Rezaei, J. C. Fabero, H. Mecha, and F. J. Franco, "LELAPE: An open-source tool to classify SEUs according to their multiplicity in radiation-ground tests on memories," *IEEE Trans. Nucl. Sci.*, vol. 71, no. 10, pp. 2260–2271, Oct. 2024. doi: 10.1109/TNS.2024.3450607.

[20] M. Wirthlin, D. Lee, G. Swift, and H. Quinn, "A Method and Case Study on Identifying Physically Adjacent Multiple-Cell Upsets Using 28-nm, Interleaved and SECDED-Protected Arrays," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3080–3087, Dec. 2014. doi: 10.1109/TNS.2014.2366913.

[21] J. A. Clemente *et al.*, "Statistical Anomalies of Bitflips in SRAMs to Discriminate SBUs From MCUs," *IEEE Trans. Nucl. Sci.*, vol. 63, no. 4, pp. 2087–2094, Aug. 2016. doi: 10.1109/TNS.2016.2551263.

[22] F. J. Franco *et al.*, "Statistical Deviations From the Theoretical Only-SBU Model to Estimate MCU Rates in SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 8, pp. 2152–2160, Aug. 2017. doi: 10.1109/TNS.2017.2726938.

[23] J. C. Fabero *et al.*, "Single Event Upsets Under 14-MeV Neutrons in a 28-nm SRAM-Based FPGA in Static Mode," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 7, pp. 1461–1469, Jul. 2020. doi: 10.1109/TNS.2020.2977874.

[24] A. Pérez-Celis and M. J. Wirthlin, "Statistical Method to Extract Radiation-Induced Multiple-Cell Upsets in SRAM-Based FPGAs," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 1, pp. 50–56, Jan. 2020. doi: 10.1109/TNS.2019.2955006.

[25] X. Wang *et al.*, "A Statistical Method for MCU Extraction Without the Physical-to-Logical Address Mapping," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 7, pp. 1443–1451, Jul. 2020. doi: 10.1109/TNS.2020.2982033.

[26] V. Vlagkoulis *et al.*, "Single Event Effects Characterization of the Programmable Logic of Xilinx Zynq-7000 FPGA Using Very/Ultra High-Energy Heavy Ions," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 1, pp. 36–45, Jan. 2021. doi: 10.1109/TNS.2020.3033188.

[27] A. Pérez-Celis, C. Thurlow, and M. Wirthlin, "Identifying Radiation-Induced Micro-SEFIs in SRAM FPGAs," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 10, pp. 2480–2487, Oct. 2021. doi: 10.1109/TNS.2021.3108572.

[28] S. Gao *et al.*, "Heavy ion-induced MCUs in 28-nm SRAM-based FPGAs: upset proportions, classifications, and pattern shapes," *Nucl. Sci. Tech.*, vol. 33, no. 12, Dec. 2022. article no. 161. doi:10.1007/s41365-022-01142-7.

[29] J. Guo, G. Mao, W. Liu, C. Shao, R. Wu, Y. Li, J. Zhao, C. Shen, H. Mou, L. Zhang, H. Li, and G. Du, "The Bitmap Decryption Model on Interleaved SRAM Using Multiple-Bit Upset Analysis," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 8, pp. 1857–1864, Aug. 2022. doi: 10.1109/TNS.2022.3186083.

[30] F. J. Franco, J. A. Clemente, G. Korkian, J. C. Fabero, H. Mecha, and R. Velazco, "Inherent Uncertainty in the Determination of Multiple Event Cross Sections in Radiation Tests," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 7, pp. 1547–1554, Jul. 2020. doi: 10.1109/TNS.2020.2977698.

[31] C. Yaqing, H. Pengcheng, S. Qian, L. Bin, and Z. Zhenyu, "Characterization of Single-Event Upsets Induced by High-LET Heavy Ions in 16-nm Bulk FinFET SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 5, pp. 1176–1181, May 2022. doi: 10.1109/TNS.2021.3127567.

[32] E. Ibe, H. Taniguchi, Y. Yahagi, K.-i. Shimbo, and T. Toba, "Impact of Scaling on Neutron-Induced Soft Error in SRAMs From a 250 nm to a 22 nm Design Rule," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1527–1538, Jul- 2010. doi: 10.1109/TED.2010.2047907.

[33] I. Chatterjee, B. L. Bhuva, S.-J. Wen, and R. Wong, "Influence of User-Controlled Parameters in Alpha Particle-Induced Single-Event Error Rates in Commercial SRAM Cells," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, no. 4, pp. 872–879, 2012. doi: 10.1109/TNS.2012.2188839.

[34] B. Ye, J. Liu, T. Wang, T. Liu, K. Maaz, J. Luo, B. Wang, Y. Yin, Q. Ji, Y. Sun, and M. Hou, "Low energy proton induced single event upset in 65nm DDR and QDR commercial SRAMs," *Nucl. Instrum. Methods Phys. Res., Sect. B*, vol. 406, pp. 443–448, 2017. doi: 10.1016/j.nimb.2017.03.162.

[35] A. B. Campbell, O. Musseau, V. Ferlet-Cavrois, W. J. Stapor, and P. T. McDonald, "Analysis of single event effects at grazing angle," in *RADECS 97. Fourth European Conference on Radiation and its Effects on Components and Systems (Cat. No.97TH8294)*, pp. 528–536, 1997. doi: 10.1109/RADECS.1997.698992.

[36] Q. X. Zhang, M. D. Hou, J. Liu, Z. G. Wang, Y. F. Jin, Z. Y. Zhu, and Y. M. Sun, "The impact of incident angle on multiple-bit upset in SRAMs," *Nucl. Instrum. Methods Phys. Res., Sect. B*, vol. 209, pp. 367–370, 2003. doi: S0168-583X(02)02026-8.

[37] K. Takeuchi, K. Sakamoto, K. Yukumatsu, K. Watanabe, Y. Tsuchiya, T. Kato, H. Matsuyama, A. Takeyama, T. Ohshima, S. Kuboyama, and H. Shindo, "Characteristic Charge Collection Mechanism Observed in FinFET SRAM Cells," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 8, pp. 1833–1839, Aug. 2022. doi: 10.1109/TNS.2022.3188993.

[38] G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Todri, A. Virazel, H. Puchner, C. Frost, F. Wrobel, and F. Saigné, "Multiple Cell Upset Classification in Commercial SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, no. 4, pp. 1747–1754, 2014. doi: 10.1109/TNS.2014.2313742.

[39] P. Nsengiyumva, D. R. Ball, J. S. Kauppila, N. Tam, M. McCurdy, W. T. Holman, M. L. Alles, B. L. Bhuva, and L. W. Massengill, "A Comparison of the SEU Response of Planar and FinFET D Flip-Flops at Advanced Technology Nodes," *IEEE Trans. Nucl. Sci.*, vol. 63, no. 1, pp. 266–272, Jan. 2016. doi: 10.1109/TNS.2015.2508981.

[40] N. Seifert, B. Gill, S. Jahinuzzaman, J. Basile, V. Ambrose, Q. Shi, R. Allmon, and A. Bramnik, "Soft Error Susceptibilities of 22 nm Tri-Gate Devices," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2666–2673, Dec. 2012. doi: 10.1109/TNS.2012.2218128.

[41] N. Seifert, S. Jahinuzzaman, J. Velamala, R. Ascazubi, N. Patel, B. Gill, J. Basile, and J. Hicks, "Soft Error Rate Improvements in 14-nm Technology Featuring Second-Generation 3D Tri-Gate Transistors," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 2570–2577, Dec. 2015. doi: 10.1109/TNS.2015.2495130.

[42] D. S. Lee, G. R. Allen, G. Swift, M. Cannon, M. Wirthlin, J. S. George, R. Koga, and K. Huey, "Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation," in *2015 IEEE Radiation Effects Data Workshop (REDW)*, pp. 222–227, Jul. 2015. doi: 10.1109/REDW.2015.7336736.

[43] M. Glorieux, A. Evans, T. Lange, A.-D. In, D. Alexandrescu, C. Boatella-Polo, R. G. Alía, M. Tali, C. U. Ortega, M. Kastriotou, P. Fernández-Martínez, and V. Ferlet-Cavrois, "Single-Event Characterization of Xilinx UltraScale+ MPSOC under Standard and Ultra-High Energy Heavy-Ion Irradiation," in *2018 IEEE Radiation Effects Data Workshop (REDW)*, pp. 189–193, Jul. 2018. doi: 10.1109/NSREC.2018.8584296.

[44] B. Du, L. Sterpone, S. Azimi, D. Merodio Codinachs, V. Ferlet-Cavrois, C. Boatella Polo, R. G. Alía, M. Kastriotou, and P. Fernandez-Martínez, "Ultrahigh Energy Heavy Ion Test Beam on Xilinx Kintex-7 SRAM-Based FPGA," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 7, pp. 1813–1819, Jul. 2019. doi: 10.1109/TNS.2019.2915207.

[45] N. J. Pieper, Y. Xiong, A. Feeley, J. Pasternak, N. Dodds, D. R. Ball, and B. L. Bhuva, "Study of Multicell Upsets in SRAM at a 5-nm Bulk FinFET Node," *IEEE Trans. Nucl. Sci.*, vol. 70, no. 4, pp. 401–409, Apr. 2023. doi: 10.1109/TNS.2023.3246085.

[46] A. Pérez-Celis, C. Thurlow, and M. Wirthlin, "Emulating Radiation-Induced Multicell Upset Patterns in SRAM FPGAs With Fault Injection," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 8, pp. 1594–1599, Aug. 2021. doi: 10.1109/TNS.2021.3071704.

[47] TRAD, "The OMERE Software. v5.8.1." [Online]. Available: https://www.trad.fr/en/space/omere-software/, Feb. 2024.

[48] R. G. Alía, A. Coronetti, K. Bilko, M. Cecchetto, G. Datzmann, S. Fiore, and S. Girard, "Heavy Ion Energy Deposition and SEE Intercomparison Within the RADNEXT Irradiation Facility Network," *IEEE Trans. Nucl. Sci.*, vol. 70, no. 8, pp. 1596–1605, Aug. 2023. doi: 10.1109/TNS.2023.3260309.