

Low interface trap density in rapid thermally annealed Al/SiN_x:H/InP metal–insulator–semiconductor devices

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(Received 21 September 1998; accepted for publication 12 December 1998)

A minimum interface trap density of 10^{12} eV⁻¹cm⁻² was obtained on SiN_x:H/InP metal–insulator–semiconductor structures without InP surface passivation. The SiN_x:H gate insulator was obtained by the electron cyclotron resonance plasma method. This insulator was deposited in a single vacuum run and was composed of two layers with different nitrogen-to-silicon ratios. The first layer deposited onto the InP was grown with a nitrogen-to-silicon ratio of N/Si=1.55, whereas the second one was grown with a N/Si ratio of N/Si=1.43. After the insulator deposition, rapid thermal annealing of the devices was performed at a constant annealing time of 30 s. The interface trap density minimum value was obtained at an optimum annealing temperature of 500 °C. Higher annealing temperatures promote thermal degradation of the interface and a sharp increase in the trap density. © 1999 American Institute of Physics. [S0003-6951(99)02007-0]

There is considerable interest in InP-based field-effect transistor technology [both metal–semiconductor field-effect transistors (MESFET) and metal–insulator–semiconductor field-effect transistor (MISFET)] due to its high electron mobility and saturated electron drift velocity. However, there are two main limiting factors of device performance: the low Schottky barrier height on InP (MESFET) and the high surface state density at the insulator–InP interface (MISFET).¹ In the latter device, the use of SiN_x:H as a gate insulator has been proven to be a good choice to obtain excellent interfaces.² In this case, the gate insulator deposition should be performed with a technique that minimizes the semiconductor surface damage and, therefore, the trap density at the insulator/InP interface. The electron cyclotron resonance (ECR) plasma deposition of SiN_x:H films onto InP gives excellent results both at the insulator properties and the interface electrical characteristics² because the insulator is deposited without any ion bombardment of the InP surface and at low substrate temperature. This last condition is the key-note in the insulator deposition on III–V semiconductors due to the thermal degradation of the semiconductor surface. Recently, we have proved^{2,3} that the whole MISFET technology could be simplified using the ECR plasma technique (for the insulator deposition), because high-quality Al/SiN_x:H/InP metal–insulator–semiconductor (MIS) devices could be obtained without any treatment of the InP surface prior to the SiN_x:H deposition.

In this letter we present further improvements in the fabrication of MIS structures, mainly focusing on the reduction of the interface trap density. To accomplish this requirement, we have made use of the following approaches:

- (i) The gate insulator was a structure composed of two different layers (in the following, a dual layer gate), obtained in a single deposition run but in two different steps: in the first one, a film with a nitrogen-to-

silicon (N/Si) ratio of 1.55 was grown directly onto the InP surface. Immediately after, the second layer with N/Si=1.43 was further deposited. The reason for these SiN_x:H composition will be given later.

- (ii) The structures were annealed to improve the interface characteristics of the SiN_x:H/InP structures. This procedure has been previously reported to optimize GaAs-based MIS devices.⁴

The MIS structures were fabricated on unintentionally doped *n*-type (100) InP wafers ($n \sim 5 \times 10^{15}$ cm⁻³). The samples were decreased with organic solvents and then etched in a HIO₃:H₂O (10% weight) solution during 1 min. Sets of six samples were immersed during 15 s in HF:H₂O (1:10), rinsed in deionized water, and dried in N₂ before being transferred to the ECR chamber. The insulator deposition was set at low temperature (200 °C) and at constant total pressure (0.6 mTorr). The gases used were N₂ and pure SiH₄. The gas flux ratios, $R = N_2/SiH_4$, used to deposit the dual layer gate were $R=9$ for the N/Si=1.55 layer and $R=5$ for the N/Si=1.43 one.⁵ The thicknesses of each component of the dual gate were ~ 50 Å for the first layer (N/Si=1.55), and ~ 150 Å for the layer with N/Si=1.43.

Each sample was further annealed at different rapid thermal annealing (RTA) cycles at temperatures between 400 and 800 °C during 30 s in Ar atmosphere, except one of them that was not annealed. Afterwards, the gate was defined by 3000-Å-thick Al dots, thermally evaporated through a mechanical mask. The electrode area was 1.2×10^{-3} cm². Finally, the back electrode (AuGe/Au) was also thermally evaporated. A postmetallization annealing was performed in Ar atmosphere (300 °C/20 min).

The device characterization was made measuring simultaneously the capacitance–voltage (C – V) curves [quasi-static (C_q) and high-frequency (C_h)] with a Keithley model 82 system. The distribution of the interface trap density (D_{it}) was calculated with the high–low-frequency method.⁶

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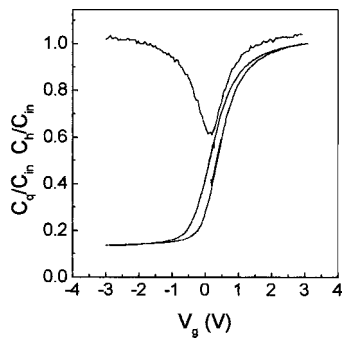


FIG. 1. High-frequency (C_h) and quasi-static (C_q) C - V characteristics normalized to the insulator capacitance (C_{in}) of Al/SiN_x:H/InP as a function of gate voltage for the best analyzed device. The insulator was deposited with the following composition: 50 Å at $R=9$ and 150 Å at $R=5$, and was annealed at 500 °C/30 s.

In Fig. 1 we present the capacitance-voltage characteristics corresponding to the best Al/SiN_x:H/InP structure, which was annealed at 500 °C/30 s. Figure 1 shows an excellent quasi-static curve, with a very large dip, revealing a low interface trap density and the unpinning of the Fermi level at the InP surface. The high-frequency C - V curve exhibits a reduced hysteresis, which suggests a low level of slow traps at the interface and a good quality of the SiN_x:H film.

In Fig. 2, we present the D_{it} distribution obtained for the device shown in Fig. 1. This distribution has the characteristic U-shaped form of C - V measurements and it has been observed in all the characterized devices. The distribution exhibits a minimum located at 0.37 eV above the midgap with an energy value similar to that reported by Kapila *et al.*⁷ The minimum of the interface trap density is 1×10^{12} eV⁻¹ cm⁻². In the same figure, we show a comparison between the results obtained by other authors in devices where the InP surface was treated in H₂S atmosphere⁷ or passivated with the deposition of an interface control layer (ICL).^{8,9} Figure 2 reveals the good quality of the interface of our structures. It should be pointed out that the three sets of data shown in Fig. 2 were obtained from the same measurement procedure, i.e., the C - V high-low-frequency method. The accuracy of the estimated D_{it} values is greatest at the minimum,¹⁰ in consequence, the comparison is straightforward and this fact leads us to conclude that our results reveal

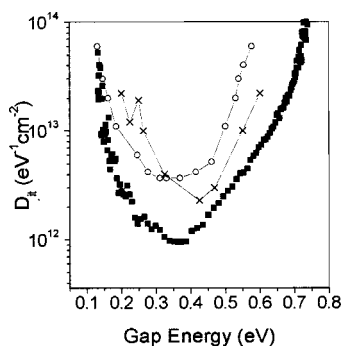


FIG. 2. Distribution of interface trap density as a function of gap energy plotted relative to the midgap, for the MIS structure measured in Fig. 1. (■) This work (—○—) results from Landheer *et al.* (Ref. 8) for devices passivated with an interface control layer and (—×—) results from Kapila *et al.* (Ref. 7) for devices treated in H₂S atmosphere.

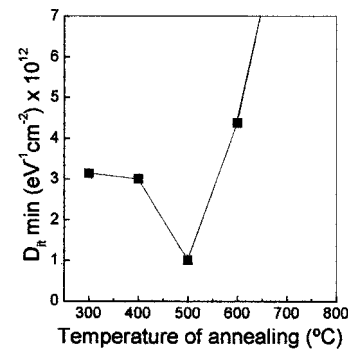


FIG. 3. Influence of RTA treatment on the minimum of D_{it} for devices in which the insulator was obtained as in Fig. 1. The line is drawn as a guide to the eye.

a better interface quality than those presented using the passivation methods mentioned above.

Regarding the insulator characteristics, the measured values for the resistivity and the breakdown field were $3\text{--}5 \times 10^{14}$ Ω cm and about 2 MV/cm, respectively. These results are similar to those recently published by Hugon *et al.*¹¹ The good quality of the device shown in Figs. 1 and 2 is due to the dual layer gate. The choice of the different compositions (N/Si=1.55 and N/Si=1.43) used in the dual gate structure is due to the following reasons: with the N/Si=1.55 layer we have recently obtained good SiN_x:H/InP interface properties,^{2,3} whereas the N/Si=1.43 layer gives the highest resistivity films.^{1,2} In consequence, the dual layer gate here described should combine both high interface quality and high insulator resistivity in the gate structure. Recently, a similar dual layer structure for the gate insulator has been successfully used in Si-based MIS devices.¹²

On the other hand, the influence of RTA temperature on the minimum of D_{it} is shown in Fig. 3. The structures were always made with the composition above described, i.e., N/Si=1.55 (50 Å) and N/Si=1.43 (150 Å). The minimum of the trap density decreases up to the annealing of 500 °C/30 s. It is known that low-temperature treatments in SiN_x:H promote a thermal relaxation and reconstruction of the lattice.^{5,13} For that reason, a simultaneous decrease of dangling-bond density is obtained.^{5,14} Since the dangling bonds are electrically active, a reduction of their concentration induced by RTA may also induce a decrease of D_{it} at the interface according to the data of Fig. 3.

For RTA temperatures higher than 500 °C, Fig. 3 shows a sharp increase of the minimum of D_{it} . The increase of the RTA temperature may promote a high thermal stress in the structure and the SiN_x:H/InP interface gets damaged, which explains the increase of D_{it} .

Summarizing, we have shown the good quality of Al/SiN_x:H/InP MIS structures deposited by the ECR-chemical vapor deposition (CVD) technique. In order to improve the interfacial electronic properties, a dual layer gate of SiN_x:H was used as the gate insulator. With this structure, a minimum of the interface state density of 1×10^{12} eV⁻¹ cm⁻², and hysteresis about 0.2 V were obtained. Also, we have analyzed the influence of RTA temperature on the D_{it} minimum. The best results were obtained with an annealing cycle of 500 °C/30 s. That points to a reconstruction of the SiN_x:H lattice and to a decrease in the dangling bonds

present both in the insulator and at the insulator/InP interface.

The process described above allows us to obtain Al/SiN_x:H/InP devices with similar quality as those passivated with physical or chemical procedures.

The authors would like to thank C. A. I. de Implantación Iónica from the Universidad Complutense in Madrid for technical assistance with the ECR-CVD system.

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