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## Conductance Transient Comparative Analysis of Electron-Cyclotron Resonance Plasma-Enhanced Chemical Vapor Deposited $\text{SiN}_x$ , $\text{SiO}_2/\text{SiN}_x$ and $\text{SiO}_x\text{N}_y$ Dielectric Films on Silicon Substrates

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An interface quality comparative study of metal-insulator-semiconductor (MIS) structures based on  $\text{SiN}_x$ ,  $\text{SiO}_2/\text{SiN}_x$  and  $\text{SiO}_x\text{N}_y$  dielectric films deposited on silicon substrates by electron-cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD) has been carried out. Overall interpretation of deep-level transient spectroscopy (DLTS) and conductance transient (G-t) measurements enables us to conclude that the interface quality of  $\text{Al}/\text{SiO}_x\text{N}_y/\text{Si}$  MIS structures is superior to those of  $\text{Al}/\text{SiN}_x/\text{Si}$  devices. Moreover, we have proved that thermal treatments applied to  $\text{Al}/\text{SiO}_x\text{N}_y/\text{Si}$  capacitors induce defect passivation, possibly related to the presence of hydrogen in the films, and disorder-induced gap-state (DIGS) density maxima can decrease to values even lower than those corresponding to  $\text{Al}/\text{SiN}_x/\text{SiO}_2/\text{Si}$  devices.  
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**KEYWORDS:** silicon nitride, silicon oxynitrides, ECR-PECVD, MIS structures, interface states, insulator damage, DLTS, conductance transients

### 1. Introduction

In the field of silicon-based metal-insulator-semiconductor (MIS) devices, as dimensions decrease to below 100 nm in ultralarge-scale integrated circuits (ULSI), the thickness of the gate dielectric in field-effect transistors (FET) falls to the 3–4 nm range. In these ultrathin insulators, the incorporation of  $\text{SiN}_x$  interlayers in the standard  $\text{SiO}_2$  dielectric films appears to be successful in order to improve gate performance, degraded due to tunneling currents and permeability to boron and alkali ion diffusion.  $\text{SiN}_x$  shows better impermeability properties than  $\text{SiO}_2$ , as well as a higher dielectric constant which enables the realization of physically thicker dielectrics with the same capacitance-voltage performance.<sup>1)</sup> Different approaches have been developed to combine the properties of  $\text{SiO}_2$  and  $\text{SiN}_x$ , such as stacked oxide–nitride–oxide (ONO) structures,<sup>2)</sup> nitrified silicon oxide films<sup>3)</sup> and compound silicon oxynitride films.<sup>1,4)</sup> However, MIS structures based on these types of dielectrics present some problems related to insulator-semiconductor interface quality, because it is necessary to carry out a complementary effort in order to develop reliable characterization methods of defects.

In this work, we present an interface quality comparative study of MIS structures based on  $\text{SiN}_x$ ,  $\text{SiO}_2/\text{SiN}_x$  and  $\text{SiO}_x\text{N}_y$  dielectric films deposited on silicon substrates by electron-cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD). PECVD techniques utilize a plasma for the generation of active precursor species which enables the deposition of the films at low temperatures. Moreover, the ECR technique allows a very efficient activation of the precursor gases,<sup>5,6)</sup> and the damage due to ion bombardment is reduced, since the substrates are placed outside the plasma region.<sup>7)</sup> As we have shown in previous works,<sup>8–10)</sup> standard measurements such as capacitance–voltage ( $C$ – $V$ ) measurements and deep-level transient spec-

troscopy (DLTS) only provide partial information, and thus could induce erroneous conclusions. However, conductance transient analysis (G-t) provides a more complete picture of the interface, as it enables us to estimate the disorder induced gap states (DIGS) density, i.e., both spatial and energetic distribution of defects at the insulator-semiconductor interface.

### 2. Experimental

The  $\text{Al}/\text{SiN}_x/\text{n-Si}$  and  $\text{Al}/\text{SiN}_x/\text{SiO}_2/\text{n-Si}$  devices were obtained as follows: the substrates used were n-Si (5  $\Omega\text{cm}$ ,  $\langle 100 \rangle$  orientation), on which we had previously deposited Al back electrodes by thermal evaporation. The substrates were cleaned using standard chemical procedures starting with dipping into acetone and methanol followed by drying with nitrogen. Then silicon was successively subjected to the following cleaning steps: dipping in  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  (1:2:5) solution for 5 min, rinsing with deionized  $\text{H}_2\text{O}$ , dipping in  $\text{HF}:\text{H}_2\text{O}$  (1:10) solution for 1 min and then rinsing with deionized  $\text{H}_2\text{O}$ . Lastly, the substrates were blown dry again with nitrogen. Then, we deposited a layer of silicon dioxide over one half of the samples by using an Astex ECR plasma source model AX4500. The  $\text{O}_2$  gas flux was 30 sccm during 3 h. Silicon dioxide thickness was approximately 90 Å. Subsequently, all the samples were subjected to an ECR-PECVD  $\text{SiN}_{1.44}$  film deposition. Gases employed in this deposition were  $\text{N}_2$  (8.76 sccm) and pure  $\text{SiH}_4$  (1.76 sccm), with a deposition time of 12 min 57 s in order to obtain a silicon nitride thickness of 740 Å. So, we have obtained two types of samples: one with a silicon oxide layer deposited over the silicon substrate, and other one, without it. In all the ECR-PECVD depositions, chamber pressure and substrate temperature were maintained at 100 W and 200°C, respectively. Al dots ( $1.24 \times 10^{-3} \text{ cm}^2$ ) were thermally evaporated through a shadow mask as gate electrodes.

As for  $\text{Al}/\text{SiO}_x\text{N}_y/\text{n-Si}$  MIS structures, the precursor gases were  $\text{N}_2$ ,  $\text{O}_2$  and  $\text{SiH}_4$ . The oxygen plus nitrogen flow to silane flow ratio was kept constant:  $R = (\Phi(\text{O}_2) +$

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$\Phi(\text{N}_2)/\Phi(\text{SiH}_4) = 5$ . However, the oxygen to silane ratio,  $Q = \Phi(\text{O}_2)/\Phi(\text{SiH}_4)$ , was varied in order to obtain different  $x$  and  $y$  parameter values. We obtained  $x = 0.63$  and  $y = 0.99$  for  $Q = 0.41$ , and  $x = 1.01$  and  $y = 0.70$  for  $Q = 0.61$ .<sup>11)</sup> The parameter  $R$  determines the silane partial pressure during deposition and, therefore, the incorporation of silicon in the samples, while  $Q$  controls the amount of oxygen in the films. During the deposition process, reactions to incorporate oxygen and nitrogen to the film are competitive, and the oxygen reaction takes preference. For high values of  $Q$  ( $Q > 2.5$ ), all the silane reacts with  $\text{O}_2$  despite the presence of  $\text{N}_2$  in the plasma, and the  $\text{SiO}_2$  composition is obtained. However, for lower  $Q$  values, some  $\text{SiH}_4$  remains which reacts with nitrogen, and intermediate oxynitride compositions are obtained.<sup>12,13)</sup> In order to determine the influence of thermal treatments on the quality of the silicon oxynitride/silicon interface, some samples were not subjected to any thermal annealing, whereas the others underwent a thermal treatment in argon atmosphere at  $300^\circ\text{C}$  for 20 min immediately after contact evaporation process was carried out.

When defects are not only located at the insulator/semiconductor interface but are spatially distributed in the insulator, they are called DIGS or “slow traps”, and conductance transients can be detected by applying bias pulses that drive MIS structures from deep to weak inversion.<sup>8)</sup> Indeed, the capture process takes place in which the empty DIGS trap electrons arriving by tunneling from the semiconductor conduction band. States near the interface capture carriers before those located deeper in the dielectric; hence, this process is time consuming. The measurement conditions (frequency and temperature) significantly affect the conductance transient shape, so from the experimental conductance transients recorded at several frequencies and at several temperatures it is possible to obtain three-dimensional defect maps, i.e., the DIGS density as a function of the spatial distance to the interface and of the energy position.<sup>9)</sup>

In a strict sense, both capacitance and conductance signals are influenced by slow traps. However, MIS devices typically show near-zero conductance in contrast to high capacitance values. Therefore, in order to evaluate slow traps, it is preferable to measure conductance transients occurring above near zero background values than capacitance transients that actually are very small variations around the standby capacitance values.

The experimental setup consists of the HP 33120A arbitrary waveform generator for applying the bias pulse and the EG&G 5206 two-phase lock-in analyzer for measuring the conductance. An HP 54501A digitizing oscilloscope records the complete conductance transient. Samples were cooled in darkness from room temperature to 77 K at 0 bias in an Oxford DN1710 cryostat. An Oxford ITC 502 controller was used to keep the temperature constant during the measurements.

### 3. Results and Discussion

First, we carried out a  $C$ - $V$  and DLTS electrical characterization of the entire set of devices. Both room-temperature and 77 K  $C$ - $V$  curves obtained for all the samples clearly exhibit hysteresis phenomena, i.e., capacitance values depend on the direction of the voltage variation,

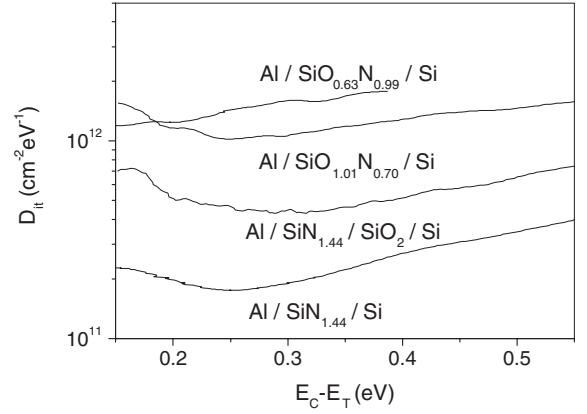


Fig. 1. Interfacial state density measured using DLTS of  $\text{Al}/\text{SiN}_x/\text{SiO}_2/\text{Si}$ ,  $\text{Al}/\text{SiN}_x/\text{Si}$  and  $\text{Al}/\text{SiO}_x\text{N}_y/\text{Si}$  MIS devices.

thus indicating that interface state distribution fits the DIGS model<sup>14,15)</sup>

The DLTS signal is obtained by recording capacitance transients at several temperatures, the samples pulsed between weak inversion and accumulation. DLTS measurements were carried out at a modulation frequency of 1 MHz. At this frequency, the slow traps located far from the interface cannot respond and only traps located at the interface respond to the small a.c. voltage variations. These measurements provide profiles of the interface state density ( $D_{it}$ ) as a function of the energy level measured from the bottom of the silicon conduction band ( $E_C - E_T$ ).<sup>16)</sup> Figure 1 shows DLTS profiles corresponding to  $\text{SiN}_x$ ,  $\text{SiO}_2/\text{SiN}_x$  and unannealed  $\text{SiO}_x\text{N}_y$  dielectric films. We can observe that  $D_{it}$  values are higher for silicon oxynitride films than for silicon nitride films and silicon oxide/silicon nitride stack films. On the other hand, it is surprising that the interface quality of  $\text{Al}/\text{SiN}_x/\text{SiO}_2/\text{Si}$  samples appears to be inferior to those of  $\text{Al}/\text{SiN}_x/\text{Si}$  devices.

Conductance transient measurements can be used to help clarify this issue. From the experimental conductance transients,  $G(t)$ , we can obtain the DIGS state density ( $N_{\text{DIGS}}$ ) as a function of the spatial distance to the interface ( $x_c$ ) and of the energy position, as follows:<sup>9)</sup>

$$N_{\text{DIGS}} = \frac{\Delta G/\omega}{0.4qA} \quad (1)$$

$$x_c(t) = x_{\text{on}} \ln(\sigma_0 v_{\text{th}} n_s t) \quad (2)$$

$$E' - E(x_c, t) = H_{\text{eff}} + kT \ln \left( \frac{\sigma_0 v_{\text{th}} N_c}{\omega/1.98} \right) - kT \frac{x_c(t)}{x_{\text{on}}}, \quad (3)$$

where  $x_{\text{on}} = \hbar/2\sqrt{2m_{\text{eff}}H_{\text{eff}}}$  is the tunneling decay length,  $\sigma_0$  is the carrier capture cross-sectional value for  $x = 0$ ,  $v_{\text{th}}$  is the carrier thermal velocity in the semiconductor,  $m_{\text{eff}}$  is the free carrier effective mass,  $n_s$  is the free carrier density at the interface and  $N_c$  is the carrier concentration in the semiconductor bulk. Furthermore,  $\omega$  is the angular frequency,  $q$  is the electron charge, and  $t$  is time. Finally,  $H_{\text{eff}}$  is the insulator-semiconductor energy barrier for minority carriers and  $E'$  denotes the carrier energy band edge at the insulator ( $E'_c$  for electrons and  $E'_v$  for holes). In the case of n-type silicon, the values of the parameters that only depend on the semiconductor substrate are  $\sigma_0 = 10^{-14} \text{ cm}^2$ ,  $v_{\text{th}} = 10^7 \text{ cm s}^{-1}$ ,  $m_{\text{eff}} = 0.32m_0$  ( $m_0 \equiv$  free electron mass),  $N_c = 2.7 \times 10^{19} \text{ cm}^{-3}$

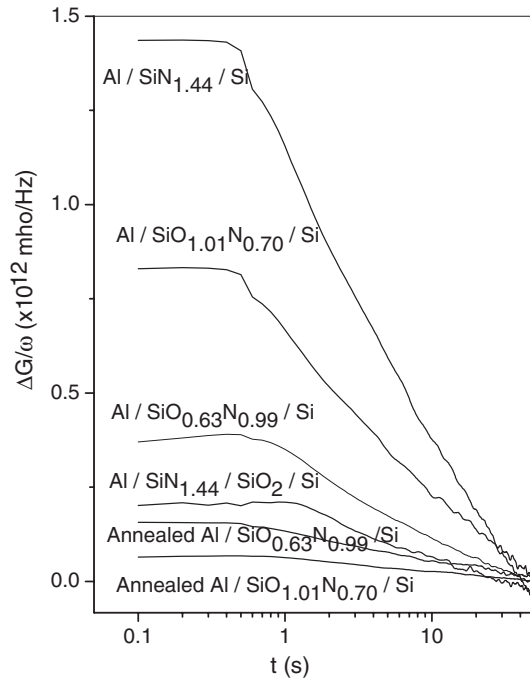


Fig. 2. 100 KHz room-temperature conductance transients corresponding to Al/SiN<sub>x</sub>/SiO<sub>2</sub>/Si, Al/SiN<sub>x</sub>/Si and Al/SiO<sub>x</sub>N<sub>y</sub>/Si MIS devices. Results for annealed Al/SiO<sub>x</sub>N<sub>y</sub>/Si structures are also shown.

and  $n_s = 10^{17} \text{ cm}^{-3}$ . As for  $H_{\text{eff}}$ , we used values as appearing in the literature: 3.2 and 2 eV for the SiO<sub>2</sub>/Si and SiN<sub>x</sub> systems, respectively.<sup>17)</sup> As for SiO<sub>x</sub>N<sub>y</sub>, we assume a linear dependency on the nitrogen to silicon content of these films as has been proved elsewhere.<sup>18,19)</sup> This yields a value of 2.47 eV and 2.71 eV for the Si<sub>1.01</sub>N<sub>0.7</sub>/Si and Si<sub>1.01</sub>N<sub>0.7</sub>/Si systems, respectively.

Figure 2 shows conductance transients recorded at room temperature and 100 KHz corresponding to all types of samples. As DIGS density is proportional to transient height, we can observe that Al/SiN<sub>x</sub>/Si devices exhibit the highest DIGS density, whereas the lowest one corresponds to Al/SiN<sub>x</sub>/SiO<sub>2</sub>/Si samples. Silicon oxynitride film-based MIS capacitors show an intermediate behavior. Moreover, in the same figure, conductance transients corresponding to MIS devices based on annealed silicon oxynitride films are plotted: in these cases, conductance transients are comparable to those obtained for Al/SiN<sub>x</sub>/SiO<sub>2</sub>/Si, i.e., DIGS density is markedly reduced.

The same picture remains in the case of complete three-dimensional defect maps, obtained by systematically recording conductance transients at temperatures varying between 77 and 300 K and frequencies ranging between 100 Hz and 100 KHz. Figures 3(a) and 3(b) shows the maps corresponding to Al/SiN<sub>x</sub>/SiO<sub>2</sub>/Si and Al/SiN<sub>x</sub>/Si samples, respectively. In these figures,  $E_C - E$  axis is taken in reference to the semiconductor, i.e., negative values indicate energy positions located in the silicon conduction band, whereas positive values correspond to band gap positions.  $x_c$  is the spatial distance in the dielectric film, measured from the interface insulator/semiconductor. We can see that for Al/SiN<sub>x</sub>/SiO<sub>2</sub>/Si samples (a), DIGS defects exist up to depths of only 20 Å into the insulator bulk, and their energy positions belong to the silicon band gap and to the silicon conduction band. Additionally, the maximum DIGS density,

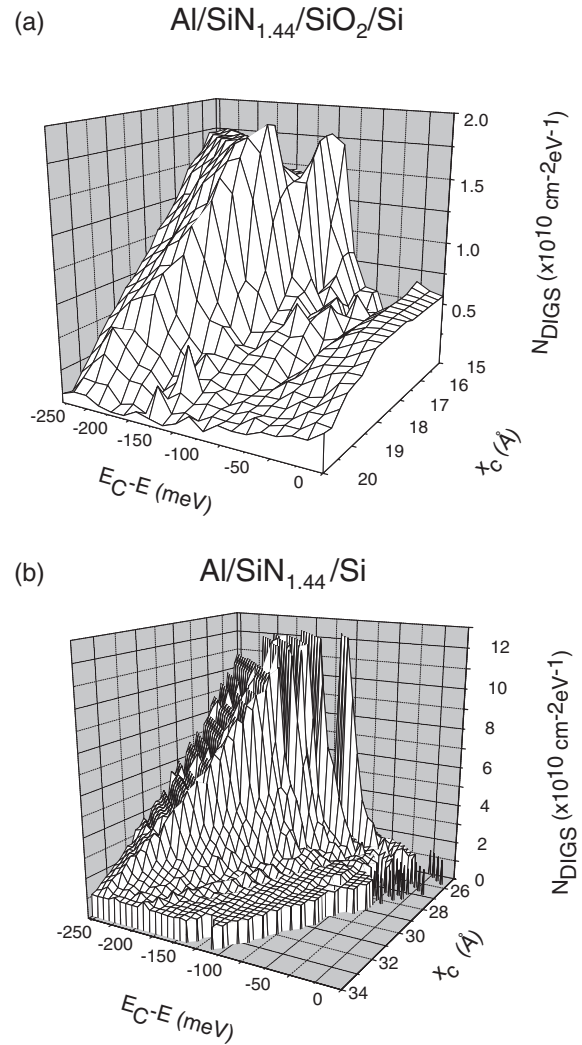


Fig. 3. Three-dimensional DIGS profiles of Al/SiN<sub>x</sub>/SiO<sub>2</sub>/Si (a) and Al/SiN<sub>x</sub>/Si (b) samples.

located at 150 meV above the silicon conduction band edge, is approximately  $2 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ . However, for the Al/SiN<sub>x</sub>/Si devices (b), although the maximum DIGS density is also located at 150 meV above the silicon conduction band edge, it is about one order of magnitude higher ( $1.2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ). Moreover, DIGS are spatially located far from the interface into the dielectric bulk up to depths of 35 Å, and their energy positions only belong to the silicon conduction band.

As for the unannealed silicon oxynitride film-based MIS devices, Fig. 4 shows the DIGS distribution obtained for SiO<sub>0.63</sub>N<sub>0.99</sub> (a) and SiO<sub>1.01</sub>N<sub>0.70</sub> (b) films. By comparing with Fig. 3, we observe that the general shape is similar to that for the Al/SiN<sub>x</sub>/Si devices: DIGS are spatially located into the dielectric bulk up to depths of almost 35 Å, and their energy positions only belong to the silicon conduction band. However, the maximum DIGS density values ( $4 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  and  $6 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ , respectively) are intermediate between those corresponding to Al/SiN<sub>x</sub>/SiO<sub>2</sub>/Si ( $2 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ ) and Al/SiN<sub>x</sub>/Si ( $1.2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ) samples.

Hence, an overall comparison of DLTS and G-t measurements enables us to conclude that defects in samples with a SiO<sub>2</sub> layer are preferentially located very close to the

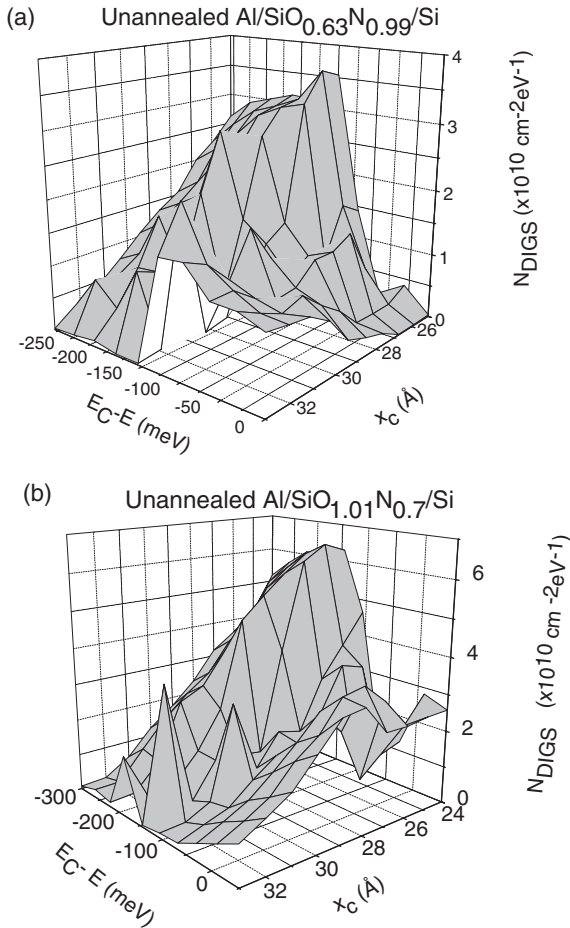


Fig. 4. Three-dimensional DIGS profiles of unannealed Al/SiO<sub>x</sub>N<sub>y</sub>/Si MIS devices:  $x = 0.63$  and  $y = 0.99$  (a),  $x = 1.01$  and  $y = 0.70$  (b).

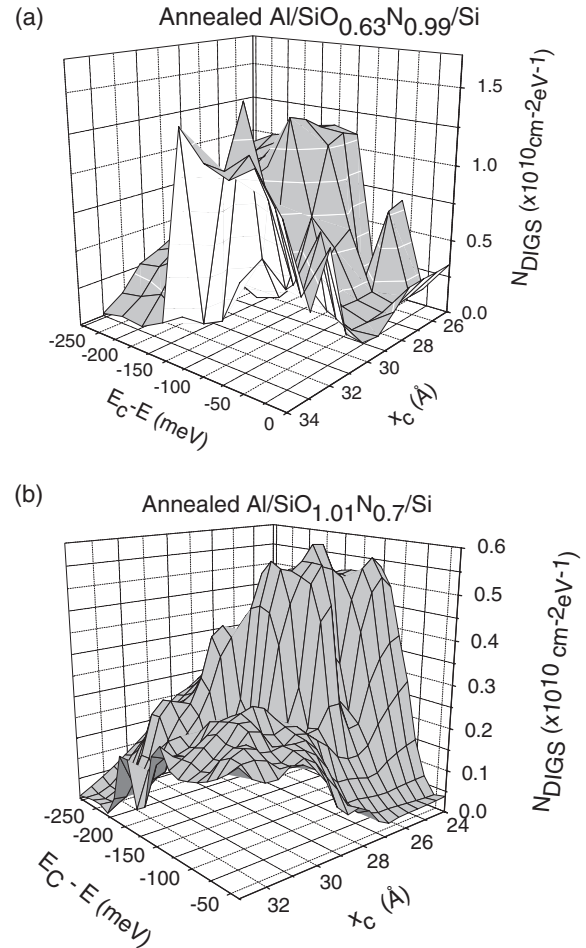


Fig. 5. Three-dimensional DIGS profiles of annealed Al/SiO<sub>x</sub>N<sub>y</sub>/Si MIS devices:  $x = 0.63$  and  $y = 0.99$  (a),  $x = 1.01$  and  $y = 0.70$  (b).

interface Si/SiO<sub>2</sub>, whereas in silicon nitride films and silicon oxynitride film-based MIS devices, DIGS are states spatially located farther away from the interface into the dielectric bulk whose energy positions belong to the silicon conduction band. Moreover, although Al/SiO<sub>x</sub>N<sub>y</sub>/Si MIS structures show a higher interfacial state density than Al/SiN<sub>x</sub>/Si devices, they exhibit lower DIGS density values, and thus better interface quality. Therefore, silicon oxynitride films are a valuable alternative to silicon oxide films.

Lastly, with respect to the annealed silicon oxynitride film-based MIS devices, in Fig. 5 we can see that again DIGS are spatially located into the dielectric bulk up to depths of almost 35 Å, and their energy positions only belong to the silicon conduction band. However, DIGS density maxima decrease to values even lower than those corresponding to Al/SiN<sub>x</sub>/SiO<sub>2</sub>/Si devices:  $1.2 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  for SiO<sub>0.63</sub>N<sub>0.99</sub> (a) and  $6 \times 10^9 \text{ cm}^{-2} \text{ eV}^{-1}$  for SiO<sub>1.01</sub>N<sub>0.70</sub> (b). Thus, thermal treatments induce defect passivation, possibly related to the presence of hydrogen in the films, as discussed by us in a previous paper.<sup>20</sup> This result shows that silicon oxynitride is a highly attractive material for the microelectronic industry.

#### 4. Conclusions

An interface quality comparative study of MIS structures based on SiN<sub>x</sub>, SiO<sub>2</sub>/SiN<sub>x</sub> and SiO<sub>x</sub>N<sub>y</sub> dielectric films deposited on silicon substrates by electron cyclotron

resonance plasma-enhanced chemical vapor deposition (ECR-PECVD) has been carried out. Overall interpretation of DLTS and conductance transient measurements enables us to conclude that as for Al/SiN<sub>x</sub>/SiO<sub>2</sub>/Si samples, defects are primarily concentrated at the insulator-semiconductor interface, whereas in the case of Al/SiN<sub>x</sub>/Si and Al/SiO<sub>x</sub>N<sub>y</sub>/Si MIS structures, they are spatially distributed in the insulator bulk. Also, although Al/SiO<sub>x</sub>N<sub>y</sub>/Si MIS structures show higher interfacial state density than Al/SiN<sub>x</sub>/Si devices, they exhibit lower DIGS density values, and thus better interface quality. Moreover, we have proved that thermal treatments applied to Al/SiO<sub>x</sub>N<sub>y</sub>/Si capacitors induce defect passivation, possibly related to the presence of hydrogen in the films, and DIGS density maxima can decrease to values even lower than those corresponding to Al/SiN<sub>x</sub>/SiO<sub>2</sub>/Si devices. Thus, from the interface quality point of view, silicon oxynitride is a highly attractive material for the microelectronic industry. This result reinforces the well-known advantages of silicon oxynitride with respect to SiO<sub>2</sub> (lower permeability to boron-atom diffusion and alkali ions, better reliability of the devices and higher dielectric constant) and Si<sub>3</sub>N<sub>4</sub> (lower mechanical stress and higher band gap).

Lastly, in this work we have shown that standard electrical characterization ( $C$ - $V$  and DLTS) could induce us to make erroneous conclusions, but conductance transient analysis provides a more complete picture of DIGS distribution.

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