Impact of Dynamic Voltage Scaling on SEU Sensitivity of COTS Bulk SRAMs and A-LPSRAMs against Proton Radiation

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***Abstract*—In aerospace industry, Commercial-Off-The-Shelf (COTS) Static Random Access Memories (SRAMs) are a cost-effective solution for obtaining high performance at the system level, which is difficult to obtain using space qualified components. Additionally, the usage of Dynamic Voltage Scaling (DVS) is commonly used in space environments, where low power consumption is a critical issue. This paper presents an analysis of the sensitivity against Single Event Upsets (SEUs) of various COTS bulk SRAMs and Advanced Low-Power SRAMs against proton radiation when using DVS to save power. Experimental results will show a clear evidence that the sensitivity to SEUs increases when the power is lowered. 2 sets of successive technologies (130-nm, 90-nm and 65-nm bulk SRAMs; and 150-nm and 110-nm A-LPSRAMs) are evaluated against 15 MeV protons and compared with results of 14 MeV neutrons presented in a previous work. Experimental data are finally compared with analytical simulations obtained by using the MUSCA-SEP3 Monte-Carlo tool to predict the effect of DVS on the SEE sensitivity on more modern technologies in the ITRS/IRDS roadmap.**

***Index Terms*—COTS, SRAM, proton tests, radiation hardness, reliability, soft error, MUSCA-SEP3.**

I. Introduction and Related Work

THE usage of Commercial-Off-The-Shelf (COTS) devices in space industry has recently become a promising alternative to space-qualified components [1]. Thus, many COTS parts can safely work in such for several years although they were not initially considered for space applications and therefore, they cannot provide as hardness assurance as space-qualified ones. Another important reason for their adoption in certain missions is that they attain performance levels that cannot be reached otherwise [2], [3].

This innovative concept, i.e., "COTS in space", can be combined with Dynamic Voltage Scaling (DVS), which consists in reducing the bias voltage of certain components that are kept idle in order to save power [4], [5]. This is especially interesting for autonomous systems, where the power consumption is a key issue. DVS can be successfully applied to non-volatile memories, by switching them off when they are not used; and to volatile ones, by keeping their supply voltage above a certain limit that guarantees data retention [6]. However, for the latter, it is also well known that, when reducing the bias voltage below the level recommended by the manufacturer (also known as "nominal voltage"), the critical charge needed to trigger a Single Event Upset (SEU) decreases as well [7]. This results into a SEU sensitivity increase that may be unacceptable and therefore, it must be studied and understood.

Many works in the literature have devoted to study the effect of DVS on the SEU sensitivity of nanoscale devices. Thus, different materials have been studied [8], as well as academic custom D Flip-Flops [9] and SRAM cells [10]. However, little work has been carried out with COTS devices. An interesting one was made by Rodbell et al. [11] by exposing a COTS IBM 32-nm SOI SRAM against low-energy protons. Also, in previous works the authors studied the effect of DVS of neutrons and alpha particles on COTS 130-nm, 90-nm and 65-nm bulk SRAMs manufactured by Cypress Semiconductor [12], [13] and on 150-nm Advanced Low-Power SRAMs (A-LPSRAMs), provided by Renesas [14]. The latter are built with cells that contain 2 additional capacitors that increase the stored charge to make bitflips less likely to occur.

This paper makes an analysis of the impact of DVS on the same SRAMs discussed in [12], [13], the A-LPSRAM in [14], as well as a new A-LPSRAM manufactured also by Renesas in 110-nm process, under 15 MeV proton radiation. These memories were biased with voltage levels ranging from 0.5V to 3.3V, which is the nominal one according to the manufacturers.

Finally, this experimental analysis will be completed with an analytical study of scaling trends for miniaturized technologies in the ITRS/IRDS roadmap [15]. Indeed, it is well known that the per-bit SEU sensitivity [16]–[18] as well as the cell critical charge [19] decreases with miniaturization. Thus, the application of DVS on technologies ranging from 150-nm to 45-nm

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TABLE I
TESTED MEMORIES AND OPERATIONAL BIAS VOLTAGES

Manufacturer	Device	Technology process	range (V)
Cypress	$CY62167GE30-45ZXI$ (a)	65-nm	$0.75-3.25$
	$CY62167EV30LL-45ZXI$ (b)	90-nm	$0.50-3.25$
	$CY62167DV30LL-55ZXI$ (c)	130-nm	$0.50-3.25$
Renesas	$RMLV1616AGSA-5S2$ (d)	110-nm	$0.90-3.25$
	$R1LV0408DSP-5SI$ (e)	150-nm	$0.65-3.25$

will be investigated, by using the MUlti-SCAles Single Event Phenomena Predictive Platform (MUSCA-SEP3), a modeling tool developed at the French Aerospace Lab (ONERA) [20], [21].

II. EXPERIMENTAL SETUP

Table I presents the Devices Under Test (DUTs) studied in this paper. They were controlled by a microcontroller board based on the Atmel SAM3X8E ARM Cortex-M3 CPU running at up to 84 MHz on an Arduino Due. To store the results and provide power, the microcontroller is connected to a computer system. It is possible to control the supply voltage of the DUT by means of a variable voltage generator, using the computer system. The variable voltage generator can provide a tunable voltage ranging from 0.05 to 3.5 V, which can leverage the operation of the memory at ultra-low bias voltage.

The system was completely tested before and after the irradiation in order to guarantee that the observed errors were due to radiation and not to consequences of a problem in the experimental setup and the memories retained information at their threshold voltages. Using a 40-pin parallel connection, the microcontroller was connected to the memory, whereas the data transmission to the computer was made with a USB port that virtualized the serial communication through the UART of the microcontroller. Everything in the irradiation chamber except the DUT itself was shielded with thick aluminum plates to not be affected during the tests, whereas the computer was in another room for controlling and monitoring the process. This is the exact same setup used before in [22].

Each test consisted of five successive steps:

1) In order to observe all the SEUs that actually occurred in the memory cells, by using proprietary information provided by the manufacturer, the ECC provided by the SRAM hardware was turned off.
2) The data are written on the memory with a specific pattern. In this case, the *checkerboard* patterns (0x55 and 0xAA) were used for logistic reasons.
3) The bias voltage of the memory is reduced and the device stays on stand-by.
4) The memory is exposed to radiation.
5) After irradiation, the bias voltage is restored to nominal and the memory is checked for errors.

It should be mentioned that, when performing the tests on Step 3), in order not to activate over-voltage protection structures present in the memories, all the address and data buses, as well as the enable pins were set to 0. This was done only when it was necessary to change the supply voltage of the memory from nominal to low. In consequence, the data of the first address of the memory was always written to 0x00 (consequently lost for performing the experiments), whichever the pattern was. Considering the size of the memory and the fact that only 8 bits were lost, it is totally bearable to sacrifice this data to adjust the voltage. Since the 65-nm memory contains ECC protection, to observe the bitflips it is neccesary to turn it off by means of a special sequence that is provided by the manufacturer.

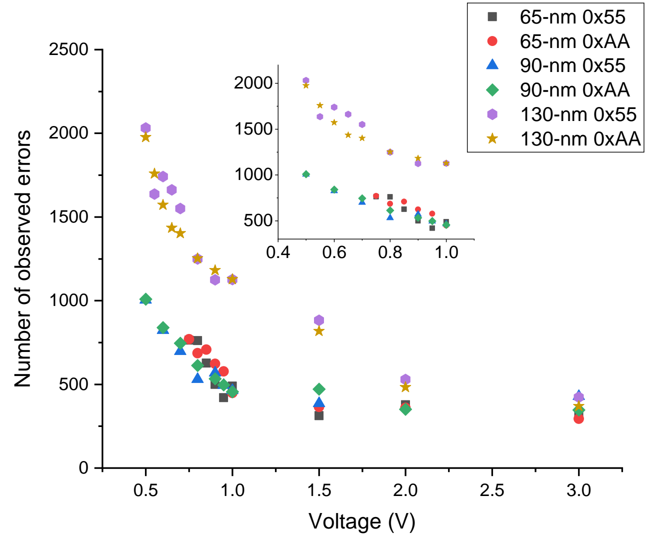

Fig. 1. Total number of bitflips observed for Cypress memories (Devices (a)-(c) in Table I) under proton radiation (rounds including micro-latchups for the 90-nm memory are excluded)

The proton irradiation campaign took place in May 2019 in the cyclotron laboratory at CNA (Centro Nacional de Aceleradores), Spain [23]. The irradiation campaign was performed at normal incidence in air, using the external beam line. The DUTs were placed at 56 cm from the exit nozzle with 100 μm aluminum foil as window, so that the final proton energy at the surface was 15.6 MeV, with an estimated spread in the order of 400 keV. The final energy of the incident beam was obtained using the energy loss data calculated with the SRIM2013 code [24]. The uniformity of the flux was better than 90% in the exposed area of interest, maintaining the flux stability within 5% during each experimental run.

III. EXPERIMENTAL RESULTS

A. Cypress SRAMs

The memories were tested in their functional range of bias V_{CC} from nominal to slightly above the threshold voltage. For each memory, two different patterns (0x55 and 0xAA) were written to examine the pattern impact on the results. Due to the time constraints, the blanket patterns (0x00 and 0xFF) were not tested in this study; however these patterns might show a slightly different behavior compared to the previous ones [25].

Fig. 1 shows the normalized number of bitflips observed in each memory at several voltages for the mentioned patterns with respect to the fluence at each round. At first glance it is noticeable that all devices showed more bitflips on lower

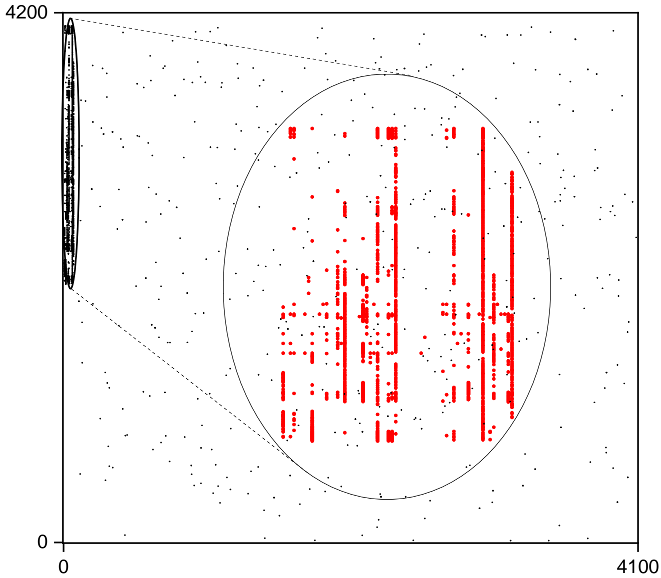

Fig. 2. bitmap of the 90-nm memory and the observed micro-latchup. Each point is the physical position of a bitflip in the DUT, indicating the axes as X and Y in the ranges of 0-4100 and 0-4200 respectively. The expanded region includes the micro-latchup with dimensions of 70×2000.

voltages compared to the nominal ones. Considering that these devices have the same sizes and the tests were performed with the same total radiation fluence, comparing the number of bitflips based on patterns does not show any significant differences in the results for each device. It is also clear that the 130-nm memory underwent more bitflips compared to the two other ones, especially at low voltages. However, at nominal voltage the number of bitflips for all the devices are similar. The results obtained at V_{CC} ranging from 0.4 to 1 V are zoomed out in Fig. 1 for the sake of clarity.

It should be mentioned that, even if at the first look the number of bitflips for the 65-nm and 90-nm memories are similar, during the tests with the 90-nm one, the authors observed many bitflips caused by micro-latchups and had to reset the device to resume the tests. Fig. 2 shows the physical position of the bitflips with respect to the DUT itself in one of the test rounds including a micro-latchup for the 90-nm memory. The same phenomenon had been observed before by the authors, testing this device under 14 MeV neutrons [12]. This type of events have been introduced before as Type-D MCU in [26]. Occurrence of a micro-latchup causing a major delay of controlling signals (for example a word line selection) in the vertical edge of a memory array, far from the address decoder, can explain the existence of this phenomenon. Also, areas with less dense faulty cells can be seen in the corrupted area of the zoomed section of the Fig. 2. Existence of current limiters and separate power lines for these areas may possibly justify these gaps in this faulty section. Since said events cause thousands of bitflips, they were excluded from Fig. 1 in favor of better readability.

An in-depth discussion of these results is presented in Section IV, including a comparison with 14 MeV neutrons carried out by the authors in a previous work [13], as well as future technological trends when applying DVS.

TABLE II
RUN SEQUENCE OF THE IRRADIATION CAMPAIGN FOR THE RENESAS MEMORIES

Device	Round	Voltage (V)	Time (s)	Flux $(p/cm^2/s)$ $\times 10^8$	Cumulative Fluence (p/cm^2) $\times 10^{10}$	Observed bitflips
110-nm (1)	1	3.25	60	1.8	1.08	0
	2	3.25	60	8.1	5.94	0
	3	3.25	60	44	32.34	×
110-nm (2)	4	0.9	60	6.8	4.08	46
	5	0.9	60	16	13.68	×
110-nm (3)	6	0.9	60	6.8	4.08	28
	7	0.9	300	7.3	25.98	6172
	8	0.9	120	6.8	34.14	×
110-nm (4)	9	0.9	60	5.8	3.48	1
	10	0.9	60	6.3	7.26	13
	11	0.9	300	6.1	25.56	229
	12	0.9	300	6.2	44.16	21675
150-nm	13	3.25	60	1.8	1.08	0
	14	3.25	60	5.6	4.44	0
	15	1	60	5.6	7.8	2
	16	0.75	300	5.4	24	26
	17	0.75	300	6.4	43.2	95
	18	0.75	300	8	67.2	1687

B. Renesas A-LPSRAMs

The manufacturer of the Advanced Low Power SRAMs (A-LPSRAMs) studied in this work claims that they are immune to the radiation, which was experimentally verified by the authors in [27] under 14-MeV neutrons. However, previous results analyzing the effects of DVS under 15-MeV neutron irradiation on Device (e) (Table I) [14] showed the contrary. Therefore, it is interesting to analyze the impact of proton radiation too. Table II shows the results for several 110-nm and one 150-nm A-LPSRAMs. Since the authors did not know about their SEU sensitivity, tests on these devices were run using trial and error.

At first, a 110-nm part was tested at a low flux and nominal voltage for one minute and no bitflip was observed. Therefore, the second test was done with a higher flux but the result was the same. To increase the probability of observing bitflips, the third round was run on a relatively high flux (4.4×10^9 $p/cm^2/s$). Nevertheless, the device stopped functioning and lost its data completely after this round, which might have been due to Total dose effect (TID). TID due to protons can cause devices suffer threshold shifts, increased device leakage (and power consumption), timing changes, decreased functionality, etc [28]. The Authors were not able to measure the exact accumulated dose on each device, however, the cumulative fluence is shown in Table II for each A-LPSRAM as a reference. It is important to mention that many of the addresses were not functional even after resetting the device and they could not retain information anymore, thus a new device was applied for the next rounds of tests.

Regarding the previous experiment, the authors run the 4th round of tests on the minimum possible functional voltage for the device and, again, with a low flux. As a result 46 bitflips were observed, however this number is very low to draw any conclusion with a high certainty. Therefore Round

5 underwent a higher flux compared to the previous one and the same result as Round 3 was observed. This again led to replacing the device with a new memory.

Round 6 was run with the same configurations as the only successful test (Round 4) to make sure the new memory has similar sensitivity. Since the results were comparable, the following round was needed to have more bitflips without the same problem as Round 5. Thus, the authors decided to extend the radiation time from 1 minute to 5 minutes on the 7th round and 6172 bitflips were observed. With this number of bitflips there is a probability of observing false multiple events by accumulation of simpler ones, so to avoid them, round 8 was performed with 2 minutes of radiation. Regardless of less time, once again the memory was unusable after this round and needed to be replaced.

The configuration of rounds 9 to 12 was selected with the same logic of previous ones to achieve a reasonable number of bitflips. However, the outcome was slightly different. After the 12th round, unless the device was functional at nominal voltage, it was unable to fully retain the data in lower voltages. At voltages below 1.5 V, even without any irradiation, some bits (in range of thousands) flipped, showing that the irradiation caused an increase in the minimum threshold voltage of these devices. The authors tested the previous devices (a,b, and c) and all of them showed the same behaviour. This phenomenon has been observed and described before in literature as low-voltage stuck bits [14].

The 150-nm memory showed a similar behavior as the 110-nm one. It was immune to radiation at nominal voltages, but bitflips started to appear at voltages below or equal to 1 V. However, for Rounds 16-18, (0.75 V with very similar proton fluences), results were very diverse: from 26 bitflips in Round 16, to 1687 bitflips in Round 18. This suggests that these A-LPSRAMs are sensitive to high fluences or to dose accumulation. The authors suggest to carry out TID tests to verify this hypothesis.

IV. Discussion and Technological Trends

A. About the Impact of DVS on Bulk COTS SRAMs

Comparing the results based on just the number of events is not sufficient. To have a better insight of these results in a comparable way, the cross-sections for each event type were calculated. These devices use bit interleaving to prevent MBUs and indeed, no MBUs were observed in any of the experiments. For Devices (a)-(c) (Table I), the authors used a confidential map provided by Cypress Semiconductor to relate the logical bit positions to the physical locations to precisely analyze the number of SBUs/MCUs. Any isolated bitflip observed in the memory is presented as an SBU. Affected addresses located at a Manhattan distance equal or lower than 3 were grouped in the same MCU.

Fig. 3 shows the SBU and n-bit MCU ($2 \leq n \leq 4$) cross-sections of the 65-nm (a), 90-nm (b) and 130-nm (c) memories with 0x55 and 0xAA patterns under 15 MeV protons. The SBU and n-bit MCU cross-sections of all the devices increase by lowering the supply voltage, specially at the lowest ones. Devices (a) and (b) have similar cross-sections even though the latter has a lower threshold voltage. However, Device (c) (130-nm) shows a higher SEU sensitivity compared to the two previous ones. Indeed, it is visible that not only the one-to-one SEU sensitivities for this device are higher, but also MCUs with higher multiplicity were observed (for instance, the presence of 4-bit MCUs in Fig. 3 c) is noticeable).

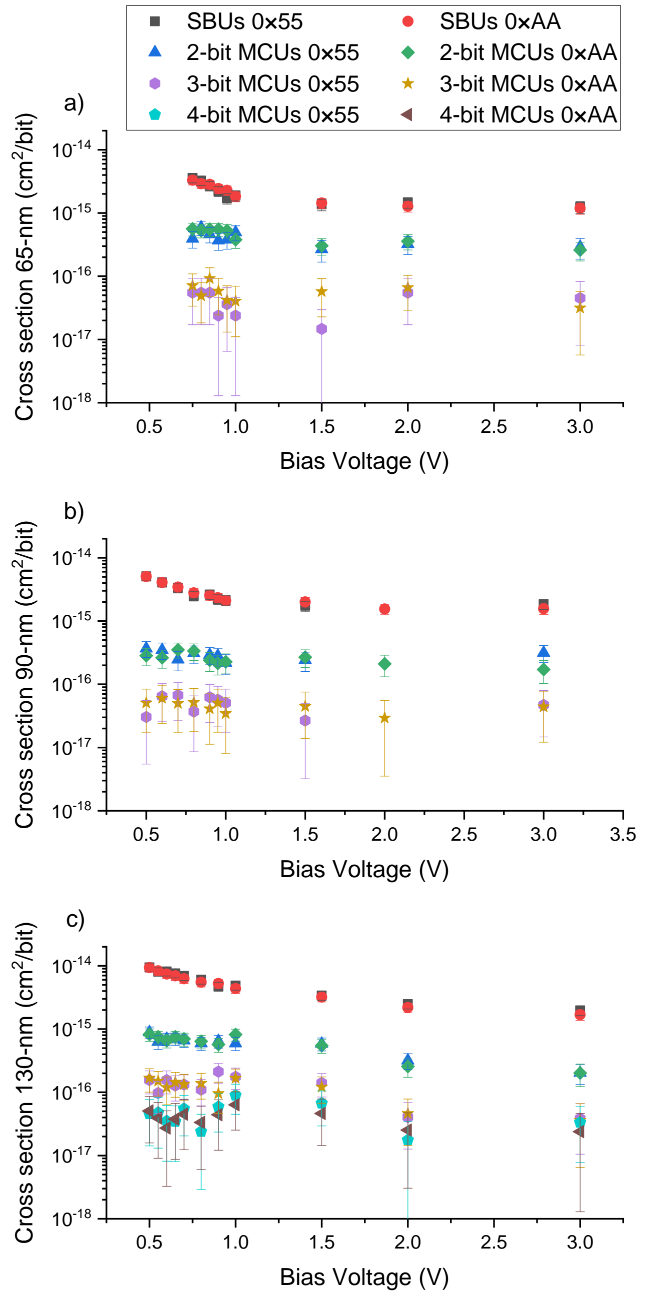

Fig. 3. 15 MeV proton SEU cross-sections of the 65-nm (a), 90-nm (b) and 130-nm (c) memories (0x55 and 0xAA patterns)

The graphs include error bars for the experimental cross-sections counting in the beam profile (±10%), fluence accuracy (±10%) and with 95% of confidence intervals as discussed in [29]. Also the probability of occurrence of so-called "false 2-bit MCUs" (MCUs that are derived from the combination of two independent SBUs) was also taken into account using the equations presented by the authors in [30].

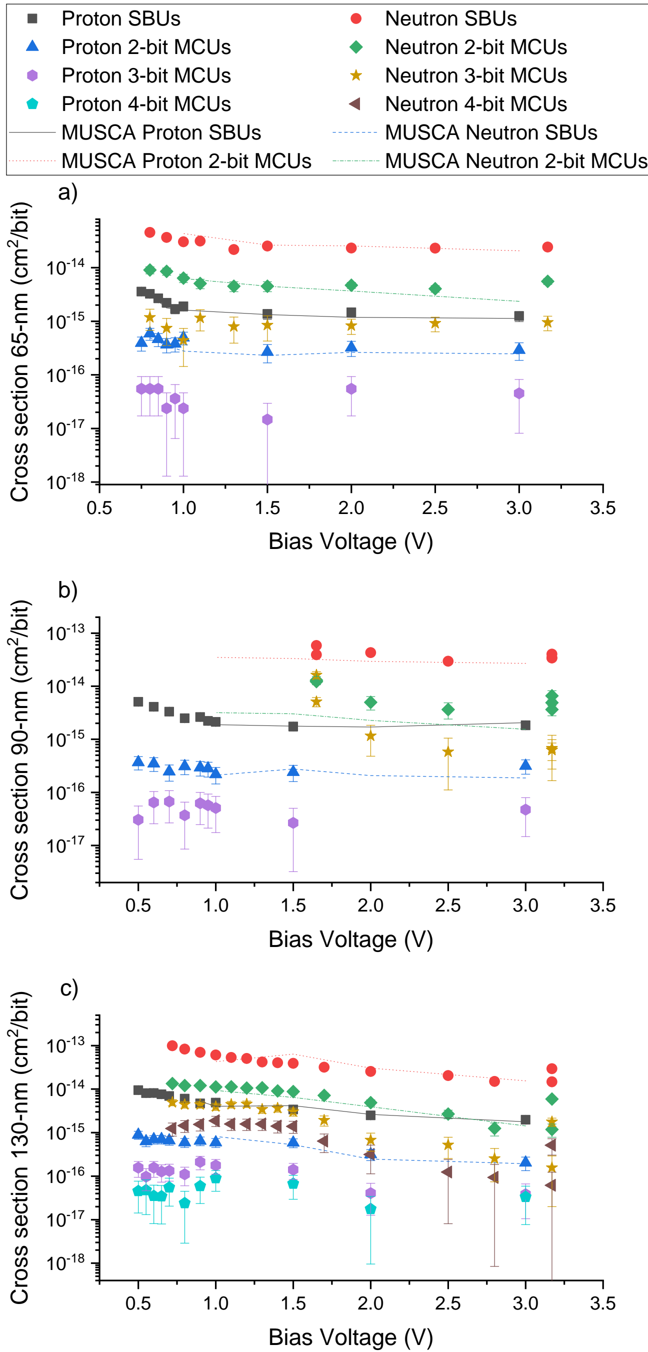

Fig. 4. 15 MeV proton and 14.2 MeV neutron SEU cross-sections of the 65-nm (a), 90-nm (b) and 130-nm (c) memories (0x55 pattern)

It is important to mention that, based on the number of bitflips per round of reading and the size of these memories (16 Mb), estimations yield that no false 2-bit MCUs occurred in any round that involved devices (a) or (b). For device (c), the maximum number of such false events was 4, (for the round made at 0.5 V with the 0xAA pattern) 2236 bitflips were observed on that occasion.

These memories were previously tested by the authors in [13] under 14.2 MeV neutrons and similar DVS conditions. Fig. 4 shows the SEU cross-section comparisons between 14.2 MeV neutrons and 15 MeV protons. It can be seen that the proton and neutron SEU cross-sections for all the devices have the same trend, however the neutron ones are constantly above the proton ones by one order of magnitude. The discussion of this difference is out of the scope of this study and was already done before in [22]. Briefly, this can be explained by higher energies of secondary ions produced by neutrons and their direction, as well as a bump in the SEE sensitivity found and analyzed at about 14.2 MeV neutrons in a previous work [31].

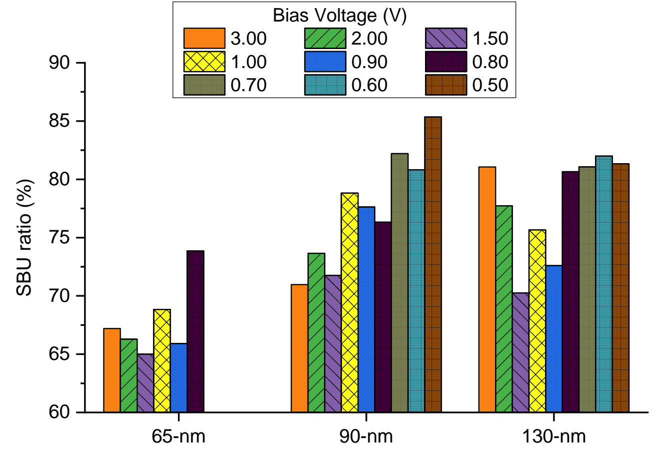

Fig. 5. SBU contribution in total number of bitflips

For all three memories the plots also include theoretical cross-section predictions issued by the MUSCA-SEP3. It was used to predict SBUs and 2-bit MCUs cross-sections at various VDDs showing similar behavior with the actual results. Simulation results also clearly show the difference in the SBU/MCU sensitivities for proton and neutron irradiation.

Next, Fig. 5 shows the ratio of the SBU contribution with respect to the total number of bitflips in the experiments carried out with these devices. It can be noted that the 65-nm one has the lowest SBU contribution to the total number of bitflips. At the nominal bias voltages (3.00 V), the SBU rates increase for larger technologies which is in agreement with previous studies [13], [32]. However, these devices show different behaviours at lower voltages. For the 90-nm SRAM, lowering the voltage increases the SBU rate, while the 65-nm and the 130-nm devices exhibit fluctuations not seen in the 90-nm device. Authors believe that these devices undergo parasitic bipolar effect as described in [33].

B. About the Shape of the Multiple Events

Even if Figs. 3 and 4 show a similar SEU cross-section for the 65-nm and 90-nm memories under 15 MeV protons, they exhibit differences in other aspects. The most important one is the appearance of micro-latchups in the 90-nm memory on lower voltages. Above that, there is a significant difference in the shape of 2-bit MCUs in the 65-nm memory with the two other devices, which is presented in Fig. 6. Using the data provided by the manufacturer, the actual shape of the 2-bit MCUs was driven through the raw results considering the Manhattan distance less than or equal to 3. Fig. 6 shows the 2-bit MCU shapes for the 65-nm (a), 90-nm (b) and 130-nm (c)

memories. With the mentioned Manhattan distance, these 2-bit MCUs can be vertical (V1-V3, depending on the distance between the involved bitcells), horizontal (H1-H3), diagonal (D) or Knight-Jump (chess game) L-shapes (KJ1-KJ4).

Vertical shapes are clearly the dominant ones in the 65-nm memory, representing more than 99% for this device. This would prevent MBUs to occur in this device even if words were organized by rows without bit interleaving. For the 90-nm and 130-nm devices, shapes are vividly different compared to the 65-nm one. The 90-nm memory has mostly horizontal shapes in all the voltages while the 130-nm has both vertical and horizontal shapes with similar abundances.

The significant difference observed between the 130&90-nm devices and the 65-nm one is attributed to a drastic change in the design of the bitcell topology, from a so-called "tall" design to a "wide" one [34]. The "tall" cell was classically used until the 90-nm technological node, but the "wide" one was adopted to alleviate process difficulties [35], for the 65-nm technological node and subsequent ones [36]. The latter improves critical dimension control and variation by aligning the polysilicon in a single direction, therefore eliminating diffusion corners and relaxing some patterning constraints on other critical layers. A detailed analysis of this point has been recently made by the authors with MUSCA-SEP3 simulations [37], hence it will not be discussed in depth in this paper. The interesting point here is to observe that the trends for low V_{CC} are very similar for protons (Fig. 6) and for neutrons (Fig. 4 in [13], which was the first time this abrupt change was noticed between devices (a) and (b)).

C. Future Technological Trends and MUSCA-SEP3 Simulations

As previously shown in Fig. 4, MUSCA-SEP3 is able to provide a precise prediction of different build technologies at various bias voltages. To have a better comparison of the sensitivity of the available SRAM technology nodes, the authors used MUSCA-SEP3 to simulate 7 additional bulk CMOS manufacturing technologies in the ITRS/IRDS roadmap (from 150-nm to 45-nm), at several bias voltages. A bit-cells' floorplan was defined (11×11) to take into account multiple events. Fig. 7 shows the results of the simulations for (a) proton SBU, (b) neutron SBU, (c) proton 2-bit MCU and (d) neutron 2-bit MCU cross sections at 5 levels of bias voltage. It is important to note that since the internal design of these devices had a shift between the 90-nm and 65-nm memories, the lines in all the plots are disconnected between these two points.

The SBU cross-section for both irradiation sources (Figs. 7(a) and 7(b)) constantly increases for all build technologies when the bias voltage is reduced. This is well known, as shown in several previous works [12], [13], [22]. For most of the bias voltages, especially the lowest ones, the cross-sections decrease with smaller built technologies. For both "tall" and "wide" technologies, it can be seen that smaller build sizes have lower SBU cross-sections compared to their ancestors except for the 130-nm memory. Smaller build technologies also show less sensitivity to the DVS as the gap between the cross-section lines is increasingly narrower.

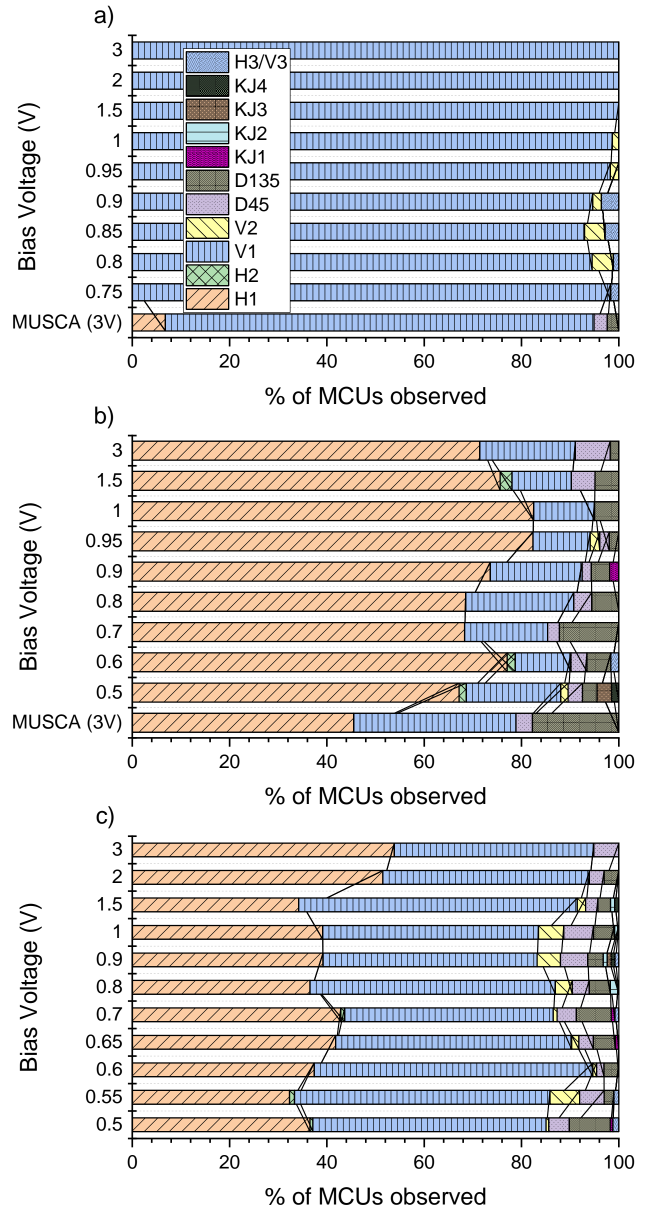

Fig. 6. 2-bit MCU shapes for the 65-nm (a), 90-nm (b) and 130-nm (c) memories

The 2-bit MCU cross-sections, putting DVS into effect, shows distinct behaviours considering the "tall" and "wide" build technologies. Results are also different from their SBU counterparts, especially for the build sizes below 65-nm (i.e., the "wide" ones). For both irradiation sources, the behaviors for "tall" and "wide" builds are different. While the neutron cross-sections follow "more or less" a flat trend for "tall" nodes for most voltages, the 2-bit MCU cross-sections increase when reducing the build size for the "wide" nodes. This difference is more extreme for the proton radiation. Thus, whereas the cross-sections undergo a drastic drop at lower voltages from the 110-nm to the 90-nm "tall" nodes, numbers are mostly growing for the "wide" ones.

Comparing the plots in Figs. 7.c) and 7.d) (MCU sensitivity for protons vs. neutrons), one can observe an unequal

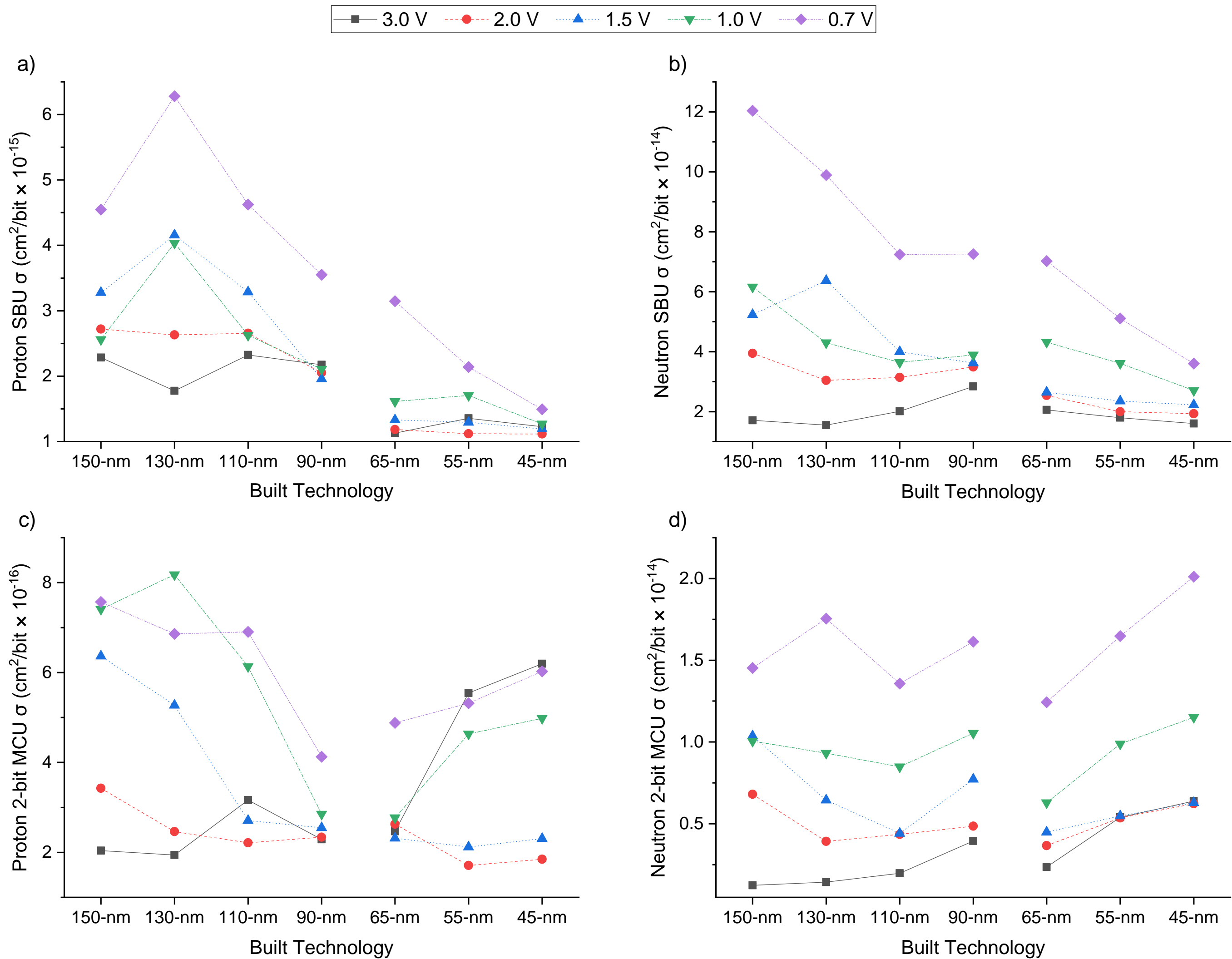

Fig. 7. Trends for (a) proton SBU, (b) neutron SBU, (c) proton 2-bit MCU and (d) neutron 2-bit MCU cross sections using MUSCA-SEP3 simulations at various voltages for several build technologies

evolution for said sensitivity in both cases. Thus, for the "tall" nodes, there is a notable difference comparing both irradiation sources. MCU cross-sections mostly decrease for protons, but this is not the case for neutrons, where they are mostly flat, with some fluctuations. However, both irradiation sources seem to affect the "wide" nodes in a similar way: in this case, cross-sections constantly increase as the build technology is miniaturized, which is the opposite behavior than the observed in Figs. 7.a) and 7.b). Therefore, for more modern "wide" nodes, DVS seems to have an increasingly higher effect on the appearance of multiple events, but increasingly less effect on the appearance of SBUs.

From the point of view of simulations, the SEE occurrence depends on two ambivalent factors: the technological intrinsic sensitivity (i.e., the critical charge) and the dimensions of the zone of sensitivity. It is therefore not easy to foreshadow trends. In the case of neutrons, the results are quite consistent since they show a decrease in SBUs and an increase in MCUs. In the case of protons, it is surprising to observe a decrease in the contribution of MCUs up to 90-nm and then an increase (Fig. 7.c). It can be assumed that the design change (from “tall” to “wide”) contributes to this behavior; however, the contribution of the direct ionization of protons is also possible. Indeed, from technological nodes 90-nm to 65-nm, the direct ionization of protons can play an important role in the SEE occurrences.

V. Conclusions

Experimental proof of the impact of DVS on the sensitivity of 3 successive COTS Cypress bulk SRAMs and 2 A-LPSRAMs manufactured by Renesas Electronics is presented in this paper. The experiments were performed at low bias voltage, extending previous studies and help to gain a better understanding on the observed outcomes. Results are also in agreement with MUSCA-SEP3 predictions. SBUs, MCUs, micro-latchups (for the 90-nm Cypress memory), SEFIs and low voltage stuck-bits (for the Renesas memories) have been observed. Shapes of 2-bit MCUs were extracted and showed that the 65-nm device has only vertical shapes while the two other devices observed various shapes due to an important

modification in cells built technology from "tall" to "wide" . A full comparison based on build technology at low voltages has also been provided by the MUSCA-SEP3 predictions, showing that while this change in the built technology decreases the SBU cross-sections for both protons and neutrons, the MCU cross-sections increase especially with neutron irradiation source.

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