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Interfacial State Density and Conductance-Transient Three-Dimensional Profiling of Disordered-Induced Gap States on Metal Insulator Semiconductor Capacitors Fabricated from Electron-Cyclotron Resonance Plasma-Enhanced Chemical Vapor Deposited $SiO_xN_yH_z$ Films

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An electrical characterization of $Al/SiO_xN_yH_z/Si$ metal–insulator–semiconductor (MIS) structures has been carried out. $SiO_xN_yH_z$ films of different compositions have been obtained from these structures by varying gas flow in the electron-cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD) system. The presence of nitrogen in the films increases the dielectric constant value and degrades the interface quality, as our measurements demonstrate. The effect of thermal annealing has also been determined. Capacitance–voltage (C–V) results show that unannealed samples exhibit positive flat-band voltages, whereas annealed ones exhibit negative values. On the other hand, from deep-level transient spectroscopy (DLTS) measurements we can conclude that interfacial state density diminishes when thermal treatments are applied. Moreover, conductance transient analysis provides the energetic and spatial distribution of defects in the films and demonstrates that thermal improvement affects not only the interface, but also the insulator bulk.
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1. Introduction

Silicon oxynitride ($SiO_xN_yH_z$) is a very promising material for the microelectronic industry as it shows some advantages with respect to the widely used SiO_2 (better impermeability to boron atom diffusion and alkali ions, higher reliability and higher dielectric constant[1)]) and SiN_x:H (lower stress, higher band gap and better electrical characteristics[2)]). Additionally, silicon oxynitride allows applications such as graded index films.[3)]

Different techniques are available for the deposition of $SiO_xN_yH_z$ films. The electron-cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD) method is very valuable because it is a low cost thermal process and the substrate is placed outside the plasma region, reducing the damage induced by ion bombardment.[4)] A very high activation of the precursor gases can be achieved, allowing the use of N_2 instead of NH_3 as the N atom source, which results in lower incorporation of hydrogen into the films.[5,6)]

The aim of this work is to carry out an electrical characterization of $Al/SiO_xN_yH_z/Si$ MIS structures, from which $SiO_xN_yH_z$ films of different compositions have been obtained by varying gas flow in the ECR-PECVD system. The influence of conventional furnace-thermal treatments applied after metallization is also investigated.

2. Experimental

Metal–insulator–semiconductor (MIS) devices were obtained as follows: substrates used were n-Si (5 Ωcm, ⟨100⟩ orientation), on which we have previously deposited Al back electrodes by thermal evaporation. Cleaning of the substrates was performed using standard chemical procedures starting with dipping into acetone and methanol followed by drying with nitrogen. Then silicon was successively subjected to the following cleaning steps: dipped in $NH_4OH : H_2O_2 : H_2O$ (1 : 2 : 5) solution for 5 min, rinsed with deionized H_2O, dipped in $HF : H_2O$ (1 : 10) solution for 1 min and then rinsed with deionized H_2O. Finally the substrates were blown dry again with nitrogen.

Then, we deposited a layer of $SiO_xN_yH_z$ by using an Astex ECR plasma source model AX4500. Precursor gases are N_2, O_2 and SiH_4. The oxygen plus nitrogen flows to silane flow ratio was kept constant: $R = (\Phi(O_2) + \Phi(N_2))/\Phi(SiH_4) = 5$. However, the oxygen to silane ratio, $Q = \Phi(O_2)/\Phi(SiH_4)$, was varied between 5 and 0 in order to obtain compositions similar to those of silicon oxide and silicon nitride, respectively. Film thickness was varied between 1028 Å (corresponding to $Q = 0$) and 1246 Å (corresponding to $Q = 5.0$). Intermediate values are: 1162 Å ($Q = 0.41$), 1237 Å ($Q = 0.61$) and 1272 Å ($Q = 0.95$). The parameter R determines the silane partial pressure during deposition and, therefore, silicon is incorporated into the samples, while Q controls the amount of oxygen in the films. During the deposition process, reactions to incorporate oxygen and nitrogen into the film are competitive, and the oxygen reaction takes preference. For high values of Q ($Q > 2.5$), all the silane reacts with the O_2, despite the presence of N_2 in the plasma and SiO_2 composition is obtained. However, for lower Q values, there is remaining SiH_4 which reacts with nitrogen, and intermediate oxynitride compositions are obtained.[7,8)] The dielectric constant value diminishes from $\varepsilon_r = 6.4$ (corresponding to $Q = 0$) to $\varepsilon_r = 3.8$ (corresponding to $Q = 5$). In all the ECR-PECVD depositions, chamber pressure and substrate temperature were kept at 100 W and 200°C, respectively. Al dots ($1.24 \times 10^{-3}\,cm^{-2}$) were thermally evaporated through a shadow mask as gate electrodes. Finally, in some cases, we applied thermal annealing in argon atmosphere at 300°C for 20 min in order to determine the influence of thermal treatments on the structure quality.

To study the interface quality of MIS structures, we applied the following techniques: capacitance–voltage (C–V), deep-level transient spectroscopy (DLTS) and conductance transient analysis.

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C–V measurements were carried out at room temperature and at 77 K with the sample in a light-tight, electrically shielded box. The measurement setup involved a 1 MHz Boonton 72B capacitance meter and a Keithley 617 programmable electrometer. Both room-temperature and 77 K *C–V* curves obtained for all the samples clearly exhibit hysteresis phenomena, thus indicating that the interface state distribution follows the well-known disorder-induced gap-state (DIGS) model.[9,10] According to this model, interface states are distributed both in energy and in space. Emission and capture of free electrons by states located in the insulator far from the interface can occur by means of tunneling mechanisms. As emission and capture kinetics are slow and nonsymmetrical, the capacitance value depends on both the direction and the speed of the voltage variation and, thus, hysteresis effects are observed, as shown in Fig. 1 for the $Q = 0.41$, unannealed sample.

DLTS measurements between 77 and 300 K were carried out using a 1 MHz Boonton 72B capacitance meter and an HP54501 digital oscilloscope to record the capacitance transients. A Keithley 617 programmable electrometer is used together with a HP214B pulse generator to introduce the quiescent bias and the filling pulse, respectively. To obtain the interface trap distribution within the forbidden gap, the bias voltage is chosen so that the MIS capacitor is just at the limit between depletion and weak inversion. Also, a 200-μs-wide pulse high enough to drive the capacitors into accumulation is applied in order to fill all interface traps. The interface trap distribution was deduced from DLTS measurements by means of the expressions reported elsewhere.[11]

Moreover, we recorded conductance transients, which provide quantitative information about the disordered-induced gap states. As we have published elsewhere,[12–14] from the experimental conductance transients measured at different frequencies and at different temperatures, we can obtain the DIGS density as a function of the spatial distance to the interface and of the energy position. The experimental setup consists of the HP 33120A arbitrary waveform generator to apply the bias pulse and the EG&G 5206 two-phase lock-in analyzer to measure the conductance. An HP 54501A digitizing oscilloscope records the complete conductance transient. Samples were cooled in darkness from room temperature to 77 K at 0 bias in an Oxford DN1710 cryostat. An Oxford ITC 502 controller was used to keep the temperature constant during the measurements.

3. Results and Discussion

From *C–V* measurements, we observe that unannealed samples exhibit a positive flat-band voltage, whereas annealed structures show negative values, as shown in Fig. 2 for the $Q = 0.41$ samples. Positive flat-band voltage means negative trapped charge in the insulator. Indeed, for the unannealed $Q = 0.41$ sample shown in the figure ($V_{FB} \approx +2.5$ V) we can estimate a charge density $Q_{insulator} \approx -6.9 \times 10^{11}\,cm^{-2}$, and for the other Q values charge densities vary between -5×10^{11} and $-20 \times 10^{11}\,cm^{-2}$. We can expect that the dominant defects in the insulator bulk are dangling bonds: $N_3 \equiv Si \uparrow$ (K center) and $O_3 \equiv Si \uparrow$ (E′ center), which are more stable in the negative state that in the neutral state. Thermal annealing induces the negative charge removal, which is possibly due to the hydrogen passivation of dangling bonds.

DLTS provides the profiles of the interface state density as a function of the energy level measured from the bottom of the silicon conductance band ($E_C - E_T$). Figure 3(a) shows DLTS profiles corresponding to $Q = 0$, $Q = 0.41$ and $Q = 0.61$ unannealed samples. The same trend is obtained for annealed samples, so we can conclude that interfacial state density for compositions similar to those of SiN_x is higher than for compositions similar to those of SiO_x. The more common interface defects are in the bond stretching model suggested by Sakurai and Sugano.[15] By considering an idealized tight-binding model for silicon and a Bethe lattice for SiO_2, they found that stretched bonds Si–Si and dangling defects $Si_3 \equiv Si \uparrow$, in which oxygen and nitrogen atoms are involved, cause defect levels in the upper half of the band gap at the interface. On the other hand, thermal treatments significantly reduce D_{it}, as shown in Fig. 3(b) for the $Q = 0$ samples, although the same is obtained for the other Q values. This finding can be explained by taking into account the fact that when thermal treatments are applied, a relaxation process including hydrogen passivation of defects is produced. Indeed, from Fourier transform infrared spectroscopy (FTIR) and elastic recoil detection analysis (ERDA) measurements we have determined the contents of N–H bonds and unbonded H atoms[7,8] in our deposited films. ERDA composition analyses provide us with the total

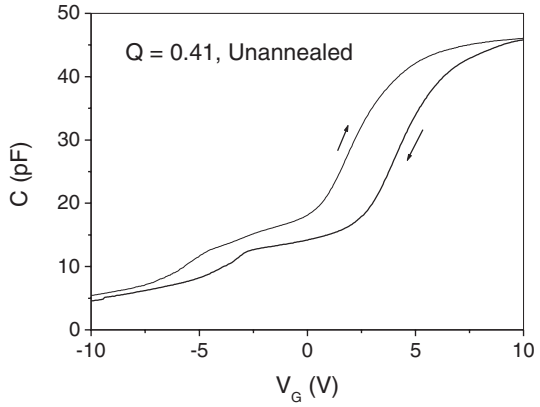

Fig. 1. 1 MHz and room-temperature *C–V* curves corresponding to $Q = 0.41$, unannealed sample. Hysteresis effect is clearly shown.

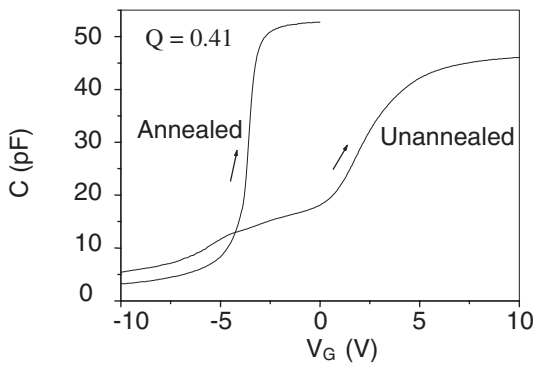

Fig. 2. 1 MHz and room-temperature *C–V* curves corresponding to $Q = 0.41$, unannealed and annealed samples. Film thickness is 1162 Å.

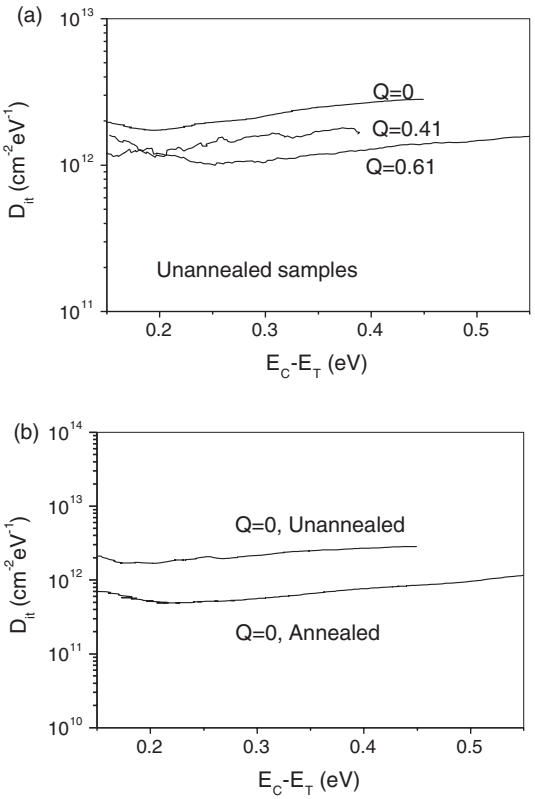

Fig. 3. Interfacial state density measured by using DLTS for different insulator compositions (a) and as a function of thermal treatment (b).

hydrogen content in the films, $[H_{TOTAL}]$. On the other hand, the FTIR measurements do not detect any Si–H and O–H bonds. To determine the actual concentrations of N–H bonds and unbounded H atoms we proceed as follows: The N–H concentration is proportional to the nitrogen content, $[N–H] = X_{NH}[N]$. X_{NH} can be easily calculated taking into account the coordination numbers of Si, O and N and assuming that only Si–O, Si–N and N–H bonds are present in the films. This calculation yields a value of $X_{NH} = 0.21$. Then, from the nitrogen content, the N–H bond concentration is derived. Finally, unbonded H atom concentration can be calculated by subtracting the total hydrogen concentration from the N–H bond concentration: $[\text{unbounded H}] = [H_{TOTAL}]-[N–H]$. This concentration is calculated to be about 30% of the total hydrogen content. We obtain these concentrations for all the unannealed films. The unbonded hydrogen concentration varies from $3.19 \times 10^{21}\,cm^{-3}$ for $Q = 0$ films (SiN_y) to 0 for $Q = 5$ films (SiO_x). Intermediate values are: $2.6 \times 10^{21}\,cm^{-3}$ for $Q = 0.41$, $1.9 \times 10^{21}\,cm^{-3}$ for $Q = 0.61$ and $0.21 \times 10^{21}\,cm^{-3}$ for $Q = 0.95$.

Moreover, conductance transient measurements provide us with three-dimensional defect maps. As we mentioned above, hysteresis effects in C–V curves indicate that there are disordered-induced gap states at the insulator/semiconductor interface, i.e., defects that are distributed away from the interface toward the insulator. Conductance transients are obtained by applying bias pulses that drive MIS structures from deep to weak inversion. Subsequently, a capture process takes place in which the empty DIGS trap electrons coming from the semiconductor conduction band. This process is assisted by tunneling and is time consuming: states near the interface capture carriers before capturing those located farther away in the dielectric bulk. Because this process is time consuming, these defects are usually called "slow traps". Defects located in the semiconductor respond instantaneously to the bias pulse and, therefore, do not affect the conductance transient. The conductance transient shape varies significantly with the frequency because only those traps with emission and capture rates of the same order of magnitude as the frequency make non-zero contributions to the conductance. When the states are spatially distributed, the emission and capture processes involve both thermal excitation and tunneling. Besides, as temperature decreases the transients are modified in a similar way as when frequency is increased at a constant temperature: the lower the temperature is, the faster the transients become. This is easily explained by taking into account the fact that the emission rate is a function of the temperature: as temperature decreases the emission rates of all DIGS states exponentially decrease, the equi-emission lines shift toward the interface and shorter distances have to be covered by tunnelling electrons. As has been discussed elsewhere,[12] only decreasing transients provide reliable information about the DIGS profile.

Figure 4 shows the DIGS distribution obtained for annealed samples of different compositions: $Q = 0$ (a) and $Q = 0.95$ (b). Negative $E_C - E$ values indicate energy positions located in the silicon conduction band, whereas

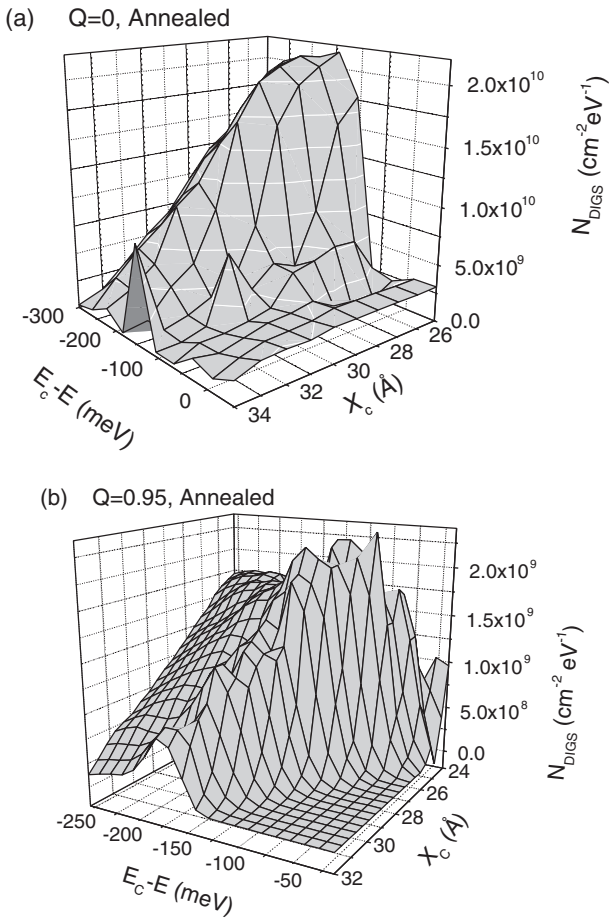

Fig. 4. Three-dimensional DIGS profile of annealed samples: (a) $Q = 0$ and (b) $Q = 0.95$.

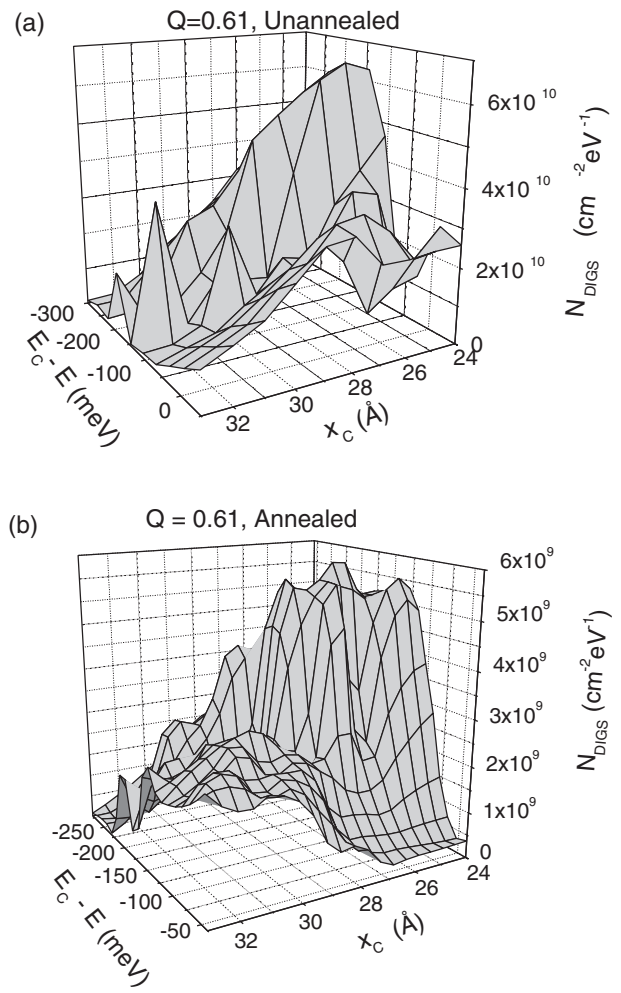

Fig. 5. Three-dimensional DIGS profile of $Q = 0.61$ samples: (a) unannealed and (b) annealed.

positive values correspond to band gap positions. x_c is the spatial distance to the interface. We can see that there are DIGS defects up to depths of around 35 Å into the insulator bulk, and they show a maximum for energies 150 meV above the silicon conductance band edge. However, DIGS density clearly depends on insulator composition: it is almost one order of magnitude higher for $Q = 0$ than for $Q = 0.95$. Similar behaviour is observed in the whole set of samples, so we can conclude that DIGS density rises when nitrogen content increases.

Figure 5 illustrates the annealing effect in the DIGS density for the $Q = 0.61$ case. We can see that for the unannealed sample (a) the damage profile is wrinkled and deeper than for the annealed one (b). Also, the DIGS maximum is one order of magnitude higher for the unannealed sample than for the annealed one. Similar results are obtained for the whole set of samples, so we can conclude that thermal annealing diminishes DIGS density.

4. Conclusions

An electrical characterization of $SiO_xN_yH_z$ films of different compositions reveals that the presence of N increases the dielectric constant value and degrades the interface quality. However, thermal treatments induce defect passivation, which is possibly related to the presence of hydrogen in the films. Conductance transient analysis, which provides a complete picture of DIGS distribution, demonstrates that this improvement affects not only the interface, but also the insulator bulk. This kind of analysis has proven to be very valuable in the field of high dielectric constant materials.

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