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## Electrical Characterization of Low Nitrogen Content Plasma Deposited and Rapid Thermal Annealed Al/SiN<sub>x</sub>:H/InP Metal-Insulator-Semiconductor Structures

Helena CASTÁN\*, Salvador DUEÑAS, Juan BARBOLLA, Estefanía REDONDO<sup>1</sup>,  
Ignacio MÁRTIL<sup>1</sup> and Germán GONZÁLEZ-DÍAZ<sup>1</sup>

*Departamento de Electricidad y Electrónica, E.T.S.I. Telecomunicación, Campus "Miguel Delibes",  
Universidad de Valladolid, 47011 Valladolid, Spain*

<sup>1</sup>*Departamento de Física Aplicada III (Electricidad y Electrónica), Facultad de Ciencias Físicas,  
Universidad Complutense, 28040 Madrid, Spain*

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The influence of the dielectric composition and post deposition rapid thermal annealing (RTA) treatments on the electrical characteristics of low nitrogen content plasma-deposited Al/SiN<sub>x</sub>:H/InP structures were analyzed. To obtain the interface state density, deep level transient spectroscopy (DLTS) measurements were carried out. We have also evaluated the insulator damage density, the so-called disorder-induced gap states (DIGS), by means of conductance transient analysis. As for the dielectric composition, both the  $x = 0.97$  and  $x = 1.43$  values provide interfacial state density and DIGS damage values of the same order of magnitude. In the  $x = 0.97$  case, RTA treatments reduce the insulator damage moving it towards the interface. In the  $x = 1.43$  case this behavior is only observed for RTA temperatures lower than 500°C. So, moderate temperature (<500°C) RTA treatments improve DIGS damage. This is an important result in terms of fabricating bi-layered metal-insulator-semiconductor (MIS) structures that not only have good-quality interfaces, but also good dielectric properties.

**KEYWORDS:** interface states, insulator damage, InP, plasma deposition, RTA, MIS, DLTS, conductance transients

### 1. Introduction

The fabrication of InP-based metal-insulator-semiconductor (MIS) structures is difficult because the surface of this material is very fragile and reactive and it is easily oxidized with a layer of native oxide which is very unstable and generally very conductive, showing a high interface state density.<sup>1)</sup> In addition, phosphorous has a low vapor pressure, so it can easily escape from the semiconductor lattice. Therefore, it is necessary to use a low-temperature insulator deposition technique that minimizes the semiconductor surface degradation. The choice of the insulator is also an important issue. In this sense amorphous silicon-nitrogen alloys are adequate for use as the gate dielectric in MIS field effect transistors (MISFETs), in which charge trapping must be minimized to avoid Fermi level pinning.<sup>2)</sup> It has been shown that electron cyclotron resonance plasma enhanced chemical vapor deposition (ECR-CVD) is a suitable technique for silicon nitride film deposition on InP because it allows a low substrate temperature.<sup>3)</sup> Also, because of the moderate energy of the ions, good-quality insulator-semiconductor interface can be obtained. However, silicon nitride films deposited by plasma-assisted processes have a moderate to high H-concentration, so they must be referred to as SiN<sub>x</sub>:H. On the other hand, rapid thermal annealing (RTA) is a very well-controlled heating process that is conventionally used after ion implantation in order to recover the surface crystallinity and to electrically activate the implanted atoms, and thermal relaxation and reconstruction of the SiN<sub>x</sub>:H lattice can also be induced.<sup>4)</sup>

In previous works<sup>5,6)</sup> we investigated the influence of nitrogen content on the quality of ECR-CVD SiN<sub>x</sub>:H/InP structures, and we observed that when the nitrogen content increased the density of interface traps decreased. However, when the nitrogen content decreased below a certain value (approx.  $x = 1.4$ ) the dielectric behavior was improved. Our conclusion was that although a high nitrogen content insulator

favors a low interfacial trap density, the electrical properties are simultaneously degraded. A reverse behavior is detected for insulator layers of low nitrogen content, where the electrical properties are improved, but the interfacial trap density is increased.

To clarify these behaviors, we fabricated<sup>7–10)</sup> MIS structures based on a bi-layered gate insulator structure, with a different composition and thickness for each layer (a N-rich bottom layer with  $x = 1.55$  and a N-poor top layer with  $x = 1.43$ , and 100 or 50 Å for the bottom layer and 400 or 150 Å for the top layer, respectively). The role of the bottom layer is to control the interfacial trap density, whereas the role of the thicker top layer is to provide good dielectric properties such as breakdown electric field and resistivity. We have demonstrated that these bi-layered structures show improvement in both their interface trap density and in their electrical properties.<sup>9,10)</sup> Regarding RTA treatment, we have experimentally proved that N-rich MIS structures ( $x = 1.55$ ) submitted to moderate temperature (400–500°C) RTA treatments show improvement in their interface trap density. However, the interfacial damage increased for the samples annealed at temperatures higher than 500°C. This was explained as follows: for the lower annealing temperatures, below 500°C, nitrogen atoms coming from the insulator may occupy phosphorous vacancies,  $V_P$ . Thus, the interfacial state density decreases due to the effective  $V_P$  passivation.<sup>5,6,9)</sup> At annealing temperatures higher than 500°C, the nitrogen loss from the  $V_P$  dominates, decreasing the passivation and, as a result, the interface trap density increases. Also, we have demonstrated that moderate temperature RTA improves interfacial state density in bi-layered MIS structures.<sup>9,10)</sup>

To complete the above-mentioned course of study, in this paper we analyse the influence of dielectric composition and post deposition RTA temperature on the electrical characteristics of low nitrogen content ECR-CV deposited silicon nitride Al/SiN<sub>x</sub>:H/InP MIS structures.

\*E-mail: helena@ele.uva.es

## 2. Experimental

### 2.1 Sample description

Substrates used were undoped (100) n-type InP fabricated by a liquid encapsulated Czochralski (LEC) process, with an unintentional dopant concentration of  $5 \times 10^{15} \text{ cm}^{-3}$ . The MIS structures were fabricated by directly depositing silicon nitride films on InP wafers by the ECR plasma method. Gases employed in the insulator deposition vacuum chamber were  $\text{N}_2$  and pure  $\text{SiH}_4$ , with two different values of the gas flux ratio,  $R = [\text{N}_2]/[\text{SiH}_4]$ ,  $R = 1$  ( $x = 0.97$ ) and  $R = 1.6$  ( $x = 1.43$ ). Substrates were heated to  $200^\circ\text{C}$ , and a total pressure of 0.6 mTorr was kept constant during the deposition process. The microwave power was also kept constant at 100 W. Prior to the dielectric deposition, the wafers were cleaned with organic solvents, etched for 1 min in  $\text{HIO}_3 : \text{H}_2\text{O}$  (10 wt%) and immersed in  $\text{HF} : \text{H}_2\text{O}$  (1 : 10) for 15 s to strip the native oxides. Finally, the samples were rinsed in deionized water and dried in  $\text{N}_2$ .

To study the effect of RTA temperature on the interface quality,  $\text{SiN}_x\text{:H/InP}$  samples were submitted to argon-atmosphere RTA processes for 30 s at temperatures varying between 400 and  $700^\circ\text{C}$ . One sample of each type ( $x = 0.97$  and  $x = 1.43$ ) was left un-annealed to be used as a control.

Al dots ( $1.12 \times 10^{-3} \text{ cm}^{-2}$ ) were then thermally evaporated through a shadow mask as gate electrodes. Finally, an AuGe/Au back electrode was evaporated. A postmetallization annealing was performed in Ar atmosphere ( $300^\circ\text{C}/20 \text{ min}$ ).

### 2.2 Electrical characterization

To study the interface quality of MIS structures, we have applied the following techniques: capacitance–voltage ( $C$ – $V$ ), deep-level transient spectroscopy (DLTS) and conductance transient analysis.

$C$ – $V$  measurements were carried out at room temperature and at a temperature of 78 K, with the sample placed in a light-tight, electrically shielded box. The measurement setup involved a 1 MHz Boonton 72B capacitance meter and a Keithley 617 programmable electrometer. The measurement run was computer controlled. The  $C$ – $V$  curves obtained at 78 K show a lower flat band voltage displacement and stretch-out than the room-temperature  $C$ – $V$  curves, indicating that some traps in the material are frozen at low temperatures. However, both the room-temperature and 78 K  $C$ – $V$  curves obtained for all the samples clearly exhibit hysteresis phenomena, indicating that interface state distribution follows the well-known disorder-induced gap-state (DIGS) model.<sup>11,12</sup> According to this model, interface states are distributed in both energy and space. The spatial extension of the disordered semiconductor region is very narrow, typically 1 to 3 monolayers. On the other hand, the disordered insulator region reaches more than  $100 \text{ \AA}$ . The emission and capture of free electrons by states located in the insulator far from the interface can occur by means of tunnelling mechanisms. As emission and capture kinetics are slow and not symmetrical, the capacitance value depends on both the direction and the speed of the voltage variation and, thus, hysteresis effects are observed.

DLTS measurements between 78 and 300 K were carried out using the same 1 MHz Boonton 72B capacitance meter and an HP54501 digital oscilloscope to record the ca-

pacitance transients. In these experiments, the Keithley 617 programmable electrometer is used together with a HP214B pulse generator to introduce the quiescent bias and the filling pulse, respectively. To obtain the interface trap distribution within the forbidden gap, the bias voltage is chosen so that the MIS capacitor is exactly at the limit between depletion and weak inversion. Also, a  $200\text{-}\mu\text{s}$ -wide pulse sufficiently high to drive the capacitors into accumulation is applied in order to fill all interface traps. The interface trap distribution ( $D_{\text{it}}$ ) was deduced from DLTS measurements by means of the expressions reported elsewhere<sup>13</sup> using an energy-independent capture cross-section value of  $\sigma_n = 1 \times 10^{14} \text{ cm}^2$ , which is typically found in III–V semiconductor-based MIS structures.<sup>14</sup>

We have measured the conductance transients which provide quantitative information about the disordered induced-damage states.<sup>15</sup> As has been published elsewhere,<sup>16,17</sup> from the experimental conductance transient,  $G(t)$ , we can obtain the DIGS state density ( $N_{\text{DIGS}}$ ) as a function of the spatial distance to the interface ( $x_c$ ) and of the energy position, as follows:

$$N_{\text{DIGS}} = \frac{\Delta G / \omega}{0.4qA} \quad (1)$$

$$x_c(t) = x_{\text{on}} \ln(\sigma_0 v_{\text{th}} n_s t) \quad (2)$$

$$E' - E(x_c, t) = H_{\text{eff}} + kT \ln \left( \frac{\sigma_0 v_{\text{th}} N_c}{\omega / 1.98} \right) - kT \frac{x_c(t)}{x_{\text{on}}}, \quad (3)$$

where  $x_{\text{on}} = \hbar / [2(2m_{\text{eff}} H_{\text{eff}})^{1/2}]$  is the tunnelling decay length,  $\sigma_0$  is the carrier capture cross-section value for  $x = 0$ ,  $v_{\text{th}}$  is the carrier thermal velocity in the semiconductor, and  $n_s$  is the free carrier density at the interface. Finally,  $H_{\text{eff}}$  is the insulator-semiconductor energy barrier for minority carriers and  $E'$  indicates the carrier energy band edge at the insulator ( $E'_c$  for electrons and  $E'_v$  for holes).

## 3. Results and Discussion

### 3.1 Al/SiN<sub>0.97</sub>:H/InP structures

Regarding to the influence of the RTA temperature on the interface quality, we have studied Al/SiN<sub>0.97</sub>:H/InP structures un-annealed and RT-annealed at different temperatures (400, 500, 600 and  $700^\circ\text{C}$ ). However, we must point out that, according to ref. 18, samples with  $x = 0.97$  and  $x = 1.43$  submitted to RTA at  $700^\circ\text{C}$  undergo an important release of nitrogen, and then a decrease in the nitrogen to silicon ratio,  $x$ , results. Because of this change in the dielectric composition, we must take care with the results corresponding to the RTA temperature of  $700^\circ\text{C}$ .

Figure 1 shows the interface trap distribution obtained by DLTS in Al/SiN<sub>0.97</sub>:H/InP structures. It appears that RTA treatments degrade the insulator-semiconductor interface. In previous works<sup>7–10</sup> we reported an interface state density decrease for moderate RTA temperatures, because nitrogen atoms fill some phosphorous vacancies. But in that study the nitrogen content of the dielectric composition ( $x = 1.55$ ) was higher than in the present case, so we can conclude that a value of  $x = 0.97$  is not sufficiently high for RTA to anneal the interface. Moreover, in this study we have carried out transient conductance measurements that provide complementary information. In Fig. 2 we have plotted conductance transients [Fig. 2(a)] and DIGS damage density as a function of the distance from the interface and of the energy position

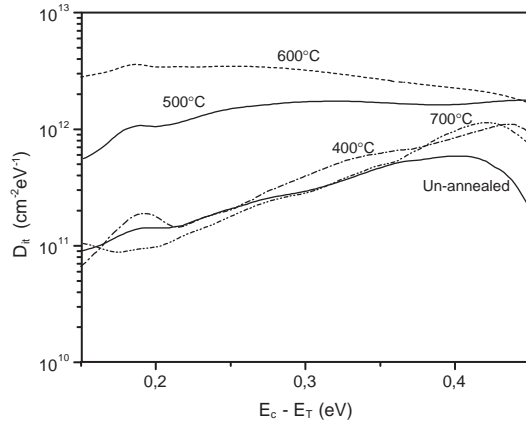


Fig. 1. Interfacial state density measured by DLTS in Al/SiN<sub>0.97</sub>:H/InP MIS structures at different RTA temperatures.

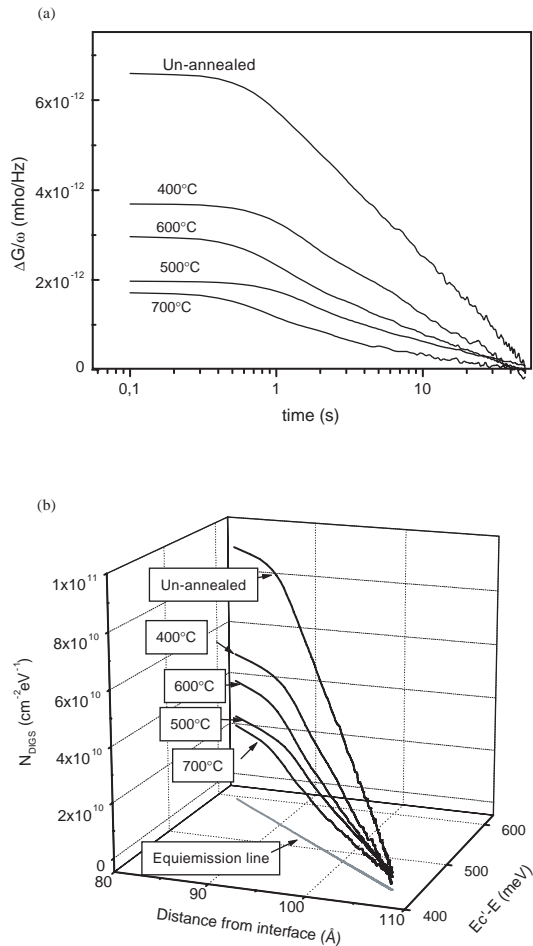


Fig. 2. Induced damage in Al/SiN<sub>0.97</sub>:H/InP MIS structures at different RTA temperatures. (a) Room-temperature 200-KHz conductance transients. (b) DIGS damage density.

measured from the insulator conduction band edge [Fig. 2(b)] corresponding to Al/SiN<sub>0.97</sub>:H/InP samples. According to this figure, DIGS damage diminishes somewhat when annealing temperature is increased. Therefore, we can conclude that RTA treatments move the insulator damage towards the interface.

In summary, the DIGS damage evolution with RTA temperature is exactly the opposite of that interfacial state den-

sity. This behavior suggests some temperature activated defect exchange between the insulator and the interface; this has previously been observed by us in Al/SiN<sub>x</sub>:H/In<sub>0.53</sub>Ga<sub>0.47</sub>As structures.<sup>19)</sup>

### 3.2 Al/SiN<sub>1.43</sub>:H/InP structures

Figure 3 shows the interface trap distribution obtained by DLTS in Al/SiN<sub>1.43</sub>:H/InP structures, un-annealed and RT-

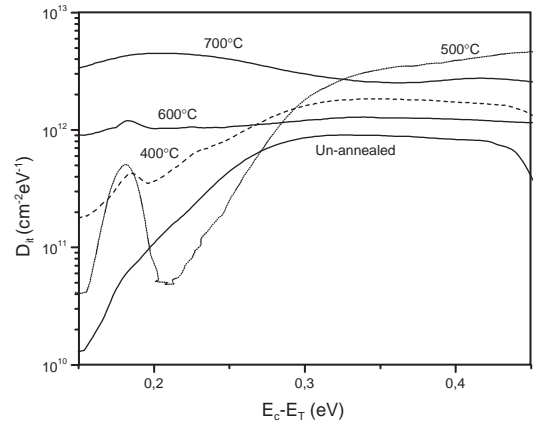


Fig. 3. Interfacial state density measured by DLTS in Al/SiN<sub>1.43</sub>:H/InP MIS structures at different RTA temperatures.

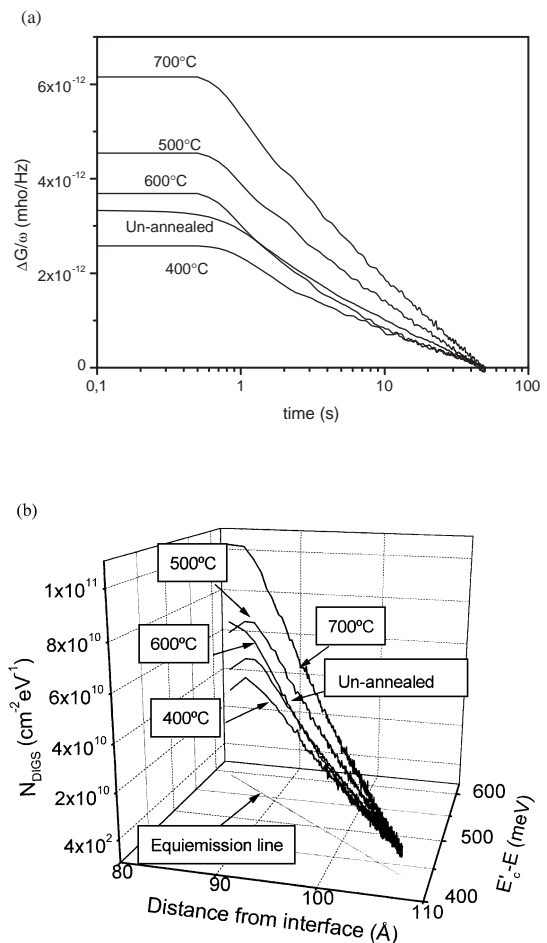


Fig. 4. Induced damage in Al/SiN<sub>1.43</sub>:H/InP MIS structures at different RTA temperatures. (a) Room-temperature 200-KHz conductance transients. (b) DIGS damage density.

annealed at different temperatures (400, 500, 600 and 700°C). As stated previously, care must be taken with the results corresponding to the RTA temperature of 700°C because of the significant decrease in the nitrogen-to-silicon ratio,  $x$ , due to the release of nitrogen atoms. In agreement with the results obtained for the  $x = 0.97$  case, we can see that RTA treatments increase the interfacial state density. Therefore, we state that a value of  $x$  lower than 1.50 is not sufficiently high to cause nitrogen atoms to fill some phosphorous vacancies or, tentatively, to promote the formation of P–N and/or In–P–N complexes that passivate the interface.<sup>20)</sup> As a consequence, the insulator-semiconductor interface remains damaged after RTA treatments.

Concerning the conductance transient analysis, in Fig. 4 we have plotted conductance transients [Fig. 4(a)] and DIGS damage density as a function of the distance from the interface and of the energy position measured from the insulator conduction band edge [Fig. 4(b)] corresponding to the Al/SiN<sub>1.43</sub>:H/InP samples. As evident from this figure, DIGS damage only diminishes for an RTA temperature of 400°C. In contrast, temperature values higher than 400°C increase DIGS damage. Thus, RTA-enhanced defect exchange between the insulator and the interface is observed at a temperature of 400°C, whereas at higher temperatures both interface and DIGS damage are increased.

#### 4. Conclusions

We have carried out the electrical characterization of low nitrogen content ECR *ex situ* silicon nitride deposited Al/SiN<sub>*x*</sub>:H/InP structures using *C–V*, DLTS and conductance transient analysis techniques. Regarding dielectric composition, both  $x = 0.97$  and  $x = 1.43$  values provide interfacial state density and DIGS damage values in the same order of magnitude, in agreement with our previous studies<sup>6)</sup> in which we demonstrated that  $D_{it}$  values strongly depend on dielectric composition for only N-rich insulators; for low N compositions  $D_{it}$  remains practically unchanged.

Regarding the effect of post deposition RTA treatments on the electrical characteristics of Al/SiN<sub>*x*</sub>:H/InP structures, we have observed that for  $x = 0.97$ , RTA treatments move the insulator damage to the interface. In contrast, in Al/SiN<sub>1.43</sub>:H/InP structures, this behavior is only observed for RTA temperatures lower than 500°C; higher temperature values increase both interface and DIGS damage.

Therefore, we can conclude that moderate temperature (<500°C) RTA treatments reduce DIGS damage, and thus, the insulator electrical properties are also improved. In contrast, interfacial state damage is slightly increased. This re-

sult is important because the main attraction of N-poor insulators is that they have good electrical properties, and we have shown that RTA treatments at moderate temperatures improve them. Moreover, as our previous studies related to N-rich and bi-layered insulators have shown, 400°C-RTA treatments improve interfacial state density. Our final conclusion is that RTA treatments at temperatures lower than 500°C are adequate to improve both interface state density and electrical properties of bi-layered structures.

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- 1) L. S. How, K. Chun, J. L. Courant, A. Falcou, P. Ossart and G. Post: *Microelectron. Eng.* **36** (1997) 69.
- 2) M. D. Biedenbender and V. J. Kapoor: *J. Electrochem. Soc.* **137** (1990) 1537.
- 3) A. Kapila, X. Si and V. Malhotra: *Appl. Phys. Lett.* **62** (1993) 2259.
- 4) Z. Yin and F. W. Smith: *Phys. Rev. B* **43** (1991) 4507.
- 5) S. García, I. Mártil, G. González-Díaz and M. Fernández: *Semicond. Sci. & Technol.* **12** (1997) 1650.
- 6) S. García, I. Mártil, G. González-Díaz, H. Castán, S. Dueñas and M. Fernández: *J. Appl. Phys.* **83** (1998) 600.
- 7) E. Redondo, N. Blanco, I. Mártil, G. González-Díaz, R. Peláez, S. Dueñas and H. Castán: *J. Vac. Sci. & Technol. A* **17** (1999) 2178.
- 8) S. Dueñas, R. Peláez, H. Castán, R. Pinacho, L. Quintanilla, J. Barbolla, I. Mártil, E. Redondo and G. González-Díaz: *J. Mater. Sci.: Mater. Microelectron.* **10** (1999) 373.
- 9) E. Redondo, N. Blanco, I. Mártil and G. González-Díaz: *Appl. Phys. Lett.* **74** (1999) 991.
- 10) R. Peláez, H. Castán, S. Dueñas, J. Barbolla, E. Redondo, I. Mártil and G. González-Díaz: *J. Appl. Phys.* **86** (1999) 6924.
- 11) L. He, H. Hasegawa, T. Sawada and H. Ohno: *Jpn. J. Appl. Phys.* **27** (1988) 512.
- 12) L. He, H. Hasegawa, T. Sawada and H. Ohno: *J. Appl. Phys.* **63** (1988) 2120.
- 13) M. Schulz and N. M. Johnson: *Appl. Phys. Lett.* **31** (1977) 622.
- 14) T. Hashizume, H. Hasegawa, R. Riemenschneider and H. L. Hartnagel: *Jpn. J. Appl. Phys.* **33** (1994) 727.
- 15) S. Dueñas, R. Peláez, H. Castán, R. Pinacho, L. Quintanilla, J. Barbolla, I. Mártil and G. González-Díaz: *Appl. Phys. Lett.* **71** (1997) 826.
- 16) H. Castán, S. Dueñas, J. Barbolla, E. Redondo, N. Blanco, I. Mártil and G. González-Díaz: to be published in *Microelectron. Reliab.*
- 17) S. Dueñas, H. Castán, J. Barbolla, I. Mártil and G. González-Díaz: submitted to *Appl. Phys. Lett.*
- 18) F. Martínez, I. Mártil, G. González-Díaz, B. Selle and I. Sieber: *J. Non-Cryst. Solids* **523** (1998) 227.
- 19) H. Castán, S. Dueñas, J. Barbolla, N. Blanco, I. Mártil and G. González-Díaz: submitted to *J. Appl. Phys.*
- 20) M. Losurdo, P. Capezutto, G. Bruno and E. A. Irene: *J. Vac. Sci. & Technol. A* **17** (1999) 2194.