Effect of interlayer trapping and detrapping on the determination of interface state densities on high-k dielectric stacks

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***Abstract*— Al/HfO_2/SiNx:H/n-Si metal-insulator-semiconductor (MIS) capacitors have been studied by electrical characterization. Films of silicon nitride were directly grown on n-type silicon substrates by electron-cyclotron-resonance assisted chemical-vapor-deposition (ECR-CVD). Silicon nitride thickness was varied from 2.96 to 6.64 nm. Afterwards, 12 nm thick hafnium oxide films were deposited by the high-pressure reactive sputtering (HPS) approach. Interface state densities were determined by deep-level transient spectroscopy and simultaneous high and low frequency capacitance-voltage (HLCV). The simultaneous measurements of the high and low frequency capacitance voltage provide interface trap density values in the range of 10^{11} $cm^{-2}eV^{-1}$ for all the samples. However, a significant increase of this density of about two orders of magnitude was obtained by DLTS for the thinnest silicon nitride interfacial layers. In this work we probe that this increase is an artifact that must be attributed to traps existing at the HfO_2/SiN_x:H interlayer interface. These traps are more easily charged or discharged as this interface comes near the substrate, that is, as thinner the SiN_x:H interface layer. The trapping/detrapping mechanisms increase the capacitance transient and, in consequence, the DLTS measurements have contributions not only from the insulator/substrate interface but also from the HfO_2/SiN_x:H interlayer interface.**

I. Introduction

High permittivity (high-k) dielectrics are nowadays being subject of great study in order to replace SiO_2 as gate dielectric in metal-oxide-semiconductor field-effect transistors (MOSFET's) in the future scales of integration [1], [2]. To achieve performance comparable to silicon oxide, high-k dielectrics have to fulfill some requirements: high quality interface with Si, thermodynamic stability in contact with Si, high recrystallization temperature, high bandgap and lower leakage conduction than silicon oxide at an equivalent oxide thickness. HfO_2-based materials are among the most promising of such materials [1] - [3].

However, before these materials can replace SiO_2 as gate dielectric, the nature and formation of electrically active defects existing in these emerging materials should be known. Defects in SiO_2 are passivated by hydrogen, but this can cause some problems in HfO_2 [4]. Moreover, as most of the high-k materials, when deposited in direct contact with Si an interfacial layer (few nanometers thick) is formed [5]. We have confirmed, in an earlier work, the formation of silicon oxide (SiO_x) as interfacial layer when depositing HfO_2 on Si [6]. This non-controlled interfacial layer can increase interfacial state density D_{it} and leakage current. The use of silicon nitride instead of silicon oxide as barrier layer can improve the effective capacitance of the gate dielectric stack, since silicon nitride has higher permittivity (≈7) than silicon oxide (≈*3.9*). Moreover, SiN_x layer prevents the growth of silicon oxides when high-k dielectric is deposited and it's known that the use of nitrides greatly reduces boron diffusion from the heavily doped poly-Si gate electrode to the lightly doped Si channel [7].

In this work we focus our attention on the interface density as measured by two techniques: deep-level transient spectroscopy and simultaneous high and low frequency capacitance-voltage (HLCV). Hafnium oxide was grown by high pressure sputtering (HPS) using Ar as processing gas,

TABLE I
ECR-CVD DEPOSITION TIME, SILICON NITRIDE THICKNESS AND INTERFACE STATE DENSITIES PROVIDED BY DLTS AND HLCV MEASUREMENTS.

Sample	ECR CVD time (s)	SiN_x:H thickness (nm)	RTA	D_{it} (x10^{11} $cm^{-2}eV^{-1}$)	
				DLTS	HLCV
Asd_1	90	6,6 ± 0,4	As-deposited	3–5	3.0
RTA_1	90	6,6 ± 0,4	600 ºC, 30s	2 - 5	2.2
Asd_2	60	5,9 ± 0,4	As-deposited	0.8 – 1	1.3
RTA_2	60	5,9 ± 0,4	600 ºC – 30s	1 - 2	2.7
Asd_3	30	3,9 ± 0,2	As-deposited	Not measured	4.5
RTA_3	30	3,9 ± 0,2	600 ºC – 30s	100 - 200	4.4
Asd_4	15	3,0 ± 0,4	As-deposited	50 - 100	2.0
RTA_4	15	3,0 ± 0,4	600 ºC - 30s	50 - 100	1.9

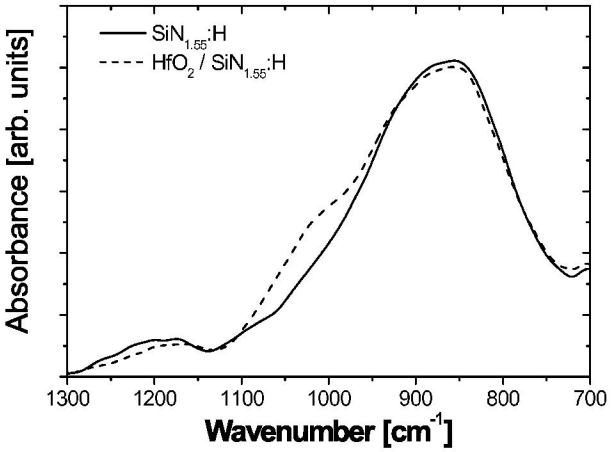

Fig. 1. FTIR spectrum of a HfO_2/SiN_x:H/Si stack (dotted line). Also shown, the FTIR spectra of a SiN_x:H film (solid line). Notice that the peak position of the main $SiN_{1.x}$:H vibration is unaffected after the HfO_2 plasma deposition process.

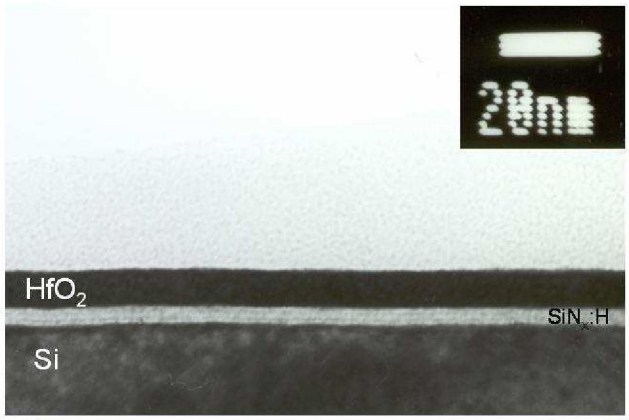

Fig. 2. Cross sectional image of a HfO_2/SiN_x:H structure. SiN_x:H thickness is 2.9 nm.

while silicon nitride was grown by electron cyclotron resonance – chemical vapor deposition (ECR-CVD), using SiH_4 and N_2 as precursors. We have studied the effect of SiN_x:H thickness in the electrical characteristics while keeping HfO_2 thickness constant at 12 nm.

II. Experimental

A. Sample Preparation

MIS structures were obtained as follows: substrates used were n-Si (polished on one side, 5 Ω cm resistivity, 500 μm thick). Before the dielectric films were deposited on the substrates, these were submitted to a standard RCA (Radio Corporation of America) cleaning. Deposition of silicon nitride was conducted in a home-made chamber attached to an ECR Astex 4500 Reactor. A mixture of high purity silane (SiH_4) and N_2 were used as precursors. Deposition times were 90, 60, 30 and 15 seconds giving rise to four different thicknesses (6.6, 5.8, 3.9, and 3 nm, respectively). Two series were obtained for each thickness, being one of them submitted to a rapid thermal annealing (RTA) at 600 °C for 30 seconds. Afterwards, 12 nm HfO_2 films were grown in an HPS system at pressure of 1.2 mbar during 30 minutes, keeping the temperature at 200 °C. High-k dielectric films were grown in a pure Ar atmosphere, because a preliminary study showed that these films presented an amorphous structure [8]. After the dielectric deposition, aluminum dot electrodes were e-beam evaporated through a shadow mask. Table I lists the samples obtained and the DLTS and HLCV experimental results.

The FTIR spectra of the SiN_x:H thin film, and the HfO_2/SiN_x:H stacked structure obtained after HfO_2 deposition in Ar atmosphere are shown in Fig. 1. The FTIR spectrum of the SiN_x:H layer has the characteristic Si-N stretching band located at 844 cm^{-1}. After the HfO_2 deposition, a smooth shoulder-like feature appears at about 1018 cm^{-1}, slightly above the frequency corresponding to the Si-O-Hf configuration (970 cm^{-1}) [14]. We tentatively attribute this band to the vibration of bonding groups involving Si, O, N, and Hf which may be formed at the HfO_2/SiN interface in small concentration.

In Fig. 2, a TEM image of a typical structure in wich SiN_x:H film has a 2.9 nm thickness is shown. From the figure, a smooth surface topography can be observed. Also well defined SiN_x:H/Si and HfO_2/ SiN_x:H interfaces can be clearly seen. The TEM image shows that the SiN_x:H film is unaltered after the deposition of the amorphous HfO_2 film in Ar plasma.

B. Experimental results

HLCV measurements summarized in Table I provide similar interface density (D_{it}) values (2-4×10^{11} cm^{-2} eV^{-1}) for all the samples, regardless the silicon nitride layer thickness. In contrast, DLTS results (Fig. 3) are clearly arranged in two groups: one corresponding to the thickest samples which has D_{it} densities from 8×10^{10} cm^{-2} eV^{-1} to 4×10^{11} cm^{-2} eV^{-1}, in good agreement with HLCV results, and the other

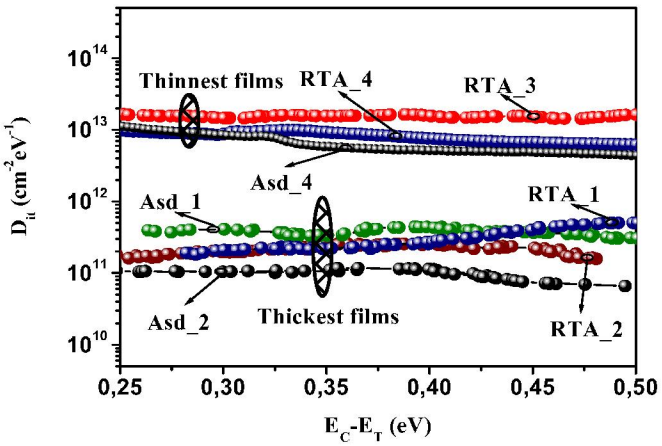

Fig. 3. Interfacial state densities measured by DLTS

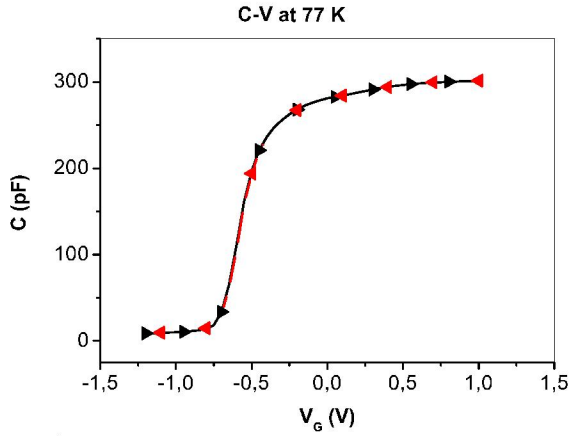

Fig. 4. 1 MHz C-V curves for a 3 nm SiN_x:H sample for voltage varying from reverse to accumulation (►) and vice versa (◄).

corresponding to the thinnest samples with D_{it} density values (from 6×10^{12} cm^{-2} eV^{-1} to 2×10^{13} cm^{-2} eV^{-1}) much higher than those obtained by HLCV. In order to explain these discrepancies we have carried out an exhaustive analysis which lead us to conclude that charging and discharging mechanisms of inner traps existing at the HfO_2/SiN_x:H affect the DLTS results. These mechanisms are tunneling assisted and, consequently, they become more important for the thinnest films.

Fig. 4 plots the C-V curves for a sample with 3 nm-thick SiN_x:H layer. The low stretch-out observed in C-V means that the trap density is very low (contrary to the DLTS results). On the other hand, no hysteresis appears regardless the voltage swing direction, so indicating that slow traps which usually exist in the insulator bulk have also very low densities and do not affect the capacitance measurements. Therefore, we have to look for one other agent causing the above mentioned discrepancies between DLTS and HLCV and we focused our attention in the traps existing at the surface between the SiN_x:H interface layer and the HfO_2 film.

First, we have recorded the interface state density profiles obtained from DLTS when varying the bias conditions. Fig. 5(a) shows important variations in the D_{it} profiles when the accumulation filling pulse voltage is varied while keeping constant the reverse voltage (when the capacitance transients are recorded). On the contrary, no significant differences are obtained when varying the reverse voltage (Fig. 5(b)). These results clearly indicate that is during the filling pulses when the mechanisms responsible for the extremely high DLTS profiles occur.

The energy band diagrams of the MIS structures under accumulation and inversion are displayed in Fig. 6. To construct them we have included the published values of the bandgap and the conduction and valence band offsets of hafnia and silicon nitride relative to silicon. We also assume that defects exist at the HfO_2/SiN_x:H interface (inner layer interface defects, ILI defects) with energies in the whole HfO_2 bandgap. DLTS measurements consist of applying accumulation pulses to fill the interface states in the upper half of the semiconductor bandgap followed by reverse pulses in which interface states emit electrons to the conduction band yielding the capacitance transients that are conveniently recorded and processed to obtain the D_{it} distribution. If the SiN_x:H film is thin enough, tunneling between the semiconductor and the inner layer interface (ILI) may occur. At accumulation, ILI states are filled by capturing electrons coming from the semiconductor conduction band by direct tunneling. Then, when the reverse pulse is applied these defects emit the captured electrons to the semiconductor band. These processes may occur in two different ways: For energies ranging from the Fermi level to the semiconductor conduction band, by tunneling between the ILI states and the interface states. Afterwards, these interface states emit electrons to the conduction band in a similar way as occurs in conventional DLTS. This extra charge increases the amplitude of the capacitance transients and, consequently, the DLTS interface

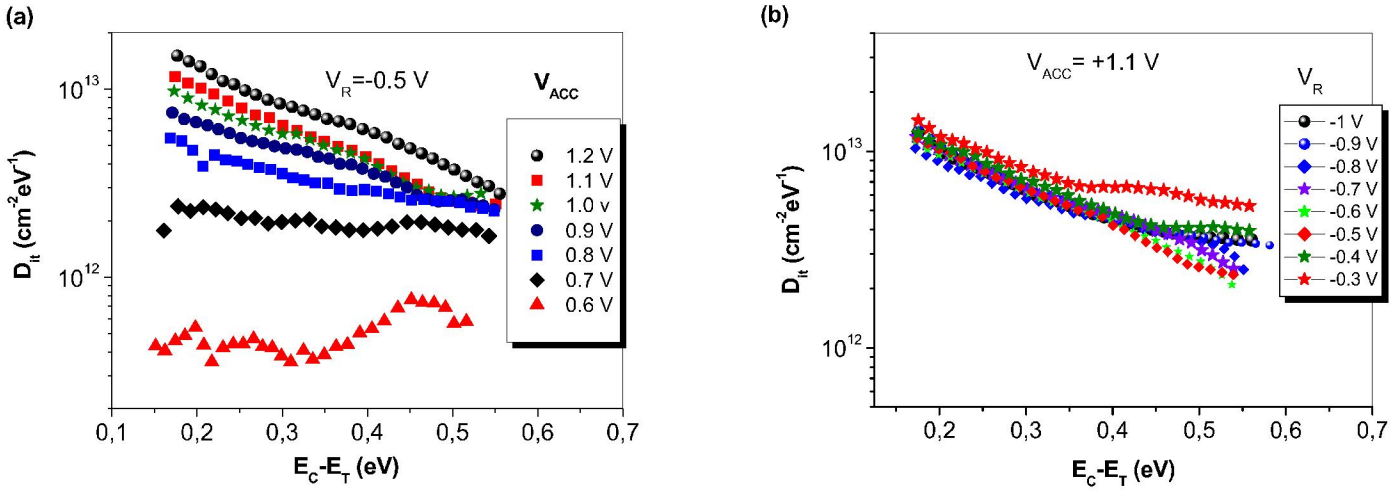

Fig. 5. DLTS profiles obtained keeping constant the voltage of the reverse-emptying-pulse (a) and the accumulation-filling pulse (b).

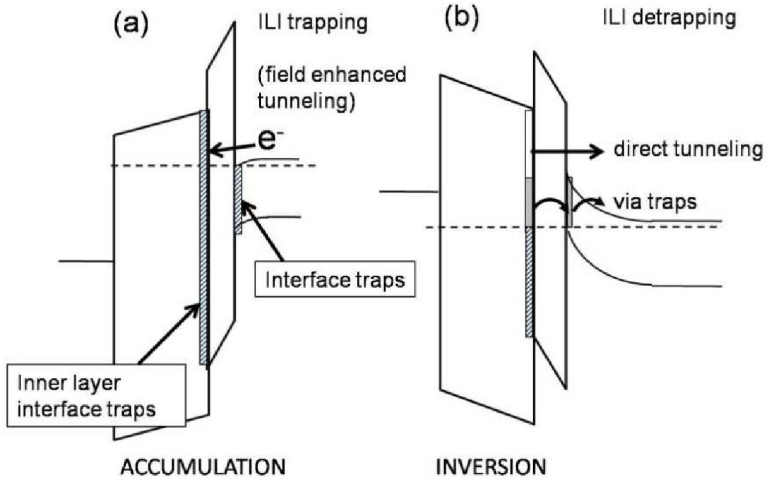

Fig. 6. Energy band diagram of the HfO_2/SiN_x:H/Si MIS structure at accumulation (a) and inversion (b).

state density values are derived. ILI states with energies over the silicon conduction band emit electrons by direct tunneling and, then, do not contribute to the DLTS results. Since all these mechanisms are tunneling assisted, as thinner the Si_3N_4 film as higher their probability. In our experiment, the Si_3N_4 layer thickness has been varied from around 3 to 6.6 nm.

To estimate the relationship between the tunneling charging/discharging probabilities for two samples with different Si_3N_4 thickness (t_1 and t_2), we can use the following quantum mechanics expression:

$$\frac{p_1}{p_2} = exp\left[\frac{2\pi\sqrt{2m_h\overline{\varphi_v}}}{h}(t_1 - t_2)\right] \qquad (1)$$

where m_h is the hole effective mass inside the barrier, $\overline{\varphi_v}$ is the mean barrier height, t_1 and t_2 are the barrier thickness and h is the Plank's constant. For the h-well triangular barrier, $\overline{\varphi_v} = \Delta E_V/2$, where ΔE_V is the valence band offset of silicon nitride relative to silicon. Gritsenko et al. [9] reported values of $\Delta E_V \approx 1.5$ eV and $m_h/m_0=(0.3\pm0.1)$. Here m_0 is the free electron mass. These values yield a relation of $p_1/p_2 = 10^{-4}$ for two layers of 6 and 3 nm, respectively, so indicating that the ILI trapping/detrapping mechanisms is negligible for thicker samples. However that is not the case for the thinnest ones, increasing the total charge emitted during the DLTS reverse pulses.

III. Conclusion

The significant increase on the interface density of about two orders obtained by DLTS for very thin silicon nitride layers in HfO_2/SiN_x:H gate stacks is an artifact caused by tunneling assisted charging and discharging of traps existing at the HfO_2/SiN_x:H interlayer interface. The trapping/detrapping mechanisms increase the capacitance transient and, in consequence, the DLTS measurements have contributions not only from the insulator/substrate interface but also from the HfO_2/SiN_x:H interlayer interface. In summary, we can conclude that interface state densities obtained by DLTS in the specific case of the HfO_2/SiN_x:H/Si system provides overestimated D_{it} values for very thin silicon nitride layers.

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