

NOISE PERFORMANCE OF SUBMICRON HEMT CHANNELS UNDER LOW POWER CONSUMPTION OPERATION

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ABSTRACT

We have investigated the noise performance of HEMT devices for low noise operation with the aim of developing a noise model valid for low power biasing. Analytical expressions useful for CAD models have been derived for the calculation of the Pospieszalski gate and drain temperatures, and have been verified from near pinchoff conditions up to usual bias voltages. An overshoot in the drain temperature as a function of the drain voltage has been observed at low drain currents in deep submicron gate length devices.

INTRODUCTION

Optimum noise performance in HEMT devices may demand for bias currents that can be too large in low power consumption applications. A good tradeoff between power consumption and low noise operation can only be achieved in a design if a model valid for a wide range of bias currents is available.

Different approaches have been pursued in the noise modeling of HEMT devices [1]-[4]. Among them, the one proposed by Pospieszalski [3] has emerged as one of the most accurate and convenient HFET noise models for CAD techniques. This model needs the empirical calculation of two different temperatures: T_G , associated to the intrinsic gate to source resistance and T_D , associated to the drain resistance. T_G has a weak influence on the final

calculated noise parameters, and in fact it has been shown that this temperature can be set to the room temperature if the drain current is not too high [5], [6]. However, T_D does exhibit a strong influence on the drain current.

The aim of this work is to investigate how T_G and T_D vary as a function of the applied bias under low drain current operation, and to present an unified expression able to predict the values of these temperatures in a wide range of bias currents and gate voltages. With this aim in mind, on wafer noise measurements of HEMT devices were performed in the range 2-26 GHz and for bias conditions ranging from near pinchoff to high cutoff frequency operation. In addition, the accuracy of the Pospieszalski model has been tested at all the measured bias points.

DEVICE MEASUREMENTS

The measured transistors were designed at the University of Chalmers and fabricated at the Philips Limeil Labs. They are 0.15 μm gate-length devices based on GaAs technology with AlGaAs/InGaAs channels. These devices feature a grounded source with a via hole that provides stabilization and facilitates broad band design. A minimum noise figure less of 1 dB was measured at 26 GHz under optimum noise performance biasing, whereas a transconductance of 700 mS/mm and maximum oscillation frequency of 200 GHz were both obtained under maximum gain bias conditions.

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On wafer noise and S parameter measurements were performed in the range 2-26 GHz by using a probe station with a network analyzer (HP8510) and an automated noise measurement system ATN NP5. A Transmission Reflection Line (TRL) calibration kit was especially designed and fabricated in the same wafer of the devices, with the aim of avoiding the inaccuracies derived from the influence of the terminal pads.

NOISE SIMULATION

The small signal equivalent circuit of the devices was extracted using an inhouse Labview program based on the cold FET method [6], [7]. In order to test the accuracy of the circuital model, an error function based on the discrepancies between the measured and the simulated S parameters was estimated [8]. Figure 1 shows the calculated errors in the simulation of the S parameters. At the highest bias currents and low drain voltages the error reaches high values due the neglect in our model of the gate to source resistance. However, the model provides a reasonable fit even for negative drain voltages. In addition, the errors in the S parameters were below 3% at all the bias points at which the noise measurements were performed.

The Pospieszalski model was used to simulate the noise performance of the devices [9]. In order to test the accuracy of this model, an error function was defined and estimated in the noise calculations. This function accounts for the discrepancies between the measured and the simulated noise parameters and has been described elsewhere [10]. The temperatures T_D and T_G were initially extracted from the noise measurements and then tuned by direct optimization. Once the optimized values were calculated, a non linear curve fitting was made to obtain an analytical expression for both T_G and T_D as a function of the drain current density.

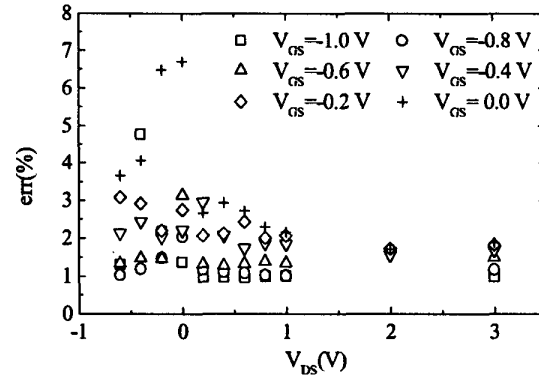


Figure 1. Errors in the extraction of the small signal parameters with the cold FET method. The drain voltages selected for the noise measurements were kept in the range 0.2 V - 3 V.

An accurate prediction of the noise parameters was achieved by assuming a linear dependence for T_G and an hyperbolic one for T_D with a current density offset,

$$T_D = T_{D0} \cosh \frac{J_D - J_0}{J_1}$$

where T_D is the drain temperature, and T_{D0} , J_0 and J_1 are fitting factors. The final values of the fitting factors are shown in figure 2 for a 100 micron width transistor. This expression is able to reproduce two remarkable features of the drain temperature at low bias currents:

- Despite the large values of the noise figure that can be obtained near pinchoff operation, T_D tends to the room temperature when *both* the drain and gate voltages tend to zero. This feature demonstrates that T_D behaves as a physical noise temperature: it tends to the room temperature near equilibrium.
- T_D exhibits an overshoot as a function of the drain voltage at low drain currents. This overshoot can clearly be observed in our samples at around 15 mA of drain current, where T_D reaches values of near 2000 K for a V_{DS} of 1.1 V

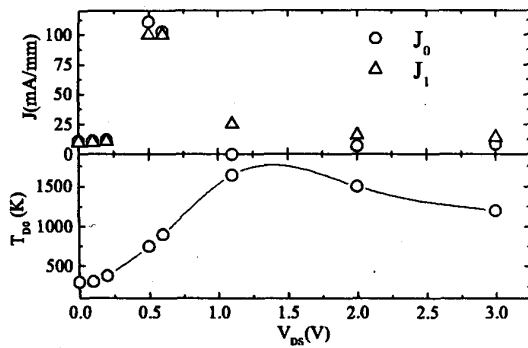


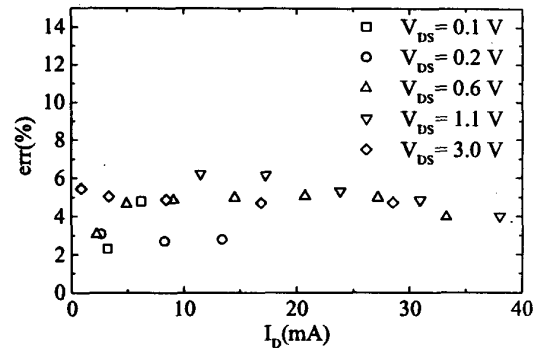
Figure 2. (a) Drain voltage dependence of the fitting parameters for the drain temperature.

and around 1300 K for V_{DS} equal to both 3 V and 0.5 V. This effect could be attributed to the noise suppression under ballistic regime that has been observed by Matulionis et al. in pulsed noise measurements of ungated HEMT structures [11], [12].

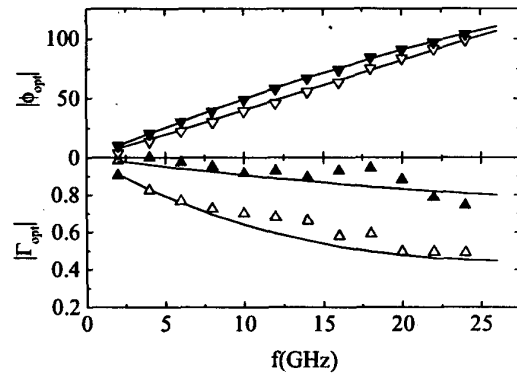
Figure 3 shows the errors obtained in the calculation of the noise parameters before and after optimization, together with a typical fit of the S and noise parameters. The optimization could not improve the fitting at the highest drain voltages. However, below 1 V the calculated values of the gate temperatures became inaccurate and gave unrealistic values at the highest currents. The optimization in this case could help to obtain noticeable improvements in the accuracy of the calculations. It must be pointed out that once the temperatures are optimized the accuracy of the model is excellent near pinchoff operation, where noise figures in excess of 6 dB and noise resistances in excess of 350 Ohm were measured.

CONCLUSIONS

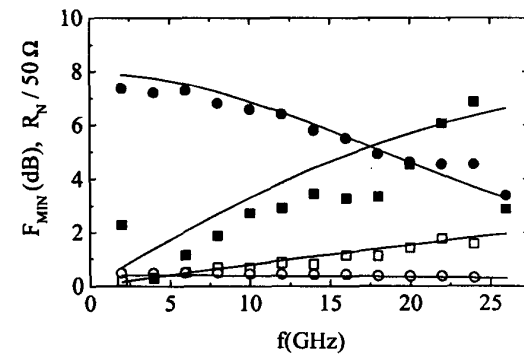
The comparison between the measurements and simulation with the Pospieszalski model of the noise performance of HEMT devices have revealed us that this model can accurately reproduce the noise parameters of the device even under near pinchoff operation. Although at



(a)



(b)



(c)

Figure 3. (a): Errors in the noise simulations after the optimization. (b), (c): Measured (symbols) and simulated (lines) noise parameters corresponding to $V_{DS} = 3$ V and $V_{GS} = 0$ V (open, error=4%) and $V_{DS} = 0.1$ V and $V_{GS} = -0.2$ V (solid, error=5%). Squares in (c) are F_{MIN} and circles are normalized R_N .

low drain bias voltages the direct extraction of the gate temperature from the measurements becomes inaccurate, a post optimization has enabled us to obtain a good accuracy in the predictions without the need for any additional refinement to the model. The optimized values of the gate and drain temperatures fit well to a linear increase for T_G and an hyperbolic one for T_D . An overshoot in T_D as a function of the gate voltage has been observed at low drain currents.

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