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Improvement of SiN_x:H/InP gate structures for the fabrication of metal–insulator–semiconductor field-effect transistors

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Abstract
In this paper we report on the optimization of the SiN_x:H insulator, deposited by the electron cyclotron resonance (ECR) plasma method, as a dielectric for metal–insulator–semiconductor (MIS) structures built on an InP compound semiconductor. Two different MIS structures have been obtained in which the minimum of the interface trap density ($D_{it,min}$) at the insulator/InP interface attains values of device quality. In the first structure, a Al/$SiN_{1.5}$:H/$SiN_{1.6}$:H/InP dual-layer insulator was obtained and optimized after rapid thermal annealing treatment at 500 °C for 30 s. After this treatment, the value of $D_{it,min}$ was 9×10^{11} cm^{-2} eV^{-1}. In the second structure, the MIS structure was Al/$SiN_{1.6}$:H/InP single-layer insulator, in which the InP surface was exposed to an N_2 plasma prior to the $SiN_{1.6}$:H film deposition. In this case, the value of $D_{it,min}$ was 1.6×10^{12} cm^{-2} eV^{-1}. Both types of structures were used as gate insulators on N-channel enhanced-mode MIS field-effect transistor test devices. From the dc output characteristics of the transistors, we obtain values for the electron channel mobility in the range 1550–1600 cm^2 V^{-1} s^{-1}. This is a confirmation of the great potential of the ECR plasma method as a simple way to obtain device quality gate structures on InP without the use of passivation processes of the InP surface prior to the deposition of the gate dielectric, thus simplifying the whole device fabrication procedure.

1. Introduction

The high electron mobility and high saturation drift velocity of GaAs and InP III–V semiconductor compounds make these the appropriate choice for microwave and high-speed field-effect based devices (MISFETs, MESFETs, MODFETs). Metal–insulator–semiconductor field-effect transistors (MISFETs) have some potential advantages over other devices, such as lower gate leakage currents, design flexibility, less dopant restrictions and higher simplicity, avoiding the use of ultra-high vacuum (UHV) techniques in the fabrication process, as in MODFET devices. The performance of MISFETs, however, critically depends on the formation of an insulator/semiconductor interface with enough low defect density. Moreover, in the case of InP based devices, the gate dielectric must be deposited at low temperature (<350 °C) to prevent the decomposition of the InP leading to the loss of phosphorous from the surface. This can cause strong interface damage, pinning the Fermi level at the InP surface.

In general, to improve the insulator/semiconductor interface and, consequently, to reduce the semiconductor surface degradation, it is necessary to use an insulator deposition technique that reduces the ion bombardment and radiation damage during the deposition process, and provides good quality insulator at low deposition temperatures. This points to the electron cyclotron resonance chemical vacuum deposition (ECR-CVD) method as a soft technique to deposit device quality SiN_x:H. This insulator has proven to be the best choice as gate insulator on MISFET devices based on III–V compound semiconductors [1, 2].

Concerning InP, to obtain a low trap density at the insulator/InP interface, many works can be found in the literature that use two main solutions:

(i) chemical passivation of the InP surface (for example, with CdS solutions [3, 4] or H_2S plasma exposure [5]) before insulator deposition;

(ii) growth on the InP surface, prior to the insulator deposition, of an interface control layer (ICL), which may be Si [6] or Si/Ge [7] with the purpose being to manage carefully the transition from the semiconductor to the insulator.

However, each solution presents some problems. In the first case, the chemical passivation process is extremely dependent on the procedure conditions being a poorly repetitive method. In the second case, the deposition of an ICL needs UHV techniques that complicate the whole fabrication process.

To avoid these technological steps, we propose the use of the following simpler procedures to form the MIS structure.

(i) Gate structures composed of two different insulator compositions that let us bring together the best SiN_x:H compositions for the interface quality and for the insulator properties. These structures have been reported elsewhere [8, 9], proving their good performance.

(ii) N_2 plasma exposure of the InP surface before the insulator deposition. This procedure has been demonstrated to reduce the interface trap density [10, 11].

(iii) Rapid thermal annealing (RTA) treatments of the MIS structure obtained in the two ways described above. This approach has been widely studied by our group in SiN_x:H/Si [12, 13], SiN_x:H/InGaAs [14, 15] and SiN_x:H/InP [16] structures, where it has been proven that the RTA treatments with temperatures between 500–700 °C, depending on the substrate, improve the whole performance of the devices.

In this paper, we first analyse the best solution to develop device quality Al/SiN_x:H/InP structures, comparing the electrical results obtained with the approaches described above. Subsequently, we present dc characterization of MISFET test devices using the different solutions in order to choose the better one among them.

2. Experimental details

MIS structures were obtained using wafers of undoped InP ($n = 5 \times 10^{15}$ cm^{-3}, (100) oriented). The samples were first degreased with organic solvents, rinsed in deionized water and dried with nitrogen. They were then superficially etched in a solution of HIO_3:H_2O (10% at weight) for 1 min and in HF:H_2O (1:10) for 15 s. We use a glove bag transfer chamber filled with pure N_2 gas in the last clean-up step to avoid the air exposure of the samples. The SiN_x:H insulator films were then deposited by the ECR-CVD technique with an Astex 4500 reactor. The deposition was done at low substrate temperature (200 °C) using SiH_4 and N_2 as precursor gases, in different ratios ($R = N_2/SiH_4$) to get different insulator compositions ($x = N/Si$) [17]. The SiN_x:H films used in this study had N-rich ($x = 1.5$–1.6) and near-stoichiometric ($x = 1.43$) compositions. The insulator thickness was 500 Å.

As we have described in the introduction, several trials of MIS structures were analysed for optimization, as follows.

(i) In the first type, the insulator deposition was performed in two steps. The first layer, deposited on InP, was chosen to be a composition of $x = 1.6$ to minimize the interface trap density [8, 9]. This is referred to as the bottom layer. Immediately afterwards, we deposit the second layer with a composition of $x = 1.5$ or $x = 1.43$ to improve ρ and E_B values. This is referred to as the top layer. The finalized gate structure is referred to as the dual-layer structure. In both cases, the total thickness is 500 Å, with a partial thickness of 100 Å for the bottom layer and 400 Å for the top layer.

(ii) In the second type, a N_2 plasma exposure was performed before a single-layer insulator deposition [10, 11]. The N_2 plasma exposure experiment was conducted under the following conditions: time duration 30 s, microwave power 60 W and N_2 gas pressure 0.5 mTorr.

(iii) After MIS formation with these procedures, RTA treatments in all of them were conducted in Ar atmosphere. The annealing temperature ranged between 300–800 °C for 30 s.

Afterwards, in all the devices, Al dots (1.2×10^{-3} cm^2) were thermally evaporated through a mechanical mask. Finally, an AuGe/Au back electrode was evaporated. A post-metallization annealing of the final devices was performed in Ar atmosphere (300 °C for 20 min).

Each MIS structure was characterized using capacitance–voltage (C–V) measurements, quasi-static (C_{QS}) and 1 MHz (C_{HF}) curves, with a Keithley Model 82 system. The interface trap density (D_{it}) was obtained using the high–low frequency method [18]. The ρ and E_B (at 1 μA cm^{-2}) values were calculated from current–voltage (I–V) measurements made in accumulation.

Test devices of the type N-channel enhanced-mode MISFETs were fabricated on (100) Fe-doped semi-insulating InP substrates by conventional photolithography. The gate dimensions were 10×100 μm^2. The source and drain contacts were formed with $^{28}Si^+$ ion implantation with a dose of 1×10^{14} cm^{-2} at 80 keV, followed by RTA activation at 800 °C for 30 s. The annealing was carried out using the face-to-face method in high purity Ar ambience. After the annealing, the InP surface was superficially etched in the same way as before the SiN_x:H deposition. Then, the gate insulator was deposited by the ECR-CVD method, as described above. Subsequently, Al was evaporated as the gate electrode. Contacts holes for source and drain electrodes were then made by reactive ion etching using SF_6, and AuGe/Au was evaporated to provide source/drain contacts.

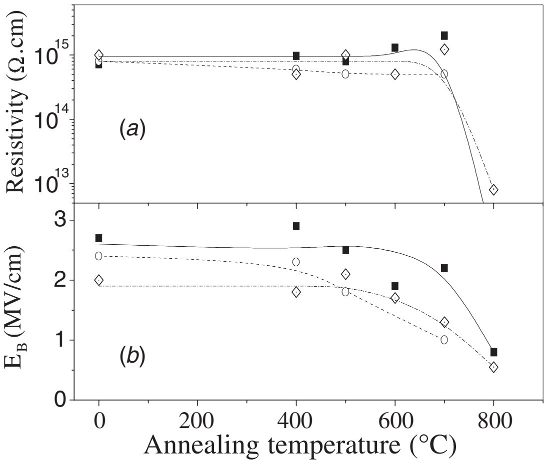

Figure 1. (*a*) Resistivity (ρ) and (*b*) breakdown field (E_B) as functions of the RTA temperatures for the following MIS structures: (■) Al/SiN$_{1.6}$:H/InP; (◇) Al/SiN$_{1.5}$:H/InP and (○) the dual-layer gate Al/SiN$_{1.5}$:H/SiN$_{1.6}$:H/InP.

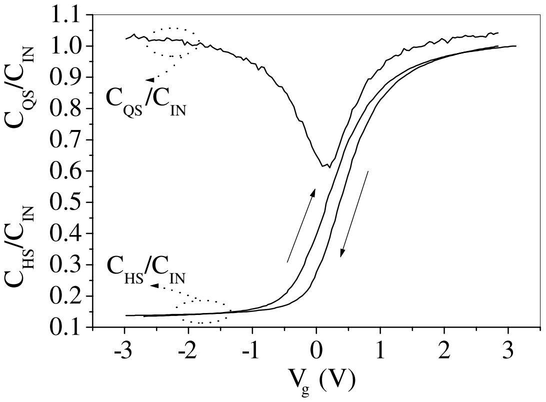

Figure 2. High-frequency (C_{HF}) and quasi-static (C_{QS}) *C–V* characteristics normalized to the insulator capacitance (C_{in}) of the Al/SiN$_{1.5}$:H/SiN$_{1.6}$:H/InP dual-layer gate structure after annealing at 500 °C for 30 s. The thickness of each layer was 100 Å ($x = 1.6$) and 400 Å ($x = 1.5$).

3. Results and discussion

3.1. MIS structures

We first analyse the results on dual-layer gate structures. In previous works [19] we have shown the influence of the nitrogen-to-silicon ratio (x = N/Si) of the films on the electrical properties of MIS structures (D_{it}, ρ and E_B). An inverse correlation between the insulator composition and interface trap density was observed. The minimum D_{it} value (3×10^{12} eV^{-1} cm^{-2}) was achieved in films with the maximum value of x ($x = 1.6$). For this composition, the values of ρ and E_B were 10^{15} Ω cm and 2 MV cm^{-1}, respectively. Better insulator properties ($\rho = 4 \times 10^{15}$ Ω cm and $E_B =$ 2.5 MV cm^{-1}) were obtained with lower x values ($x = 1.43$). However, at this insulator composition, the interface quality was worse than with $x = 1.6$, being now the minimum of the interface trap density of 4×10^{12} eV^{-1} cm^{-2}.

From these previous results, we have made dual-layer gate structures [8, 9] to join the lower interface trap densities of SiN$_{1.6}$:H compositions and the best insulator characteristics of the SiN$_{1.43}$:H or SiN$_{1.5}$:H compositions. This approach has been widely used in Si-based technology [20] but, to our knowledge, not in III–V semiconductor technology.

Figures 1(*a*) and (*b*) present the behaviour of ρ and E_B with the annealing temperature, respectively, for three groups of samples: single layer with $x = 1.6$, single layer with $x = 1.5$ and the dual-layer gate ($x = 1.5/x = 1.6$). We can observe that the insulator characteristics of the dual-layer structure are very similar to that of single layers. The ρ and E_B values are degraded with temperatures above 600 °C, as we can observe in these figures.

However, both ρ and E_B were found to be independent of the N$_2$ plasma exposure process, with values in the range $\sim 10^{15}$ Ω cm and ~2 MV cm^{-1}, respectively.

Focusing on the interface quality of these structures, in figure 2 we show the use of the annealing performed at 500 °C for 30 s on the *C–V* characteristics for Al/SiN$_{1.5}$:H/SiN$_{1.6}$:H/InP structures, which is the better structure obtained. The quasi-static C_{QS} curve presents a deep and well-defined dip, indicating the high quality of the insulator/semiconductor interface. In figure 3(*a*), we present the interface trap distribution for the following devices: single-layer Al/SiN$_{1.6}$:H/InP annealed at 500 °C for 30 s; dual-layer Al/SiN$_{1.5}$:H/SiN$_{1.6}$:H/InP annealed at 500 °C for 30 s; single-layer Al/SiN$_{1.6}$:H/InP subjected to a N$_2$ plasma exposure before the SiN$_x$:H deposition and, finally, the same device but after annealing at 500 °C for 30 s. In all these cases, the interface trap distribution has the characteristic U-shaped form. For the RTA annealed dual-layer gate structure, the distribution exhibits a minimum (9×10^{11} eV^{-1} cm^{-2}) located at 0.45 eV above midgap. The N$_2$ plasma exposure of the InP surface gives a value of $D_{it,min} = 1.6 \times 10^{12}$ cm^{-2} eV^{-1}. The effects of the N$_2$ plasma exposure together with an annealing treatment have been demonstrated [10] not to be a good option for optimization of the device. In fact, the device N$_2$ plasma exposed and then annealed at 500 °C for 30 s exhibited a minimum for the interface trap density of 3×10^{12} eV^{-1} cm^{-2}. The thermal treatment induces the desorption of phosphorous–nitrogen (P–N) and/or indium–phosphorous–nitrogen (In–P–N) complexes formed on InP during the plasma cleaning, that passivate the InP surface.

With the comparison of data shown in figure 3(*a*), we prove that the best solution to obtain gate quality MIS devices is to use the dual-layer structure as gate insulator, with a RTA treatment of 500 °C for 30 s. This optimized device presents the lowest interface trap densities and ρ and E_B values which are actually close to the best results obtained with SiN$_x$:H compositions of $x = 1.43$ or $x = 1.5$ (see figures 1(*a*) and (*b*)).

To compare our results with those procedures that use chemical passivation and/or ICLs to improve the interface behaviour, we present in figure 3(*b*) the best D_{it} distribution obtained in this work (Al/SiN$_{1.5}$:H/SiN$_{1.6}$:H/InP dual-layer gate structure annealed at 500 °C for 30 s), the results from Landheer *et al* [6] obtained in MIS structures passivated using an ICL and the results from Kapila *et al* [5], where the InP surface was treated in H$_2$S plasma. The minimum of D_{it} distribution in our structure (9×10^{11} eV^{-1} cm^{-2}), facing those obtained with S-passivation (2.5×10^{12} eV^{-1} cm^{-2}) [5] or ICL technique (4×10^{12} eV^{-1} cm^{-2}) [6], indicates

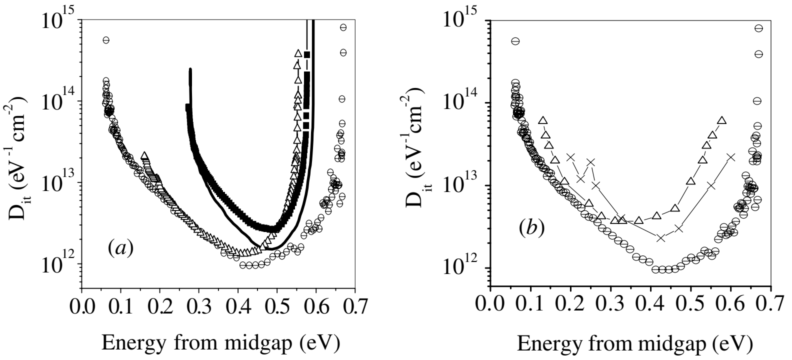

Figure 3. (*a*) Interface trap distribution (D_{it}) as a function of gap energy plotted relative to the midgap, for the dual-layer structure of figure 2 (⊖). The other distributions are for the following devices: (Δ) single-layer Al/SiN$_{1.6}$:H/InP annealed at 500 °C/30 s; (——) single-layer Al/SiN$_{1.6}$:H/InP subjected to N$_2$ plasma exposure; (■) single-layer Al/SiN$_{1.6}$:H/InP plasma exposed and annealed at 500 °C for 30 s. (*b*) Interface trap distribution as a function of gap energy plotted relative to the midgap, for the MIS structure measured in figure 2 (⊖): (Δ) results from Landheer *et al* [6] for devices passivated with an ICL; (×) results from Kapila *et al* [5] for devices treated in H$_2$S atmosphere.

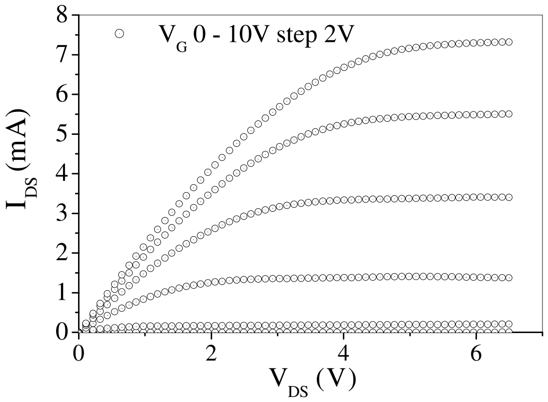

Figure 4. Output dc I–V characteristics for an N-channel InP MISFET with a gate length of 10 μm. The gate structure is Al/SiN$_{1.5}$:H/SiN$_{1.6}$:H/InP annealed at 500 °C for 30 s. The V_G steps are 2 V.

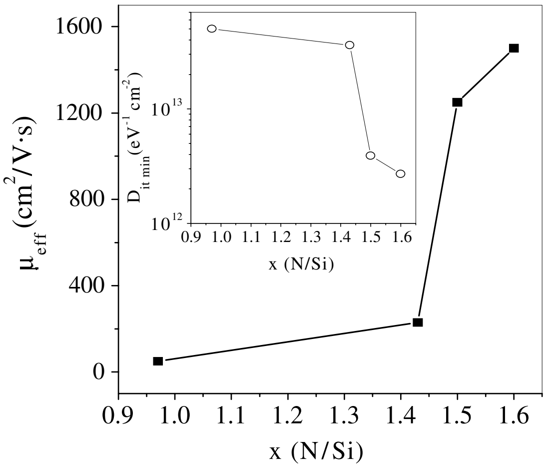

Figure 5. Evolution of the channel effective electron mobility (μ_{eff}) as a function of the insulator gate composition. The inset of the figure illustrates the evolution of the minimum of interface trap density measured in MIS structures as a function of the insulator composition.

the excellent performance of the RTA treated dual-layer gate interface without any additional treatment of the InP surface previous to the SiN$_x$:H deposition.

Arguably, high-quality C–V and I–V characteristics are necessary conditions for a viable MISFET technology. Ultimately, however, a functional MISFET is the appropriate test of a particular material system for MIS applications.

3.2. Test MISFET devices

To demonstrate the feasibility of our dual-layer gate structure for high-performance device applications, N-channel MISFET test devices were fabricated. We did not make an attempt to optimize either gate dimensions, which are quite large (with a length of 10 μm and a width of 100 μm), nor source and drain design.

Figure 4 presents the best transistor output characteristics measured in the dark with the ICS software from Keithley. The gate structure used in this device is that analysed above (Al/SiN$_{1.5}$:H/SiN$_{1.6}$:H/InP dual-layer gate structure, optimized with RTA treatment at 500 °C for 30 s). The transistor curves clearly show pinch-off characteristics and, at zero gate voltage, the device does not exhibit any leakage currents. The threshold voltage (V_{th}) is about 0.05 V. An extrinsic transconductance of 15 mS mm^{-1} was measured for the transistor in the saturation regime at room temperature.

To obtain the effective electron mobility (μ_{eff}) in the channel of the transistor, the drain current in the saturation region (I_{DS}) was obtained at a constant drain voltage (V_{DS}) for different gate voltages (V_{GS}). Using the slope of the plot I_{DS} versus V_{GS} we can obtain μ_{eff} as [21]

$$\mu_{\mathrm{eff}} = \left(\frac{L}{W}\right)\frac{\left.\left(\dfrac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}}\right)\right|_{V_{\mathrm{DS}}}}{(V_{\mathrm{GS}}-V_{\mathrm{th}})C_{\mathrm{in}}} \qquad (1)$$

where C_{in} is the gate insulator capacitance per unit area, and L and W are the length and width of the gate, respectively. A maximum channel mobility of 1600 cm^2 V^{-1} s^{-1} was measured.

On the other hand, when the gate dielectric structure was obtained with the N_2 plasma exposure already described, the dc output characteristics of the corresponding test device were similar to those shown in figure 4, with the values for the transconductance and for the effective electron mobility now being 15 mS mm^{-1} and 1550 $\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$, respectively.

The values obtained in both cases for μ_{eff} are really good results and confirm the low value of D_{it} at the SiN_x:H/InP interface in both types of test transistor. To make this fact obvious, we finally present in figure 5 the evolution of the maximum μ_{eff} values obtained in MISFET devices with simple gate structures (Al/SiN_x:H/InP), where we have ranged the insulator composition. The inset of the figure shows the evolution of the minimum D_{it} values measured in Al/SiN_x:H/InP MIS structures, with the same SiN_x:H composition. In this figure, we can observe the straight relation between μ_{eff} and D_{it}, and we can conclude that a good SiN_x:H/InP interface gives rise to less scattering mechanisms at the channel region, improving μ_{eff} (which is an indication of the microscopic surface mobility).

4. Conclusions

We have shown in this paper that both the dual-layer gate structure Al/$\mathrm{SiN}_{1.5}$:H/$\mathrm{SiN}_{1.6}$:H/InP and the single-layer Al/$\mathrm{SiN}_{1.6}$:H/InP, in which the InP surface was exposed to a N_2 plasma prior to the deposition of the insulator, have interface properties of device quality that allow us to use such structures as the gate zone in MISFET devices. The method used to deposit the SiN_x:H film insulator was the ECR-CVD plasma method. In the dual-layer gate structure, the optimization of the device with RTA treatment performed at 500 °C for 30 s gives a minimum value for the interface trap density of $9 \times 10^{11}\ \mathrm{eV}^{-1}\ \mathrm{cm}^{-2}$. This is one of the best-reported values for this parameter in MIS devices with InP.

In addition, we have developed a simple technology to fabricate N-channel enhanced-mode MISFET test transistors with non-optimized gate geometry (with a 10 μm length and a 100 μm width). With both types of gate structure, the devices exhibit good output dc characteristics, with an electron channel mobility of 1600 $\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ (dual-layer gate) and 1550 $\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$ (single layer with N_2 plasma exposure). These values show that both types of gate structure are a good choice for InP-based MISFET technology.

Acknowledgments

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